Am93L10/93L16

Low-Power BCD Decade Counter/Four-Bit Binary Counter

Distinctive Characteristics

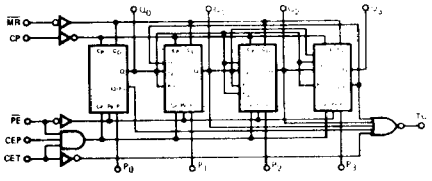
- 75 mw typical power dissipation.
- 13 MHz typical count rate
- 100% reliability assurance testing in compliance with MIL STD 883
- Fully synchronous counting and parallel loading

FUNCTIONAL DESCRIPTION

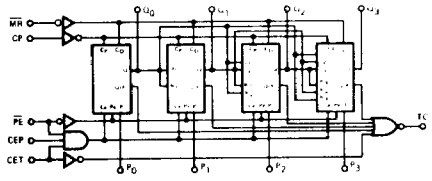
The Am93L10 and Am93L16 are four-bit synchronous up-counters. The 93L10 is a modulo 10 counter and the 93L16 is a hexadecimal counter. Each counter contains four master-slave flip-flops driven by a common clock input (CP). When CP is LOW, data is entered into the masters of the flip-flops. If the parallel enable ($\overline{PE}$) is HIGH, then data is entered into each master from the slaves of the other flip-flops via J and K type inputs. If $\overline{PE}$ is LOW, then data is entered into the masters via the D-type parallel inputs (P_0, P_1, P_2, P_3). When the clock changes from LOW to HIGH, the data in the masters is transferred to the slaves and the outputs (Q_0, Q_1, Q_2, Q_3). The masters are inhibited from change as long as the clock is HIGH. In the count mode ($\overline{PE}$ HIGH), there are two count enables, count enable parallel (CEP) and count enable trickle (CET). Both must be HIGH for counting to occur. The terminal count state of each device (9 for the 93L10 and 15 for the 93L16) is decoded and ANDed with the CET input to produce a terminal count output (TC). Long synchronous counter systems are constructed by connecting the TC output of the first counter to the CEP inputs of all other counters and the TC output of each counter after the first to the CET input of the next counter. Both counters have an asynchronous master reset ($\overline{MR}$) which clears all four flip-flops independent of any other inputs.

For proper operation, the $\overline{PE}$ input must not change from LOW to HIGH during the clock LOW time unless the P_i inputs are identical to the Q_i outputs. If CEP and CET are both HIGH at any time during the clock LOW time, (and $\overline{PE}$ is HIGH), then the count will increment when the clock goes HIGH.

Am93L10



Am93L16



LOADING RULES

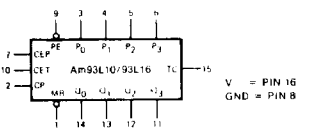
In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
CEP, $\overline{MR}$	0.5	0.25	1.0	1.0
CET, CP, $\overline{PE}$	1.0	0.5	2.0	2.0
P_0, P_1, P_2, P_3	0.34	0.17	0.68	0.68
Output Drive	HIGH	LOW	HIGH	LOW
Q_0, Q_1, Q_2, Q_3, TC	9	3	18	12

NOTES:

1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



ORDERING INFORMATION

Package Type	Temperature Range	Am93L10 Order Number	Am93L16 Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L1059X	U6M93L1659X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L1059X	U7B93L1659X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L1051X	U7B93L1651X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L1051X	U4L93L1651X
Dice	Note	UXX93L10XXD	UXX93L16XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1059X, Am93L1659X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L1061X, Am93L1651X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.36$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	µA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		15	27.5	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay—Q Outputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	18	35	50	ns
t_{pd-}	Turn On Delay—Q Outputs		20	40	55	ns
t_{pd+}(TC)	Turn Off Delay TC		40	80	95	ns
t_{pd-}(TC)	Turn On Delay TC		18	35	45	ns
t_s(CE)	Set-up Time CEP or CET	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 2)	10	50	80	ns
t_s(P)	Set-up Time P-Inputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 3)	30	70	110	ns
$t_s(\overline{PE})$	Set-up Time $\overline{PE}$		10	45	80	ns
$t_{pd-}(\overline{MR})$	Turn-on Delay for $\overline{MR}$	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	26	52	95	ns
t_{pd+}(CET to TC)	Turn Off Delay for CET to TC	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 4)	18	35	55	ns
t_{pd-}(CET to TC)	Turn On Delay for CET to TC		20	40	60	ns
f_c	Count Frequency	$V_{CC} = 5.0$ V, $C_L = 15$ pF	8	13		MHz

SWITCHING TIME WAVEFORMS

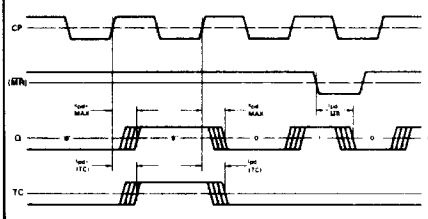


Figure 1

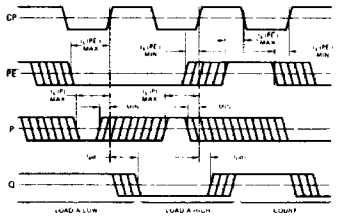


Figure 3

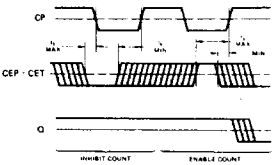


Figure 2

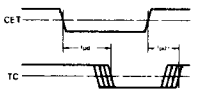


Figure 4

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901 Thompson Place
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(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

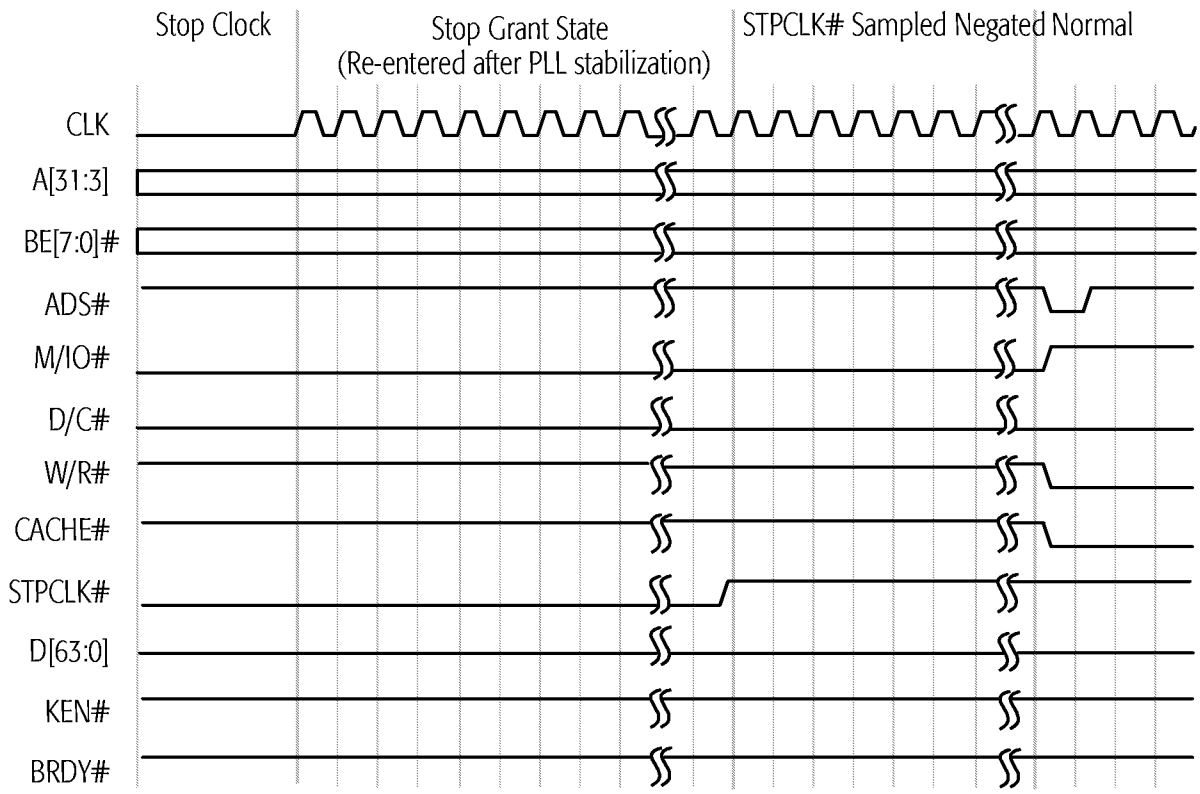

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

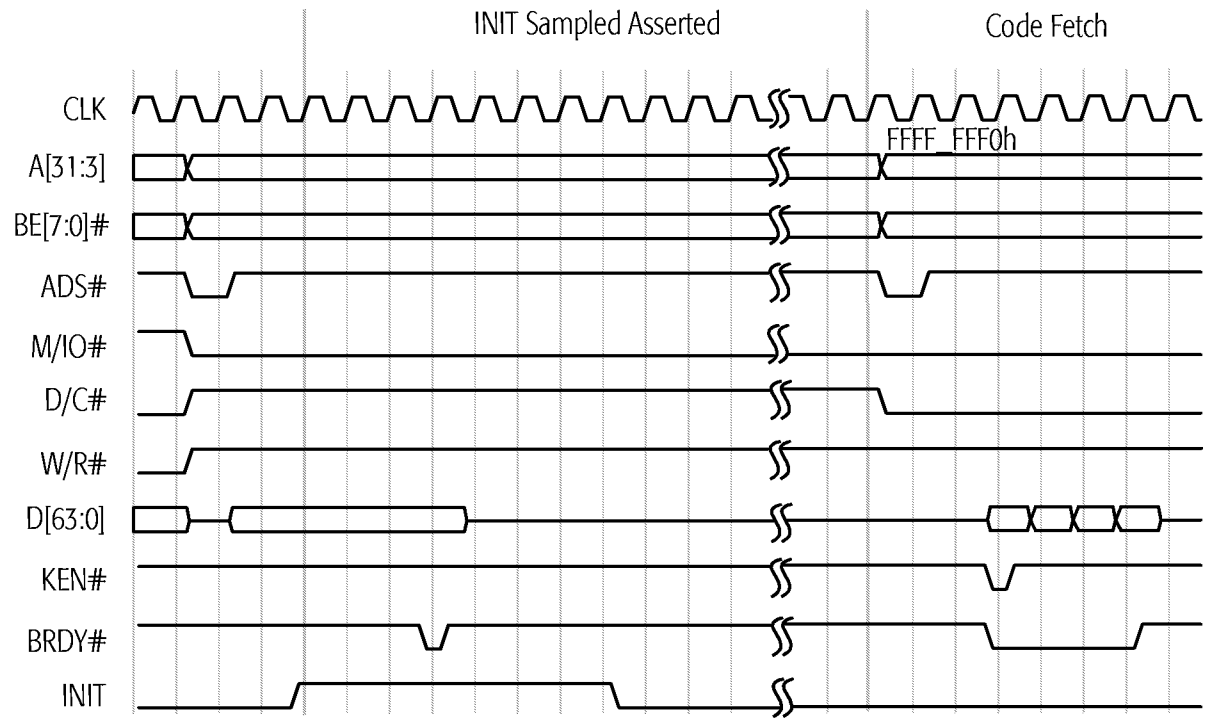

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.