SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

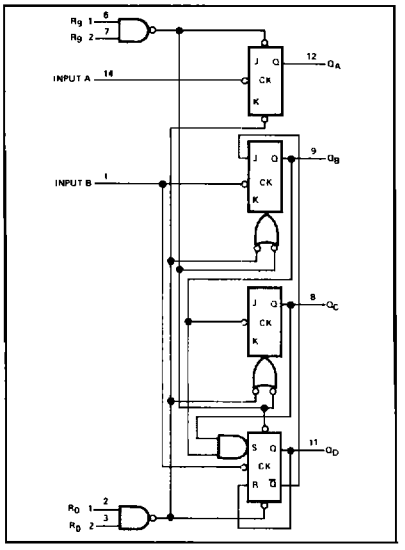
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

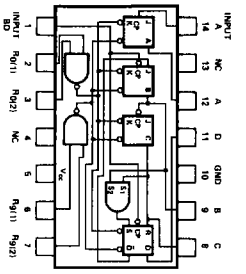
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM 54LS/74LS

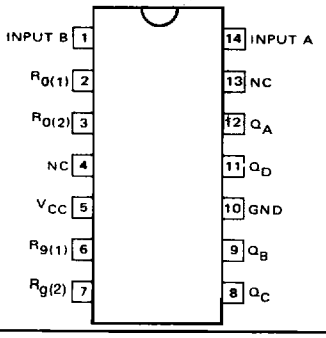


PIN CONFIGURATION

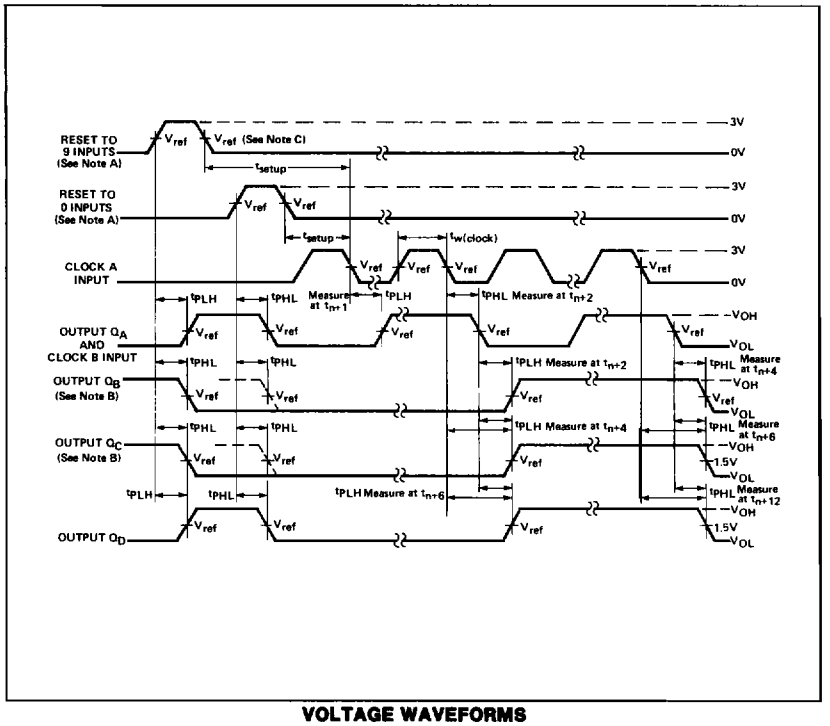
54/74
A,F,W PACKAGE



54LS/74LS
A,F,W PACKAGE



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.3 V.
Load circuit is shown at front of section (for totem pole outputs).

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
$t_{w(Clock)}$	Width of			50						ns
	clock pulse	A	Q				15			
		B	Q				30			
		Reset	Q				15			
$t_{w(Reset)}$	Width of			50			25			ns
	reset pulse									
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_C		60	100				ns
t_{PHL}	High-to-low				60	100				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					32	48	
t_{PHL}	High-to-low							34	50	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					21	32	
t_{PHL}	High-to-low							23	35	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	
t_{PLH}	Low-to-high	Set-to-9	Q_A,Q_D					20	30	
t_{PHL}	High-to-low	Set-to-9	Q_B,Q_C					26	40	

Load circuit and typical waveforms shown at front of section .

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

LOGIC