# CMOS Static RAM 1 Meg (256K x 4-Bit) Revolutionary Pinout

**IDT71128**

## Features

- **256K x 4 advanced high-speed CMOS static RAM**
- **JEDEC revolutionary pinout (center power/GND) for reduced noise.**
- **Equal access and cycle times**
  - *— Commercial and Industrial: 12/15/20ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
- **Available in a 32-pin 400 mil Plastic SOJ.**

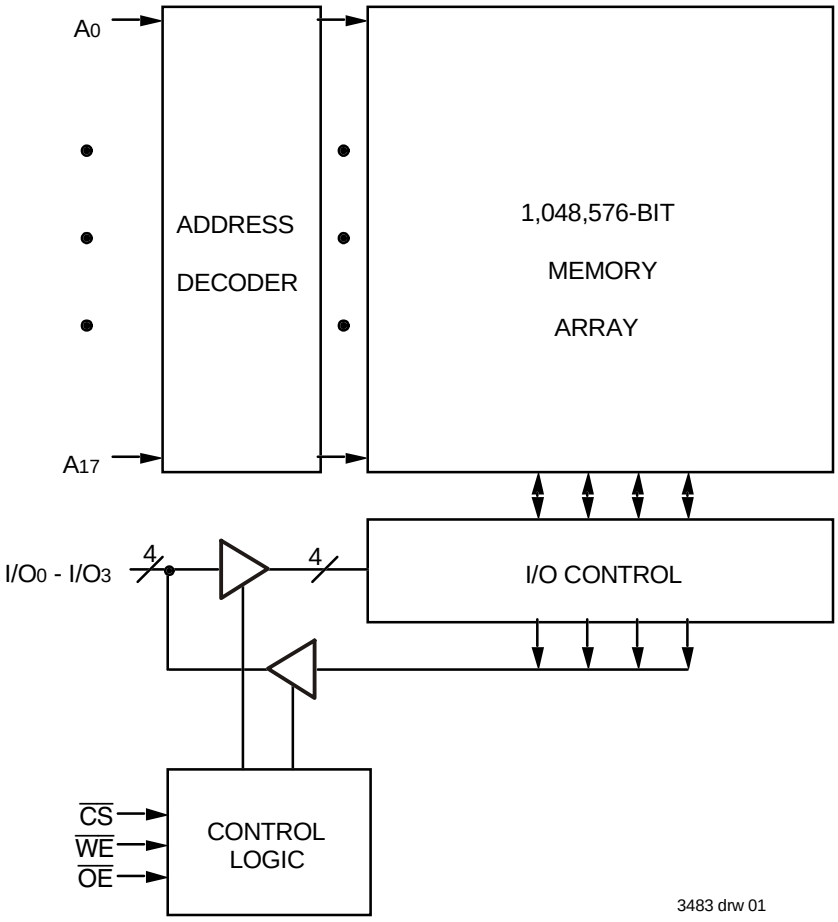
## Description

The IDT71128 is a 1,048,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

The IDT71128 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71128 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

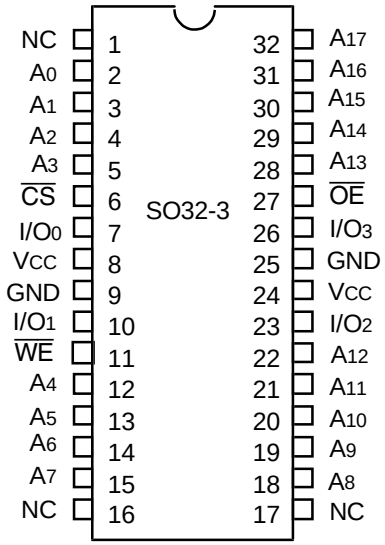
The IDT71128 is packaged in a 32-pin 400 mil Plastic SOJ.

## Functional Block Diagram




**FEBRUARY 2001**

## Pin Configuration

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**SOJ**
**Top View**

## Truth Table[1,2]

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Function |
|---|---|---|---|---|
| L | L | H | $DATA_{OUT}$ | Read Data |
| L | X | L | $DATA_{IN}$ | Write Data |
| L | H | H | High-Z | Output Disabled |
| H | X | X | High-Z | Deselected - Standby ($I_{SB}$) |
| $V_{HC}$[3] | X | X | High-Z | Deselected - Standby ($I_{SB1}$) |

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**NOTES:**
1. H = $V_{IH}$, L = $V_{IL}$, x = Don't care.
2. $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ -0.2V.
3. Other inputs ≥$V_{HC}$ or ≤$V_{LC}$.

## Absolute Maximum Ratings[1]

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | -0.5 to +7.0[2] | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C |
| $P_T$ | Power Dissipation | 1.25 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed Vcc + 0.5V.

## Capacitance

### ($T_A$ = +25°C, f = 1.0MHz, SOJ package)

| Symbol | Parameter[1] | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 8 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 8 | pF |

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**NOTE:**
1. This parameter is guaranteed by device characterization, but is not production tested.

## Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | –40°C to +85°C | 0V | 5.0V ± 10% |

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## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | -0.5[1] | — | 0.8 | V |

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**NOTE:**
1. $V_{IL}$ (min.) = –1.5V for pulse width less than 10ns, once per cycle.

# DC Electrical Characteristics
## (Vcc = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA, $V_{CC}$ = Min. | 2.4 | — | V |

3483 tbl 06

# DC Electrical Characteristics(1)
## (Vcc = 5.0V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V)

| Symbol | Parameter | 71128S12 | | 71128S15 | | 71128S20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Com'l. | Ind. | Com'l. | Ind. | Com'l. | Ind. | |
| $I_{CC}$ | Dynamic Operating Current<br>$\overline{CS} \leq V_{IL}$, Outputs Open, $V_{CC}$ = Max., f = $f_{MAX}$(2) | 155 | 155 | 150 | 150 | 145 | 145 | mA |
| $I_{SB}$ | Standby Power Supply Current (TTL Level)<br>$\overline{CS} \geq V_{IH}$, Outputs Open, $V_{CC}$ = Max., f = $f_{MAX}$(2) | 40 | 40 | 40 | 40 | 40 | 40 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current (CMOS Level)<br>$\overline{CS} \geq V_{HC}$, Outputs Open, $V_{CC}$ = Max., f = 0(2)<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | 10 | 10 | 10 | 10 | 10 | 10 | mA |

3483 tbl 07

**NOTES:**
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$ (all address inputs are cycling at $f_{MAX}$); f = 0 means no address input lines are changing.

# AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figure 1 and 2 |

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# AC Test Loads

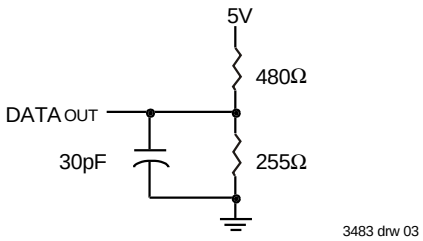
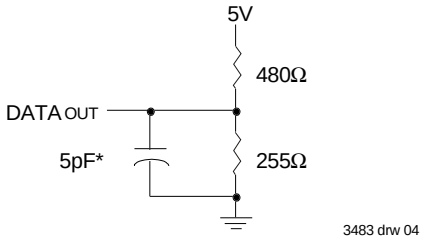



**Figure 1. AC Test Load**




*Including jig and scope capacitance.

**Figure 2. AC Test Load**
**(for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{OW}$, and $t_{WHZ}$)**

# AC Electrical Characteristics

## (Vcc = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | 71128S12 | | 71128S15 | | 71128S20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AA}$ | Address Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 12 | — | 15 | — | 20 | ns |
| $t_{CLZ}$(1) | Chip Select to Output in Low-Z | 3 | — | 3 | — | 3 | — | ns |
| $t_{CHZ}$(1) | Chip Deselect to Output in High-Z | 0 | 6 | 0 | 7 | 0 | 8 | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 6 | — | 7 | — | 8 | ns |
| $t_{OLZ}$(1) | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| $t_{OHZ}$(1) | Output Disable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 7 | ns |
| $t_{OH}$ | Output Hold from Address Change | 4 | — | 4 | — | 4 | — | ns |
| $t_{PU}$(1) | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$(1) | Chip Deselect to Power-Down Time | — | 12 | — | 15 | — | 20 | ns |
| **WRITE CYCLE** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | — | 15 | — | 20 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 10 | — | 12 | — | 15 | — | ns |
| $t_{CW}$ | Chip Select to End of Write | 10 | — | 12 | — | 15 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 10 | — | 12 | — | 15 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 7 | — | 8 | — | 9 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$(1) | Output active from End-of-Write | 3 | — | 3 | — | 4 | — | ns |
| $t_{WHZ}$(1) | Write Enable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 8 | ns |

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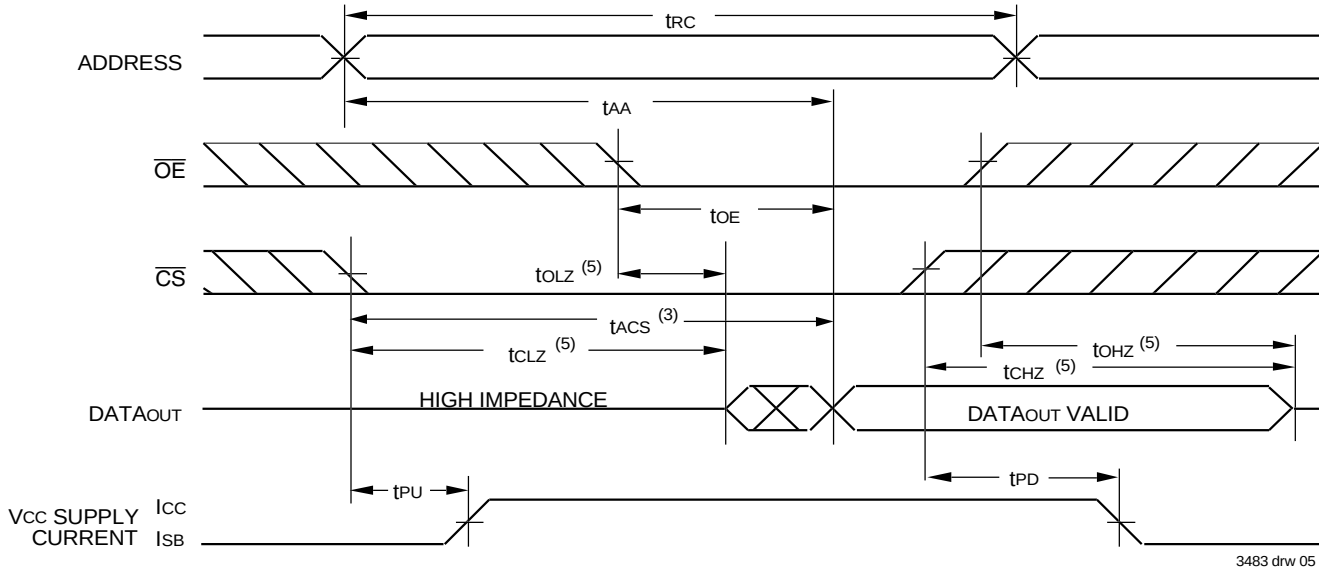
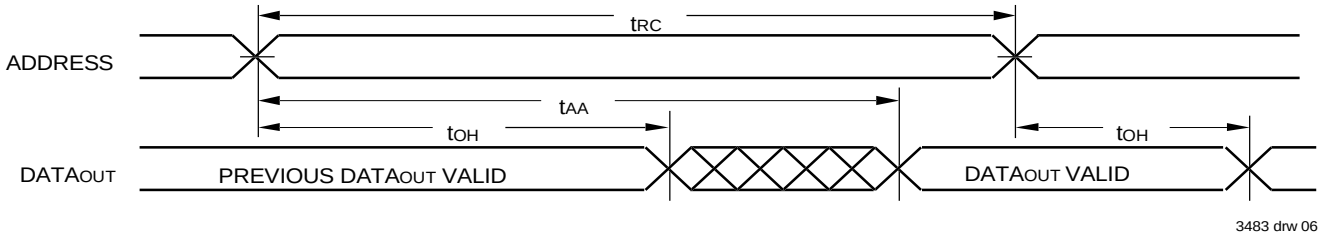
**NOTE:**
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

## Timing Waveform of Read Cycle No. 1(1)

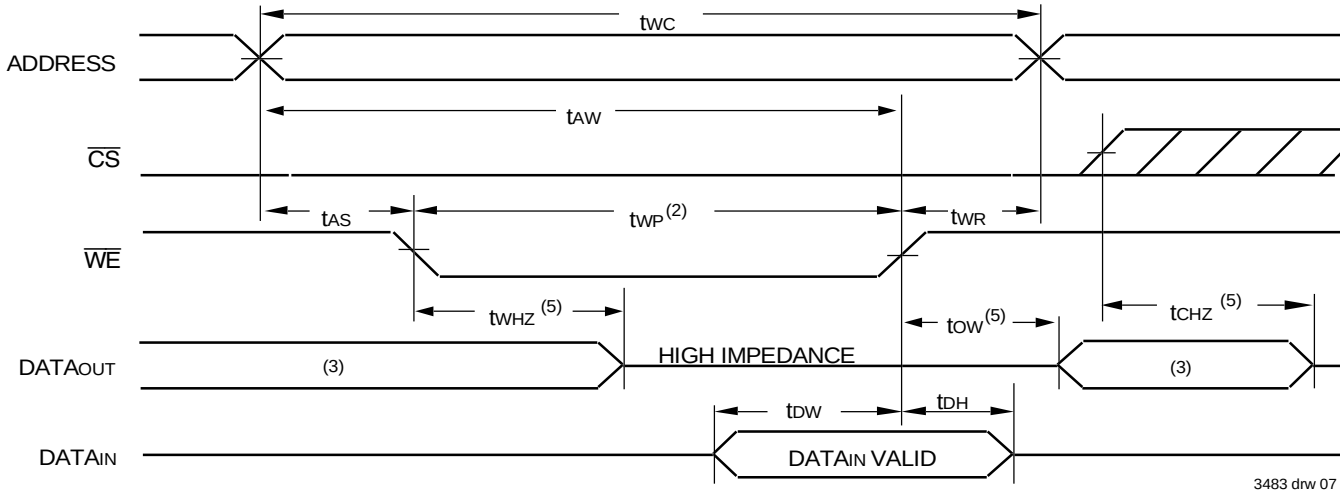



## Timing Waveform of Read Cycle No. 2(1, 2, 4)

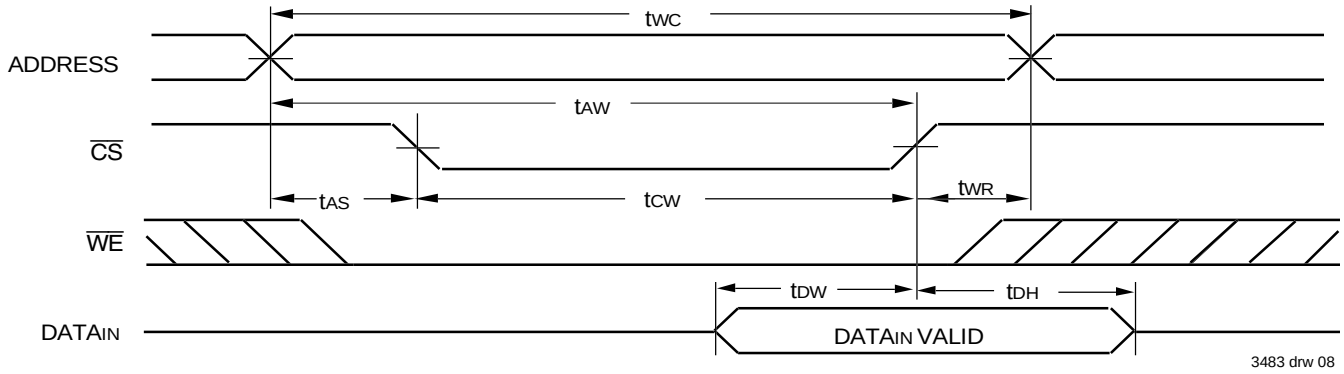



**NOTES:**
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise $t_{AA}$ is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

## Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1, 2, 4)

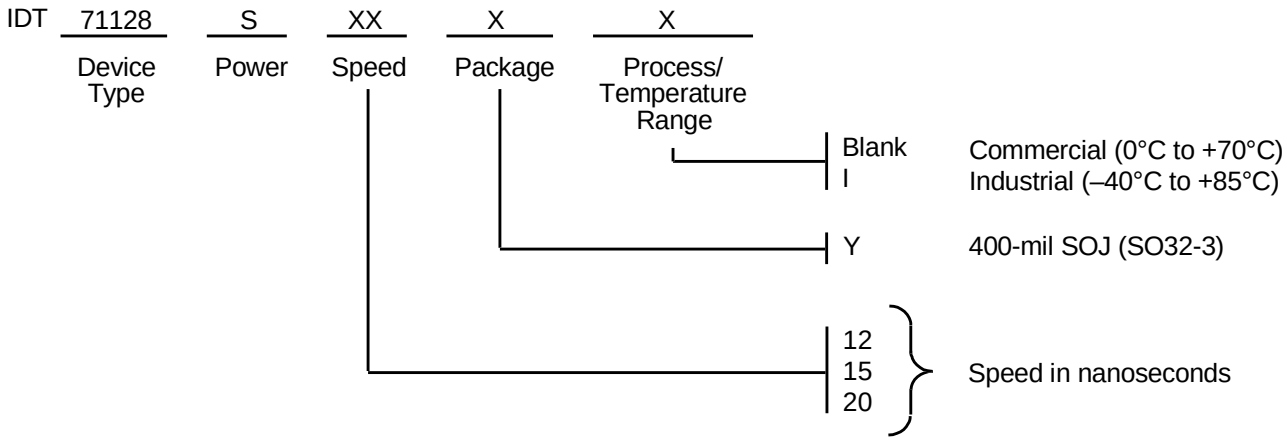



## Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1, 4)




**NOTES:**
1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, $t_{WP}$ must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified $t_{WP}$.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the $t_{CW}$ write period.
5. Transition is measured ±200mV from steady state.

# Ordering Information

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# Datasheet Document History

| | | |
|---|---|---|
| 8/5/99 | | Updated to new format |
| | Pg. 3 | Removed military entries from DC table |
| | Pg. 4 | Removed Note 1, renumbered notes and footnotes |
| | Pg. 6 | Removed Note 1, renumbered notes and footnotes |
| 8/13/99 | Pg. 8 | Added Datasheet Document History |
| 9/30/99 | Pg. 1, 3, 4, 7 | Added 12ns, 15ns, and 20ns industrial temperature speed grade offerings |
| 2/18/00 | Pg. 3 | Revise $I_{SB}$ for Industrial Temperature offerings to meet commerical specifications |
| 3/14/00 | Pg. 3 | Revised $I_{SB}$ to accomidate speed functionality |
| 8/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |

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