



# MICROCHIP 93AA46, 93LC46, 93C46 93AA46A/B, 93LC46A/B, 93C46A/B

## 1K Microwire® Serial EEPROM

### Device Selection Table

Part Number	VCC Range	Org Pin	Word Size	Temp Ranges
93AA46	1.8-5.5	Yes	8 or 16-bit	I
93LC46	2.5-5.5	Yes	8 or 16-bit	I, E
93C46	4.5-5.5	Yes	8 or 16-bit	I, E
93AA46A	1.8-5.5	No	8-bit	I
93AA46B	1.8-5.5	No	16-bit	I
93LC46A	2.5-5.5	No	8-bit	I, E
93LC46B	2.5-5.5	No	16-bit	I, E
93C46A	4.5-5.5	No	8-bit	I, E
93C46B	4.5-5.5	No	16-bit	I, E

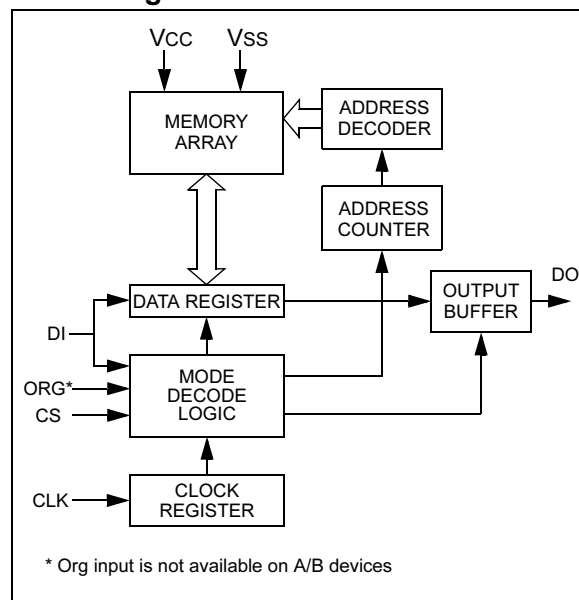
### Features

- Low power CMOS technology
- ORG pin for selectable memory configuration
- No org pin for dedicated word sizes
  - 128 x 8-bit organization 'A' version devices
  - 64 x 16-bit organization 'B' version devices
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles
- Data retention > 200 years
- 8-pin MSOP and 6-pin SOT
- Temperature ranges supported:
  - Industrial (I): -40°C to +85°C
  - Automotive (E) -40°C to +125°C

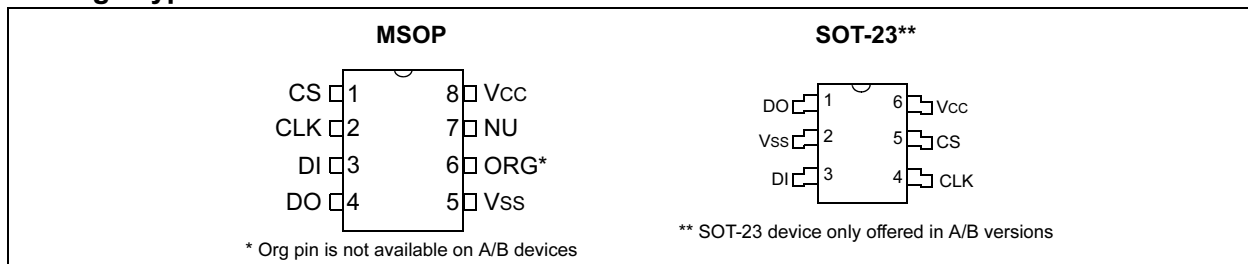
### Description

The Microchip Technology Inc. 93AA46, 93LC46, 93C46, 93AA46A/B, 93LC46A/B & 93C46A/B are 1K low voltage serial Electrically Erasable PROMs (EEPROM). Generic memory devices such as the 93AA46, 93LC46 or 93C46 are dependent upon external logic levels driving the ORG pin to set word size. For dedicated 8-bit communication, the 93AA46A, 93LC46A or 93C46A devices are selected, while the 93AA46B, 93LC46B and 93C46B devices are selected for 16 bits. Advanced CMOS technology makes these devices ideal for low power, non-volatile memory applications. This 93XX Series is available in standard 8-lead MSOP and 6-lead SOT-23 packages.

### Block Diagram



### Package Types



# 93XX46, 93XX46A/B

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

V <sub>CC</sub> .....	6.5V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.6V to V <sub>CC</sub> +1.0V
Storage temperature .....	-65°C to +150°C
Ambient temp. with power applied .....	-40°C to +125°C
ESD protection on all pins .....	≥ 4 kV

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

DC CHARACTERISTICS			V <sub>CC</sub> = +1.8V to +5.5V Industrial (I): T <sub>AMB</sub> = -40°C to +85°C Automotive (E): T <sub>AMB</sub> = -40°C to +125°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
D1	V <sub>IH1</sub>	High level input voltage	2.0	—	V <sub>CC</sub> +1	V	V <sub>CC</sub> ≥ 2.7V
	V <sub>IH2</sub>		0.7 V <sub>CC</sub>	—	V <sub>CC</sub> +1	V	V <sub>CC</sub> < 2.7V
D2	V <sub>IL1</sub>	Low level input voltage	-0.3	—	0.8	V	V <sub>CC</sub> ≥ 2.7V
	V <sub>IL2</sub>		-0.3	—	0.2 V <sub>CC</sub>	V	V <sub>CC</sub> < 2.7V
D3	V <sub>OL1</sub>	Low level output voltage	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 4.5V
	V <sub>OL2</sub>		—	—	0.3	V	I <sub>OL</sub> = 100 μA, V <sub>CC</sub> = 2.5V
D4	V <sub>OH1</sub>	High level output voltage	2.4	—	—	V	I <sub>OH</sub> = -400 μA, V <sub>CC</sub> = 4.5V
	V <sub>OH2</sub>		V <sub>CC</sub> -0.2	—	—	V	I <sub>OH</sub> = -100 μA, V <sub>CC</sub> = 2.5V
D5	I <sub>LI</sub>	Input leakage current	—	—	±10	μA	V <sub>IN</sub> = 0.1V to V <sub>CC</sub>
D6	I <sub>LO</sub>	Output leakage current	—	—	±10	μA	V <sub>OUT</sub> = 0.1V to V <sub>CC</sub>
D7	C <sub>IN</sub> , C <sub>OUT</sub>	Pin capacitance (all inputs/outputs)	—	—	7	pF	V <sub>IN</sub> /V <sub>OUT</sub> = 0V ( <b>Note 1 &amp; 2</b> ) T <sub>AMB</sub> = 25°C, F <sub>CLK</sub> = 1 MHz
D8	I <sub>CC</sub> write	Operating current	—	—	3	mA	F <sub>CLK</sub> = 2 MHz, V <sub>CC</sub> = 5.5V
D9	I <sub>CC</sub> read		—	—	1	mA	F <sub>CLK</sub> = 2 MHz, V <sub>CC</sub> = 5.5V
			—	—	500	μA	F <sub>CLK</sub> = 1 MHz, V <sub>CC</sub> = 3.0V
			—	100	—	μA	F <sub>CLK</sub> = 1 MHz, V <sub>CC</sub> = 2.5V
D10	I <sub>CCS2</sub>	Standby current	—	—	1	μA	I-Temp
			—	—	5	μA	E-Temp CLK = CS = 0V ORG = DI = V <sub>SS</sub> or V <sub>CC</sub> ( <b>Note 3</b> )

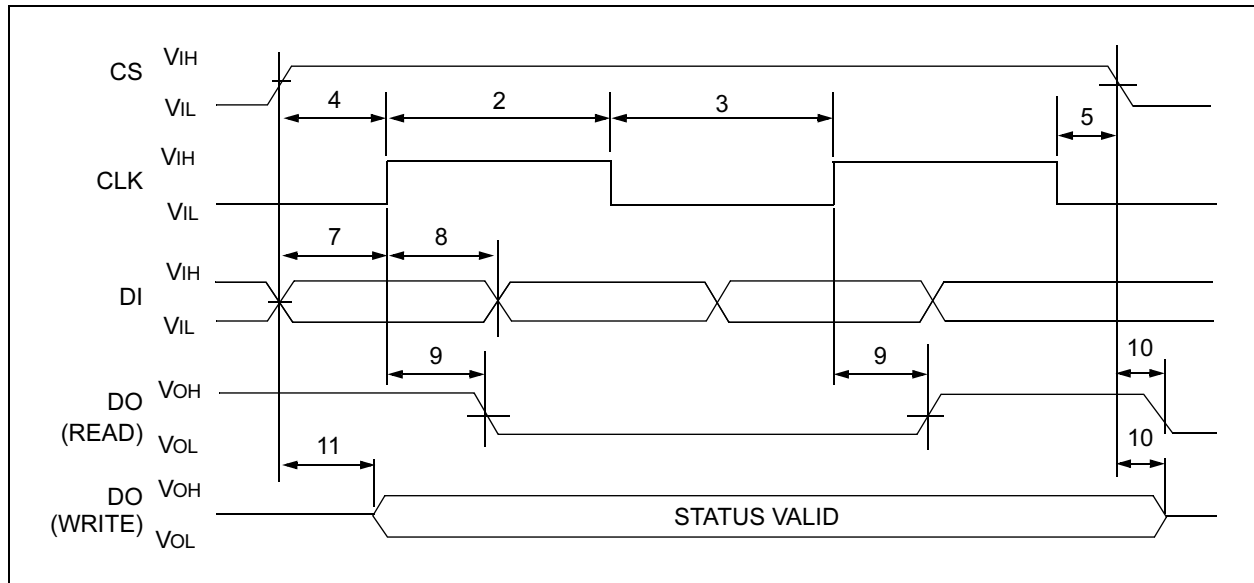
- Note 1:** This parameter is tested at T<sub>AMB</sub> = 25°C and F<sub>CLK</sub> = 1 MHz.  
**Note 2:** This parameter is periodically sampled and not 100% tested.  
**Note 3:** Org pin not available on ‘A’ or ‘B’ versions.

## AC CHARACTERISTICS

AC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TAMB = -40°C to +85°C Automotive (E): TAMB = -40°C to +125°C				
Param. No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
1	FCLK	Clock frequency	—	—	2	MHz	VCC ≥ 4.5V
			—	—	1	MHz	VCC < 4.5V
2	TCKH	Clock high time	250	—	—	ns	
3	TCKL	Clock low time	250	—	—	ns	
4	TCSS	Chip select setup time	50	—	—	ns	Relative to CLK
5	TCSH	Chip select hold time	0	—	—	ns	Relative to CLK
6	TCSL	Chip select low time	250	—	—	ns	
7	TDIS	Data input setup time	100	—	—	ns	Relative to CLK
8	TDIH	Data input hold time	100	—	—	ns	Relative to CLK
9	TPD	Data output delay time	—	—	400	ns	CL = 100 pF
10	TcZ	Data output disable time	—	—	100	ns	CL = 100 pF ( <b>Note 2</b> )
11	TSV	Status valid time	—	—	500	ns	CL = 100 pF
12	TWC	Program cycle time	—	4	10	ms	ERASE/WRITE mode
			—	1.5	2	ms	93CXX devices only
13	TEC		—	8	15	ms	ERAL mode (VCC=5V ±10%)
14	TWL		—	16	30	ms	WRAL mode (VCC=5V ±10%)
15	—	Endurance	1M	—	1M	cycles	25°C, VCC = 5.0V, ERAL/ WRAL ( <b>Note 3</b> )

- Note 1:** This parameter is tested at TAMB = 25°C and FCLK = 1 MHz.  
**Note 2:** This parameter is periodically sampled and not 100% tested.  
**Note 3:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website: [www.microchip.com](http://www.microchip.com).

**FIGURE 1-1: SYNCHRONOUS DATA TIMING**



# 93XX46, 93XX46A/B

**TABLE 1-1: INSTRUCTION SET FOR X 16 ORGANIZATION (B - VERSION DEVICES OR ORG = 1)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	9
ERAL	1	00	1 0 X X X X	—	(RDY/BSY)	9
EWDS	1	00	0 0 X X X X	—	HIGH-Z	9
EWEN	1	00	1 1 X X X X	—	HIGH-Z	9
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/BSY)	25

**TABLE 1-2: INSTRUCTION SET FOR X 8 ORGANIZATION (A - VERSION DEVICES OR ORG = 0)**

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/BSY)	10
EWDS	1	00	0 0 X X X X X	—	HIGH-Z	10
EWEN	1	00	1 1 X X X X X	—	HIGH-Z	10
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/BSY)	18

## 2.0 FUNCTIONAL DESCRIPTION

When the ORG\* pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

### 2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the Standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

### 2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

### 2.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC exceeds a typical voltage level of 1.5V for 'AA' and 'LC' devices or 3.8V for 'C' devices.

During power-down, the source data protection circuitry acts to inhibit all programming modes when VCC falls below 1.4V for 'AA' and 'LC' devices or 3.5V for 'C' devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

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\*Org pin is not available on A/B devices

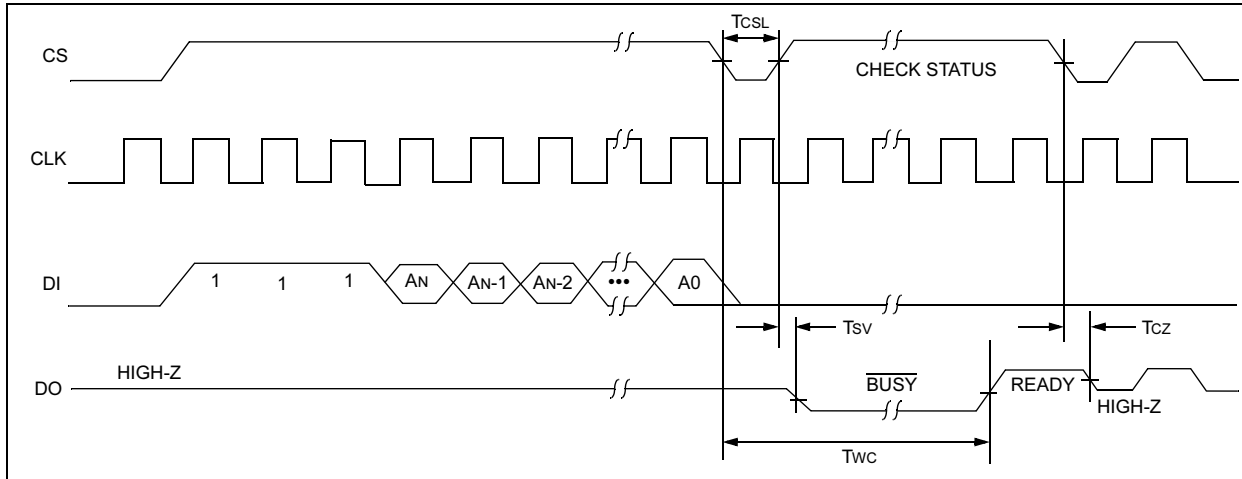
# 93XX46, 93XX46A/B

## 2.4 ERASE

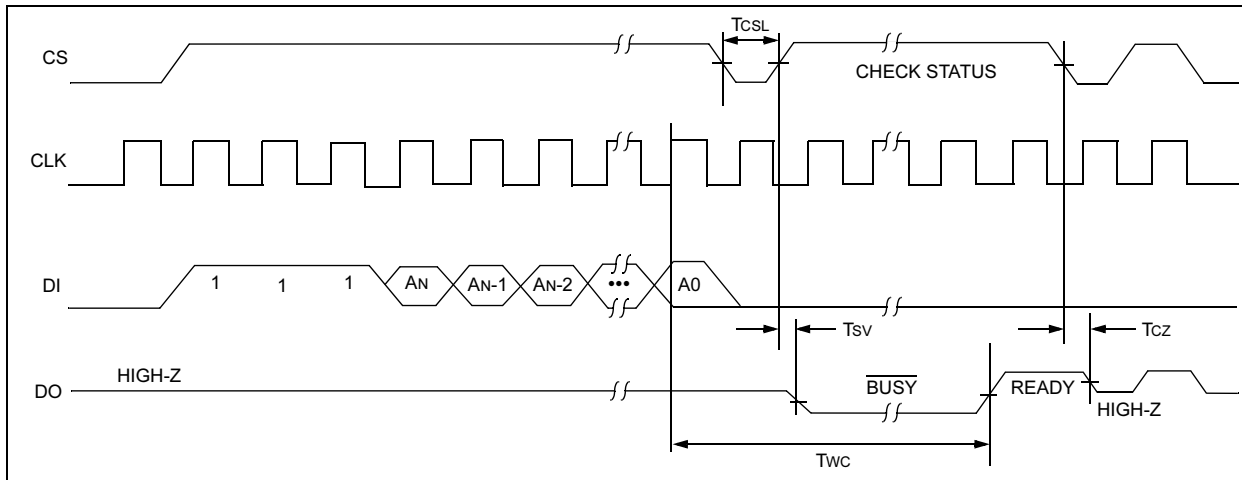
The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on 'C' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the READY/ $\overline{\text{BUSY}}$  status of the device if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

**FIGURE 2-1: ERASE TIMING FOR 93AA AND 93LC DEVICES**



**FIGURE 2-2: ERASE TIMING FOR 93C DEVICES**



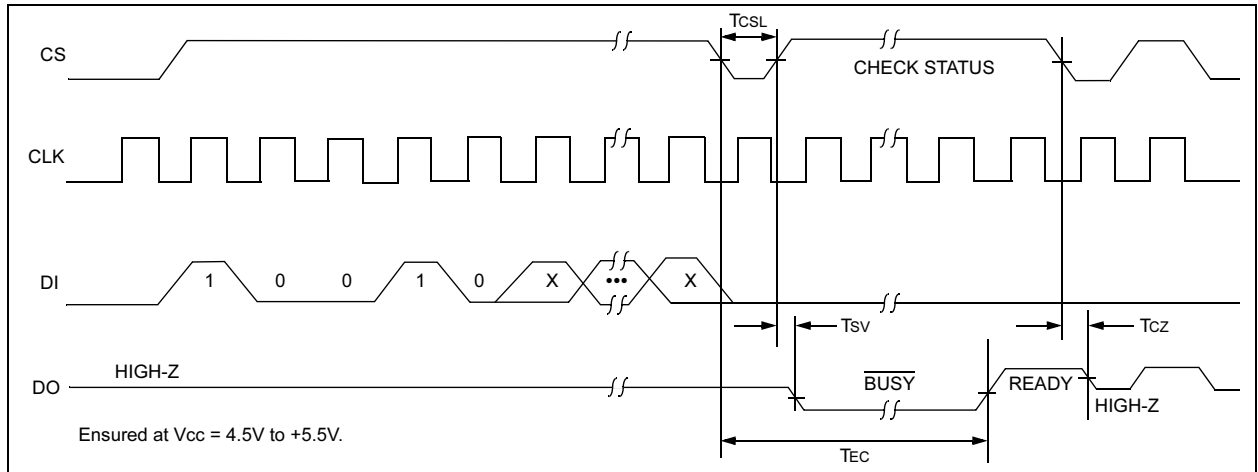
## 2.5 ERASE ALL (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on 'C' devices where the rising edge of CLK before the last

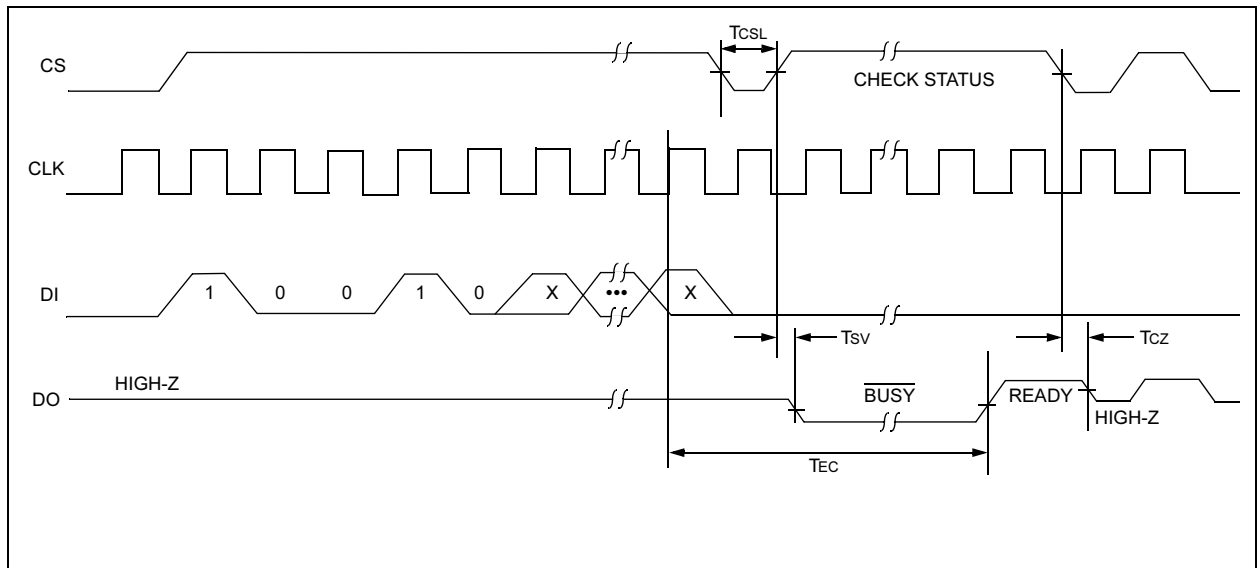
data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/ $\overline{\text{BUSY}}$  status of the device, if CS is brought high after a minimum of 250 ns low ( $T_{\text{CSL}}$ ).

**FIGURE 2-3: ERAL TIMING FOR 93AA AND 93LC DEVICES**



**FIGURE 2-4: ERAL TIMING FOR 93C DEVICES**



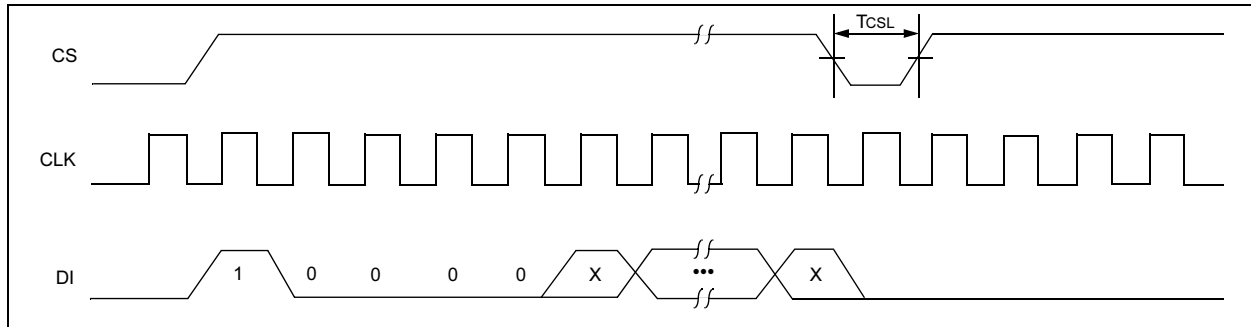
# 93XX46, 93XX46A/B

## 2.6 ERASE/WRITE DISABLE AND ENABLE (EWDS/EWEN)

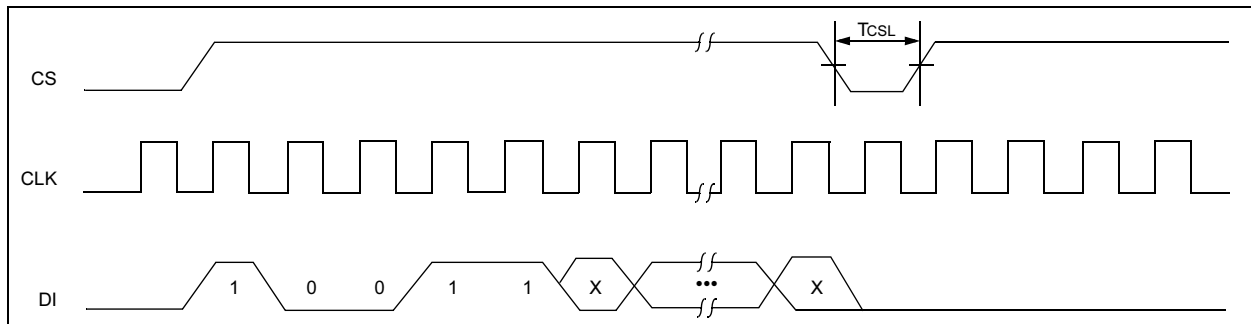
The 93XX46, 93XX46A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the

device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

**FIGURE 2-5: EWDS TIMING**



**FIGURE 2-6: EWEN TIMING**

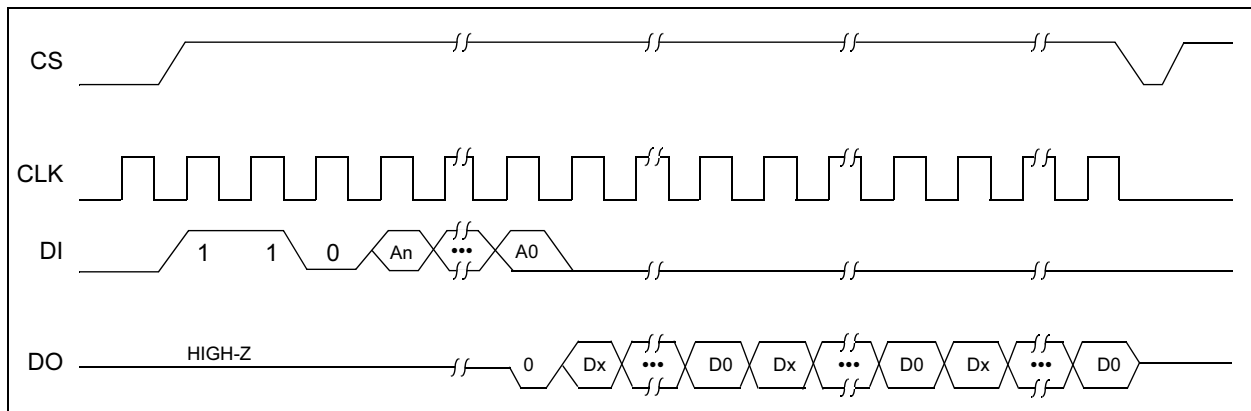


## 2.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-Version devices) or 16-bit (If ORG pin is high or B-version devices) output string. The output data bits will toggle

on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

**FIGURE 2-7: READ TIMING**



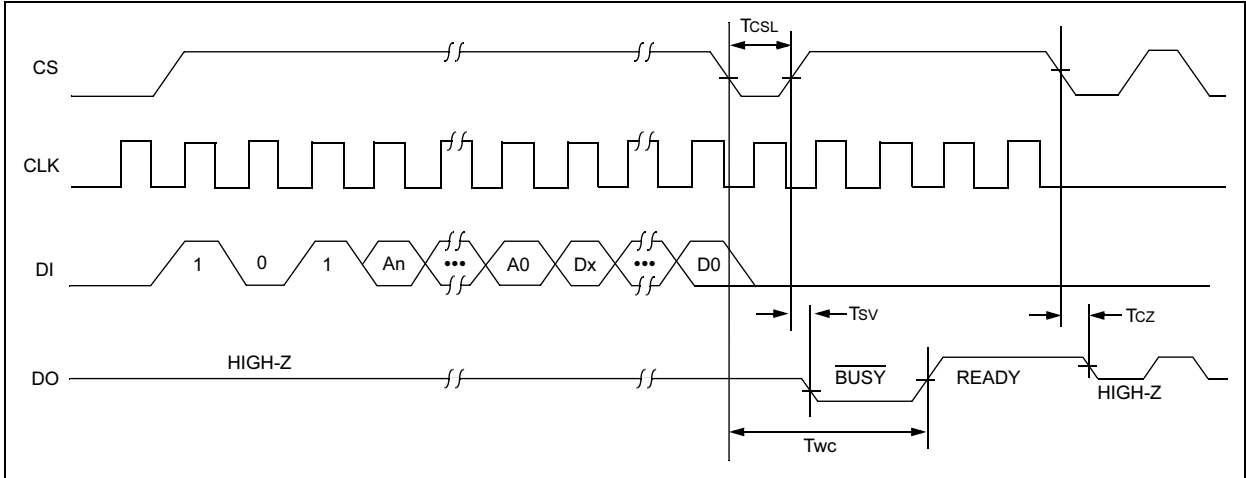


## 2.8 WRITE

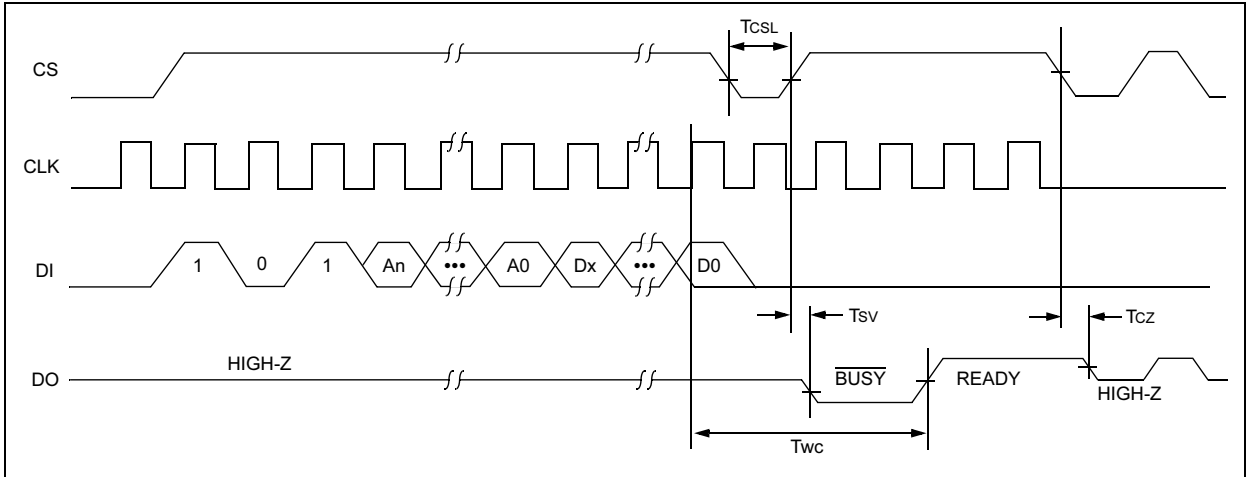
The WRITE instruction is followed by 8 bits (If ORG is low or A-version parts) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle, except on 'C' devices where the rising edge of CLK before the last data bit initiates the write cycle.

The DO pin indicates the READY/BUSY status of the device, if CS is brought high after a minimum of 250 ns low ( $T_{CSL}$ ). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

**FIGURE 2-8: WRITE TIMING FOR 93AA AND 93LC DEVICES**



**FIGURE 2-9: WRITE TIMING FOR 93C DEVICES**



# 93XX46, 93XX46A/B

## 2.9 WRITE ALL (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS, except on 'C' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an

automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/BUSY status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 2-10: WRAL TIMING FOR 93AA AND 93LC DEVICES

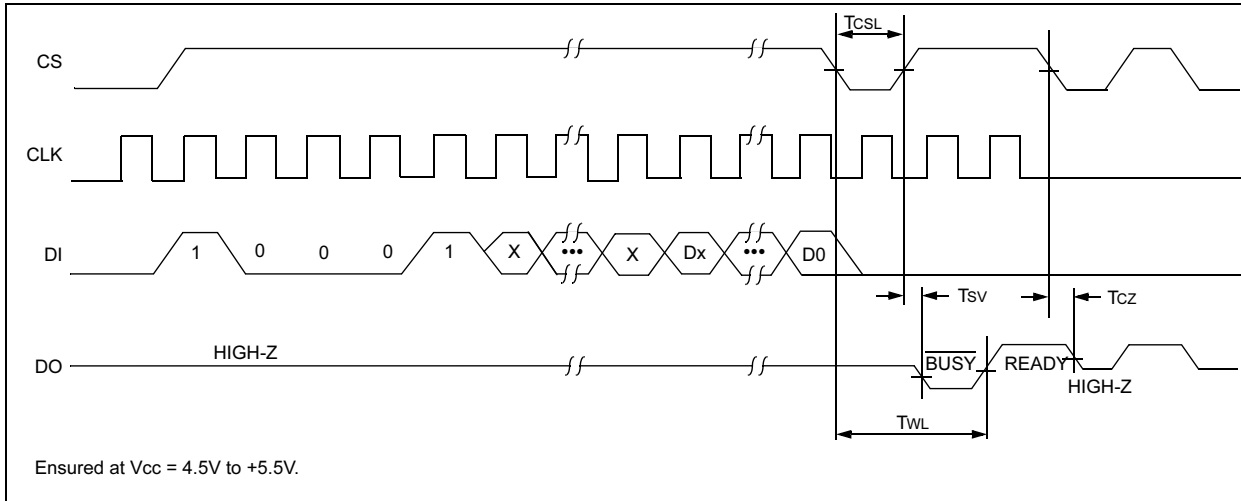
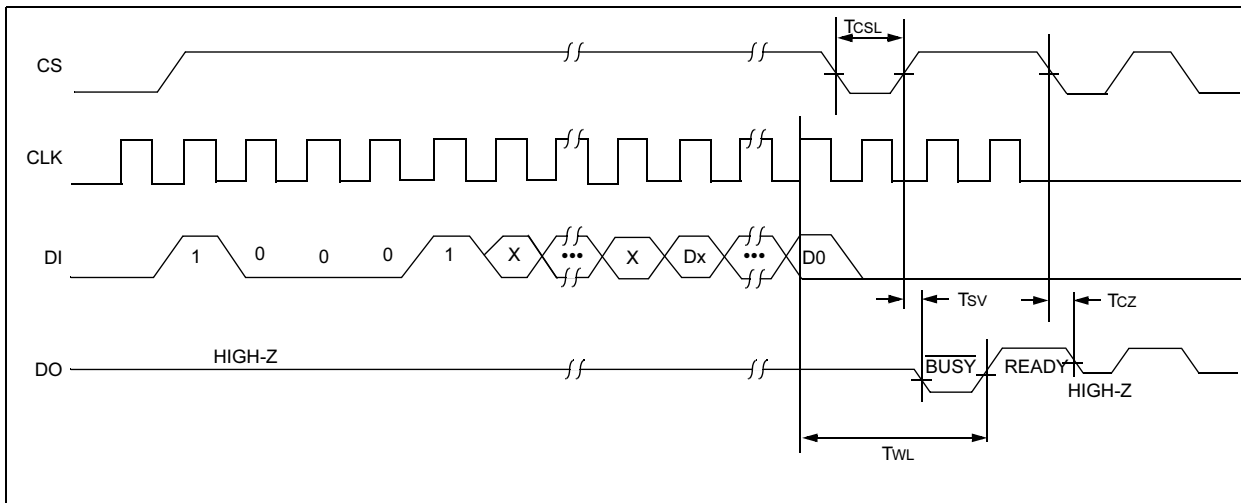


FIGURE 2-11: WRAL TIMING FOR 93C DEVICES



## 3.0 PIN DESCRIPTIONS

**FIGURE 3-1: PIN DESCRIPTIONS**

Name	MSOP	6-LEAD SOT-23	Function
CS	1	5	Chip Select
CLK	2	4	Serial Clock
DI	3	3	Data In
DO	4	1	Data Out
V <sub>ss</sub>	5	2	Ground
ORG/NC	6	N/A	Organization / No Connect (No internal connection for 93XX46A/B)
NC	7	N/A	No Connect (No Internal Connection)
V <sub>cc</sub>	8	6	Power Supply

### 3.1 CHIP SELECT (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T<sub>CsL</sub>) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

Input filter spike suppression was added to reduce susceptibility to noise.

### 3.2 SERIAL CLOCK (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T<sub>CKH</sub>) and clock low time (T<sub>CKL</sub>). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but the START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and

data bits before an instruction is executed. CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Input filter spike suppression was added to reduce susceptibility to noise.

### 3.3 DATA IN (DI)

Data In (DI) is used to clock in a START bit, opcode, address and data synchronously with the CLK input.

Input filter spike suppression was added to reduce susceptibility to noise.

### 3.4 DATA OUT (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (T<sub>PD</sub> after the positive edge of CLK).

This pin also provides READY/ $\overline{\text{BUSY}}$  status information during ERASE and WRITE cycles. READY/ $\overline{\text{BUSY}}$  status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (T<sub>CsL</sub>) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

### 3.5 ORGANIZATION (ORG)\*

When the ORG pin is connected to V<sub>cc</sub> or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to V<sub>ss</sub> or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

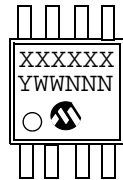
On the dedicated 'A' and 'B' devices the user selectable ORG function is not present. (No internal connection.)

# 93XX46, 93XX46A/B

## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

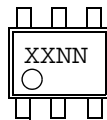
8-Lead MSOP (150 mil)



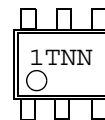
Example:



6-Lead SOT-23



Example:

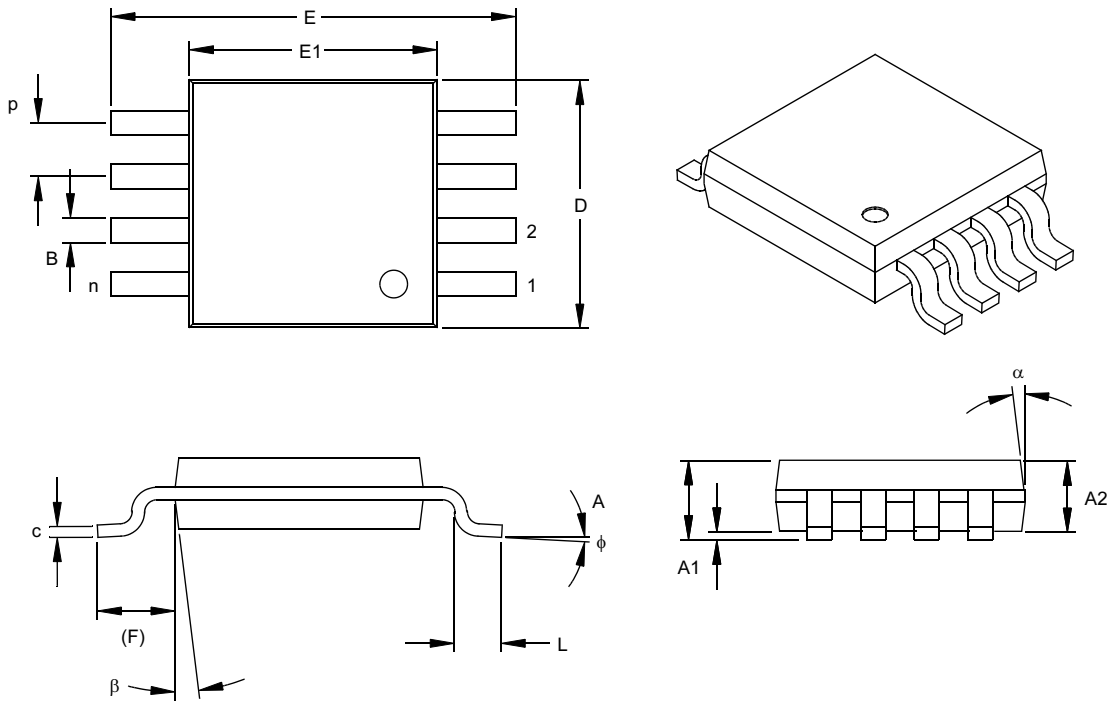


<b>Legend:</b>	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

\* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

# 93XX46, 93XX46A/B

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

\*Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

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NOTES:

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Device: 93XX46, 93XX46A/B Literature Number: DS21749A

Questions:

1. What are the best features of this document?

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<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>XX</u>
Device	Pinout	Tape & Reel	Temperature Range	Package
Device:	93AA46: 1K 1.8V Microwire Serial EEPROM 93AA46A: 1K 1.8V Microwire Serial EEPROM 93AA46B: 1K 1.8V Microwire Serial EEPROM			
	93LC46: 1K 2.5V Microwire Serial EEPROM 93LC46A: 1K 2.5V Microwire Serial EEPROM 93LC46B: 1K 2.5V Microwire Serial EEPROM			
	93C46: 1K 5.0V Microwire Serial EEPROM 93C46A: 1K 5.0V Microwire Serial EEPROM 93C46B: 1K 5.0V Microwire Serial EEPROM			
Pinout:	Blank= Standard pinout			
Tape & Reel:	Blank= Standard packaging T = Tape & Reel			
Temperature Range:	I = -40°C to +85°C E = -40°C to +125°C			
Package:	MS = Plastic MSOP (Micro Small outline, 8-lead) OT = SOT-23, 6-lead (Tape and Reel only)			

**Examples:**

a) 93AA46-I/MS: 1K, 128x8 or 64x16 Serial EEPROM, MSOP package

b) 93AA46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package

c) 93AA46AT-I/OT: 1K, 128x8 Serial EEPROM, SOT-23 package, tape and reel

d) 93AA46T-I/MS: 1K, 128x8 or 64x16 Serial EEPROM, MSOP package, tape and reel

a) 93LC46A-I/MS: 1K, 128x8 Serial EEPROM, MSOP package

b) 93LC46BT-I/OT: 1K, 64x16 Serial EEPROM, SOT-23 package, tape and reel

c) 93LC46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package

a) 93C46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package

b) 93C46-I/MS: 1K, 128x8 or 64x16 Serial EEPROM, MSOP package

c) 93C46AT-I/OT: 1K, 128x8 Serial EEPROM, SOT-23 package, tape and reel

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NOTES:

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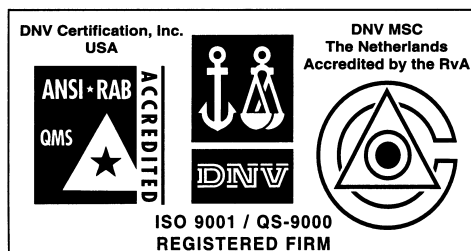
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