

MM74C73 • MM74C76 Dual J-K Flip-Flops with Clear and Preset

General Description

The MM74C73 and MM74C76 dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and \bar{Q} outputs. The MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. This flip-flop is edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Features

- Supply voltage range: 3V to 15V
- Tenth power TTL compatible: Drive 2 LPTTL loads
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power: 50 nW (typ.)
- Medium speed operation: 10 MHz (typ.)

Applications

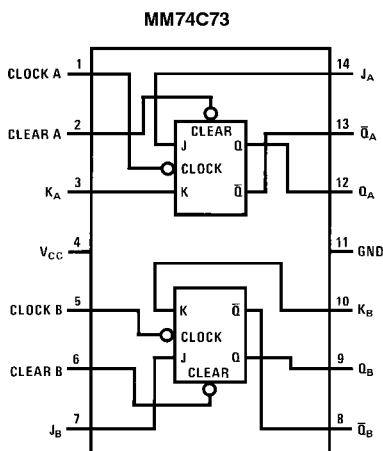
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Ordering Code:

Order Number	Package Number	Package Description
MM74C73N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C76M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74C76N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

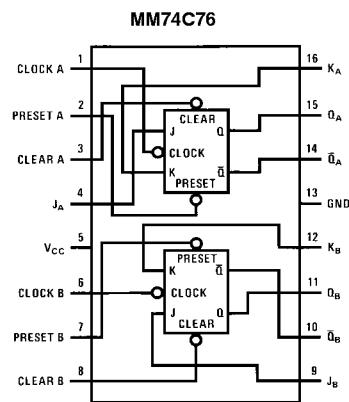
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams



Note: A logic "0" on clear sets Q to logic "0".

Top View



Note: A logic "0" on clear sets Q to a logic "0".

Note: A logic "0" on preset sets Q to a logic "1".

Top View

Truth Tables

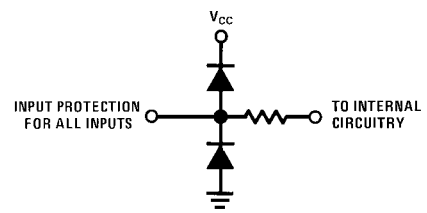
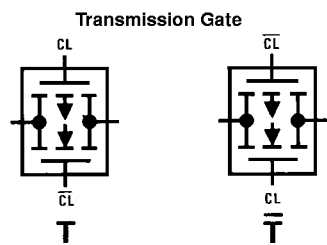
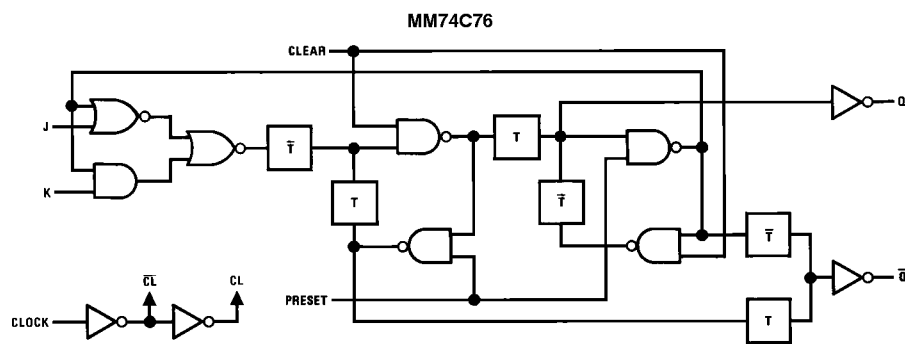
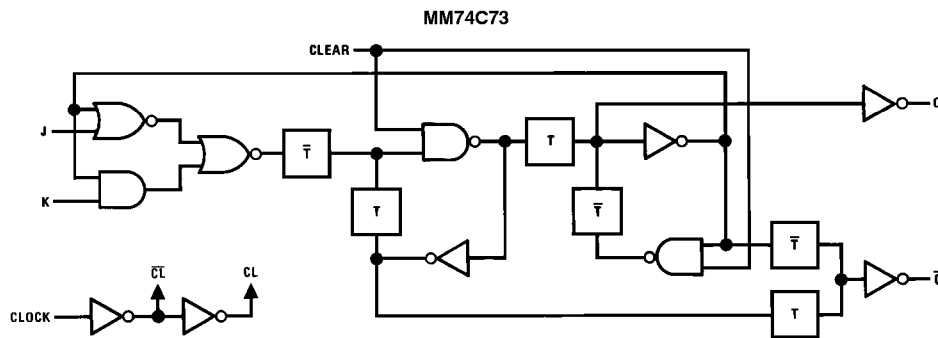
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

t_n = bit time before clock pulse
 t_{n+1} = bit time after clock pulse

Preset	Clear	Q_n	\bar{Q}_n
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q_n (Note 1)	\bar{Q}_n (Note 1)

Note 1: No change in output from previous state

Logic Diagrams



Absolute Maximum Ratings(Note 2)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature	
(Soldering, 10 seconds)	260°C
Operating V_{CC} Range	+3V to 15V
V_{CC} (Max)	18V

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

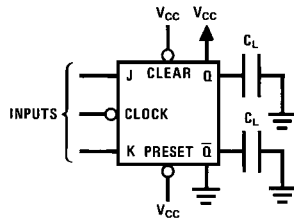
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$	4.5			V
		$V_{CC} = 10V$	9			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$			0.5	V
		$V_{CC} = 10V$			1	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$			1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1			μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.050	60	μA
LOW POWER TTL TO CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	8			mA

AC Electrical Characteristics (Note 3) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise noted

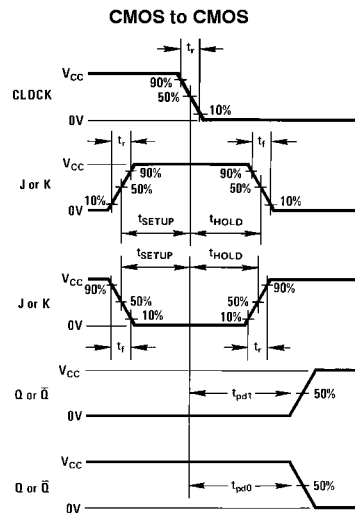
Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	Any Input		5		pF
t_{pd0} , t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or \bar{Q}	$V_{CC} = 5V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$		110 45	175 70	ns ns
t_H	Time after Clock Pulse that J and K must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$		-40 -20	0 0	ns ns
t_{PW}	Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5V$ $V_{CC} = 10V$		120 50	190 80	ns ns
t_{PW}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		90 40	130 60	ns ns
t_{MAX}	Maximum Toggle Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.5 7	4 11		MHz MHz
t_r , t_f	Clock Pulse Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$			15 5	μs μs

Note 3: AC Parameters are guaranteed by DC correlated testing.

AC Test Circuit



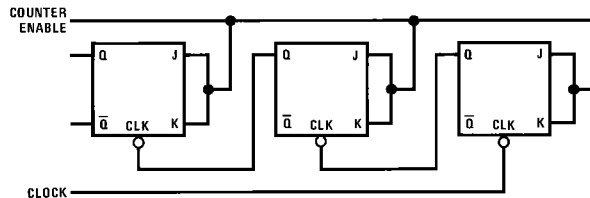
Switching Time Waveforms



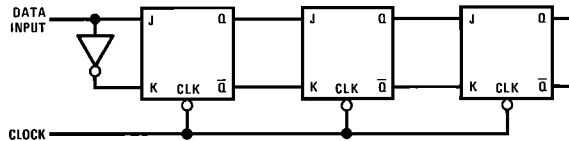
$t_r = t_f = 20 \text{ ns}$

Typical Applications

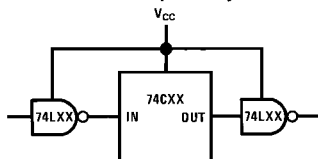
Ripple Binary Counters



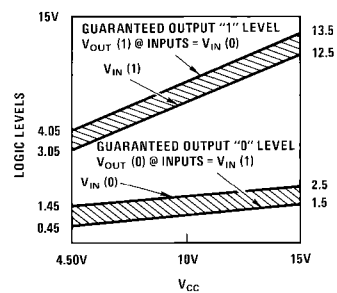
Shift Registers



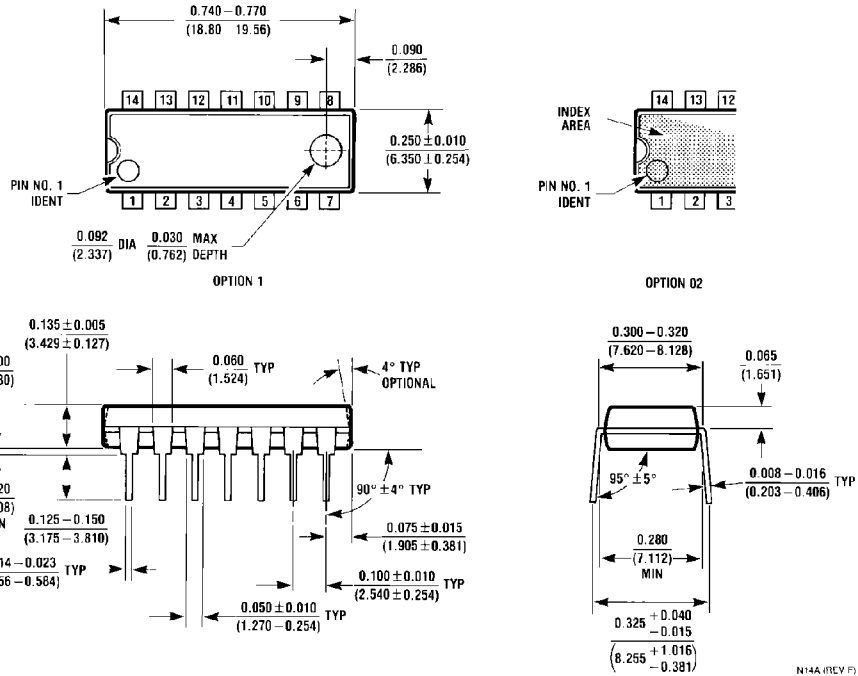
74C Compatibility



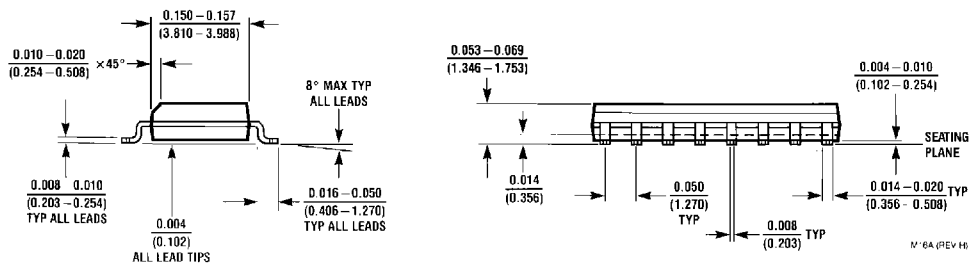
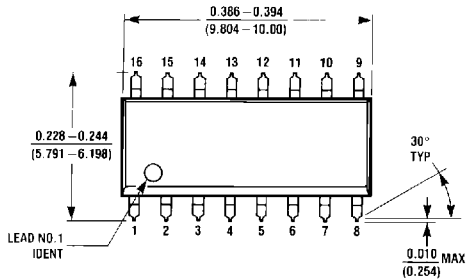
Guaranteed Noise Margin as a Function of V_{CC}



Physical Dimensions inches (millimeters) unless otherwise noted

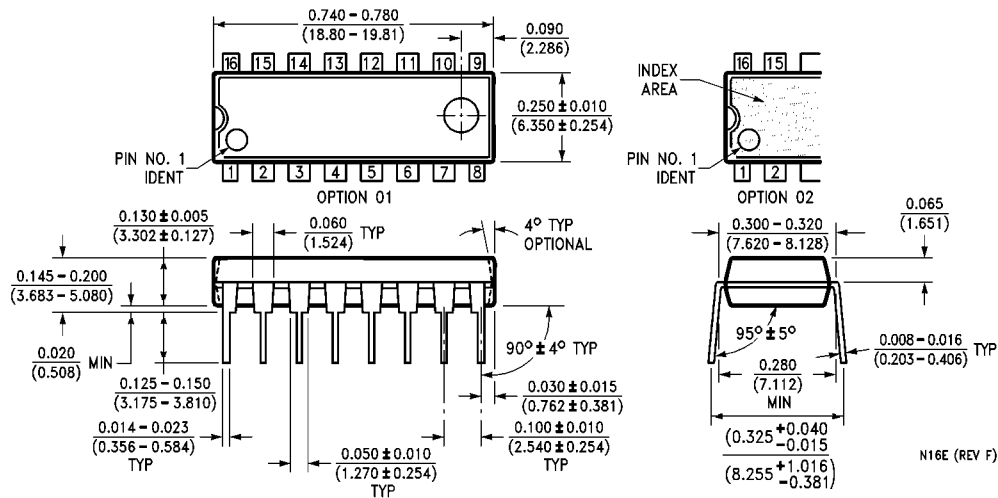


14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com