

**世界先進積體電路股份有限公司**  
**Vanguard International Semiconductor Corp.**

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| SECURITY C<br>VIS-INTERNAL |
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| Rev   | Date       | ECN      | From  | Description  |
|---|------------|----------|---|--|
| 1   | 12/06/2000 | 1G5-0179 | 黃志凱   | Original   |
| 2   | 06/01/2001 | 901190   | 曾毓琳   | VA6087 1Mx16 EDO 3.3V yield 太低, 原因為Icc6 ( self-refresh current ) kill yield, 在考量客戶需求及產品良率之後, 決定放鬆Icc6規格                      |
| 3   | 10/19/2001 | 902563   | 曾毓琳   | 1.刪除VG26(V)(S)18165D字樣<br>2.文件名稱改為VA6087 1M*16 EDO DRAM Product Spec.  |
| 4   | 12/19/2002 | 20022298 | 曾毓琳   | 3.Ordering information 新增TSOP II欄位<br>1.Page 5 Vcc=+3.15V~3.6V<br>2.Page 6 Icc6 -6 600uA Icc4 80 &130mA Page 7 Icc6 -6 550uA |
| Originator : <b>黃志凱</b><br>Origination Dept. Manager: 1313 <b>陳瑛政</b> |            |          | Title<br><br><p style="text-align: center;">VA6087 1M*16 EDO DRAM Product Spec.</p> |  |
| Signature on file in DMS  |            |          | Doc. No.:1G5-0179   |  |
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**PLEASE RETURN OLD VERSION SPEC TO DCC**

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## Description

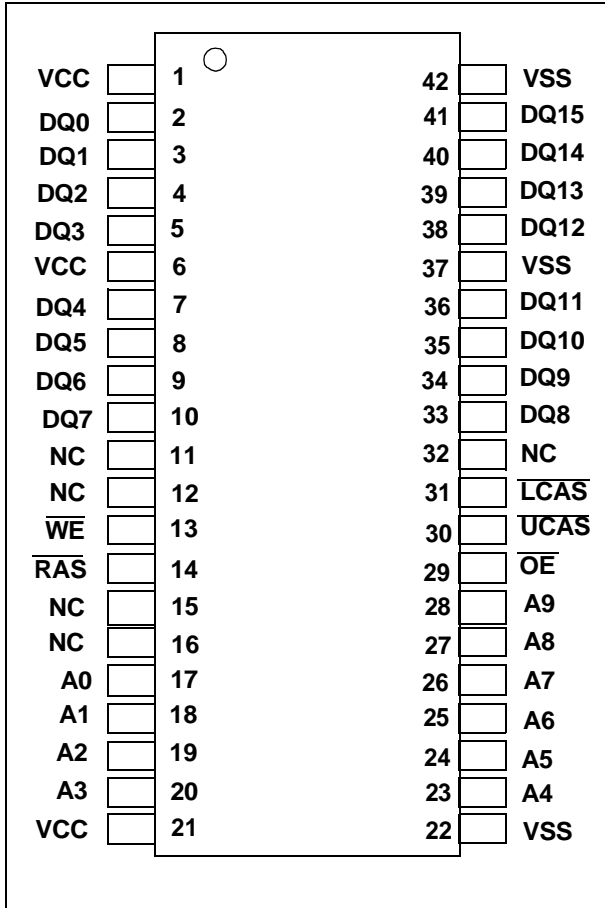
The device CMOS Dynamic RAM organized as 1,048,576 words x 16 bits with extended data out access mode. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. Self-refresh is supported and CBR cycles are being performed. It is packaged in JEDEC standard 42-pin 400mil SOJ and 50(44)-pin 400mil TSOPII.

## Features

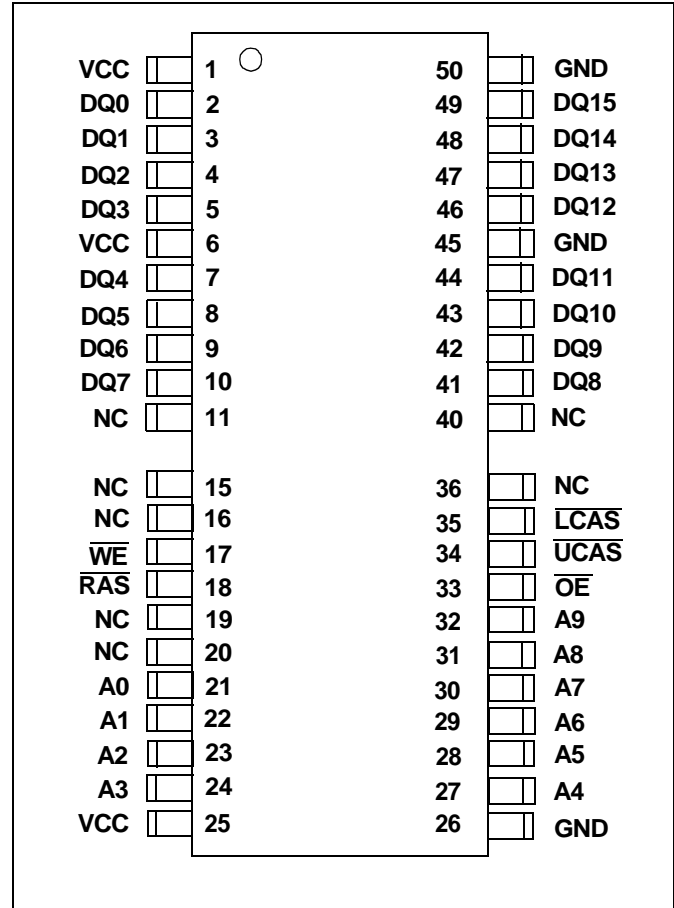
- Single 5V or 3.3V only power supply
- High speed  $t_{RAC}$  access time: 50/60ns
- Extended-data-out (EDO) page mode access
- I/O level: TTL compatible ( $V_{CC} = 5V$ )  
LVTTTL compatible ( $V_{CC} = 3.3V$ )
- 4 refresh modes:
  - $\overline{RAS}$  only refresh
  - $\overline{CAS}$  - before -  $\overline{RAS}$  refresh
  - Hidden refresh
  - Self-refresh
- Refresh interval:
  - $\overline{RAS}$  only refresh,  $\overline{CAS}$  - before -  $\overline{RAS}$  refresh and hidden refresh: 1024 cycles in 16 ms
  - Self-refresh: 1024 cycles
- JEDEC standard pinout: 44-pin 400mil SOJ and 50(44)-pin 400mil TSOPII

### Pin Configuration

42-Pin 400mil SOJ



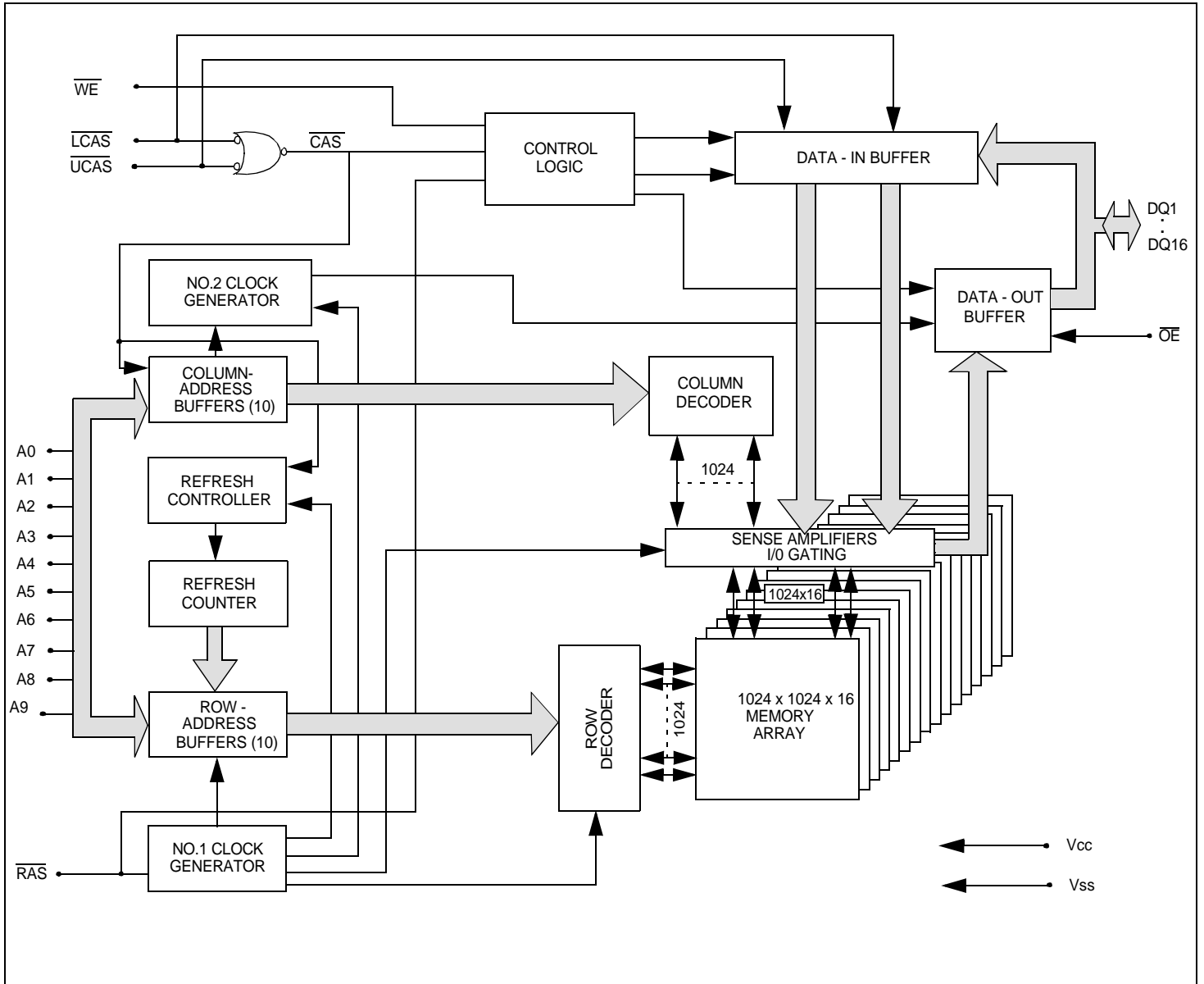
50(44)-Pin 400mil TSOPII



### Pin Description

| Pin Name  | Function  |
|---|---|
| A0-A9   | Address inputs<br>- Row address: A0-A9<br>- Column address: A0-A9<br>- Refresh address: A0-A9 |
| DQ0-DQ15  | Data-in / data-out  |
| $\overline{\text{RAS}}$                             | Row address strobe  |
| $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ | Column address strobe   |
| $\overline{\text{WE}}$                              | Write enable  |
| $\overline{\text{OE}}$                              | Output enable   |
| Vcc   | Power (+5 V or + 3.3V)  |
| Vss   | Ground  |
| NC  | No connection   |

## Block Diagram



**TRUTH TABLE**

| FUNCTION                              |           | $\overline{\text{RAS}}$ | $\overline{\text{LCAS}}$ | $\overline{\text{UCAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | ADDRESSES |     | DQ <sub>S</sub>                            | Notes |
|---------------------------------------|-----------|-------------------------|--------------------------|--------------------------|------------------------|------------------------|-----------|-----|--|-------|
|                                       |           |                         |                          |                          |                        |                        | ROW       | COL |  |       |
| STANDBY                               |           | H                       | H → X                    | H → X                    | X                      | X                      | X         | X   | High-Z                                     |       |
| READ : WORD                           |           | L                       | L                        | L                        | H                      | L                      | ROW       | COL | Data-Out                                   |       |
| READ : LOWER BYTE                     |           | L                       | L                        | H                        | H                      | L                      | ROW       | COL | Lower Byte: Data-Out<br>Upper Byte: High-Z |       |
| READ: UPPER BYTE                      |           | L                       | H                        | L                        | H                      | L                      | ROW       | COL | Lower Byte: High-Z<br>Upper Byte: Data-Out |       |
| WRITE: WORD<br>(EARLY WRITE)          |           | L                       | L                        | L                        | L                      | X                      | ROW       | COL | Data-In                                    |       |
| WRITE: LOWER<br>BYTE (EARLY)          |           | L                       | L                        | H                        | L                      | X                      | ROW       | COL | Lower Byte: Data-In<br>Upper Byte: High-Z  |       |
| WRITE : UPPER<br>BYTE (EARLY)         |           | L                       | H                        | L                        | L                      | X                      | ROW       | COL | Lower Byte: High-Z<br>Upper Byte: Data-In  |       |
| READ WRITE                            |           | L                       | L                        | L                        | H → L                  | L → H                  | ROW       | COL | Data-Out, Data-In                          | 1,2   |
| PAGE-MODE<br>READ                     | 1st Cycle | L                       | H → L                    | H → L                    | H                      | L                      | ROW       | COL | Data-Out                                   | 2     |
|                                       | 2nd Cycle | L                       | H → L                    | H → L                    | H                      | L                      | n/a       | COL | Data-Out                                   | 2     |
| PAGE-MODE<br>WRITE                    | 1st Cycle | L                       | H → L                    | H → L                    | L                      | X                      | ROW       | COL | Data-In                                    | 1     |
|                                       | 2nd Cycle | L                       | H → L                    | H → L                    | L                      | X                      | n/a       | COL | Data-In                                    | 1     |
| PAGE-MODE<br>READ-<br>WRITE           | 1st Cycle | L                       | H → L                    | H → L                    | H → L                  | L → H                  | ROW       | COL | Data-Out, Data-In                          | 1,2   |
|                                       | 2nd Cycle | L                       | H → L                    | H → L                    | H → L                  | L → H                  | n/a       | COL | Data-Out, Data-In                          | 1,2   |
| HIDDEN<br>REFRESH                     | READ      | L → H → L               | L                        | L                        | H                      | L                      | ROW       | COL | Data-Out                                   | 2     |
|                                       | WRITE     | L → H → L               | L                        | L                        | L                      | X                      | ROW       | COL | Data-In                                    | 1,3   |
| $\overline{\text{RAS}}$ -ONLY REFRESH |           | L                       | H                        | H                        | X                      | X                      | ROW       | n/a | High-Z                                     |       |
| CBR REFRESH                           |           | H → L                   | L                        | L                        | H                      | X                      | X         | X   | High-Z                                     | 4     |

Notes: 1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).

2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).

3. EARLY WRITE only.

4. At least one of the two  $\overline{\text{CAS}}$  signals must be active ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ).

**Absolute Maximum Ratings**

| Parameter                             | Symbol     | Value        | Unit          |   |
|---------------------------------------|------------|--------------|---------------|---|
| Voltage on an any pin relative to Vss | 5V<br>3.3V | $V_T$        | -1.0 to + 7.0 | V |
|                                       |            |              | -0.5 to + 4.6 |   |
| Supply voltage relative to Vss        | 5V<br>3.3V | $V_{CC}$     | -1.0 to + 7.0 | V |
|                                       |            |              | -0.5 to + 4.6 |   |
| Short circuit output current          | $I_{OUT}$  | 50           | mA            |   |
| Power dissipation                     | $P_D$      | 1.0          | W             |   |
| Operating temperature                 | $T_{OPT}$  | 0 to + 70    | °C            |   |
| Storage temperature                   | $T_{STG}$  | -55 to + 125 | °C            |   |

**Recommended DC Operating Conditions**

| Parameter/Condition            | Sym-<br>bol | 5 Volt Version |     |                | 3.3 Volt Version |     |                | Unit |
|--------------------------------|-------------|----------------|-----|----------------|------------------|-----|----------------|------|
|                                |             | Min            | Typ | Max            | Min              | Typ | Max            |      |
| Supply Voltage                 | $V_{CC}$    | 4.5            | 5.0 | 5.5            | 3.15             | 3.3 | 3.6            | V    |
| Input High Voltage, all inputs | $V_{IH}$    | 2.4            | -   | $V_{CC} + 1.0$ | 2.0              | -   | $V_{CC} + 0.3$ | V    |
| Input Low Voltage, all inputs  | $V_{IL}$    | -1.0           | -   | 0.8            | -0.3             | -   | 0.8            | V    |

**Capacitance**

Ta = 25°C, V<sub>CC</sub> = 5V ±10 % or V<sub>CC</sub> = + 3.15V~3.6V, f = 1MHz

| Parameter  | Symbol    | Max | Unit | Note |
|--|-----------|-----|------|------|
| Input capacitance (Address)  | $C_{I1}$  | 5   | pF   | 1    |
| Input capacitance ( $\overline{RAS}$ , $\overline{LCAS}$ , $\overline{UCAS}$ , $\overline{OE}$ , $\overline{WE}$ ) | $C_{I2}$  | 7   | pF   | 1    |
| Output capacitance (Data-in, Data-out)   | $C_{I/O}$ | 7   | pF   | 1, 2 |

Note: 1. Capacitance measured with effective capacitance measuring method.  
 2. RAS, LCAS and UCAS = V<sub>IH</sub> to disable Dout.

**DC Characteristics; 5- Volt Verion ( $T_a = 0$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ )**

| Parameter                      | Symbol    | Test Conditions   | VG26(S)18165 |     |     |     | Unit    | Notes |
|--------------------------------|-----------|---|--------------|-----|-----|-----|---------|-------|
|                                |           |   | -5           |     | -6  |     |         |       |
|                                |           |   | Min          | Max | Min | Max |         |       |
| Operating current              | $I_{CC1}$ | $\overline{\text{RAS}}$ cycling<br>LCAS / UCAS cycling<br>$t_{RC} = \text{min}$     | -            | 160 | -   | 145 | mA      | 1, 2  |
| Standby current                | $I_{CC2}$ | TTL interface<br>RAS, LCAS / UCAS = $V_{IH}$<br>Dout = High-Z                       |              | 2   | -   | 2   | mA      |       |
|                                |           | CMOS interface<br>RAS, $\overline{\text{CAS}} \geq V_{CC} - 0.2V$<br>Dout = High-Z  |              | 1   | -   | 1   | mA      |       |
| RAS-only refresh current       | $I_{CC3}$ | $\overline{\text{RAS}}$ cycling,<br>LCAS / UCAS = $V_{IH}$<br>$t_{RC} = \text{min}$ | -            | 160 | -   | 145 | mA      | 1, 2  |
| EDO page mode current          | $I_{CC4}$ | $t_{RC} = \text{min}$   | -            | 80  | -   | 130 | mA      | 1, 3  |
| CAS-before-RAS refresh current | $I_{CC5}$ | $t_{RC} = \text{min}$<br>RAS, LCAS / UCAS cycling                                   | -            | 160 | -   | 145 | mA      | 1, 2  |
| Self-refresh current           | $I_{CC6}$ | $t_{RAS} \geq 100\mu s$   | -            | 500 | -   | 600 | $\mu A$ |       |
| Input leakage current          | $I_{LI}$  | $0V \leq V_{IN} \leq V_{CC} + 0.5V$   | -5           | 5   | -5  | 5   | $\mu A$ |       |
| Output leakage current         | $I_{LO}$  | $0V \leq V_{OUT} \leq V_{CC} + 0.5V$<br>Dout = Disable                              | -5           | 5   | -5  | 5   | $\mu A$ |       |
| Output high Voltage            | $V_{OH}$  | $I_{OH} = -5mA$   | 2.4          | -   | 2.4 | -   | V       |       |
| Output low voltage             | $V_{OL}$  | $I_{OL} = +4.2mA$   | -            | 0.4 | -   | 0.4 | V       |       |

Notes:

1.  $I_{CC}$  is specified as an average current. It depends on output loading condition and cycle rate when the device is selected.  $I_{CC}$  max is specified at the output open condition.
2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .
3. For  $I_{CC4}$ , address can be changed once or less within one EDO page mode cycle time.

**DC Characteristics ; 3.3 - Volt Version ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = + 3.15\text{V}\sim 3.6\text{V}$ ,  $V_{SS} = 0\text{V}$ )**

| Parameter   | Symbol    | Test Conditions   | VG26V(S)18165 |     |     |     | Unit          | Notes |
|---|-----------|---|---------------|-----|-----|-----|---------------|-------|
|   |           |   | -5            |     | -6  |     |               |       |
|   |           |   | Min           | Max | Min | Max |               |       |
| Operating current   | $I_{CC1}$ | $\overline{\text{RAS}}$ cycling<br>LCAS / UCAS cycling<br>$t_{RC} = \text{min}$                             | -             | 160 | -   | 145 | mA            | 1, 2  |
| Standby Current   | $I_{CC2}$ | LVTTL interface<br>RAS, LCAS / UCAS = $V_{IH}$<br>Dout = High-Z   | -             | 2   | -   | 2   | mA            |       |
|   |           | CMOS interface<br>$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$<br>Dout = High-Z | -             | 0.5 | -   | 0.5 | mA            |       |
| $\overline{\text{RAS}}$ - only refresh current                            | $I_{CC3}$ | $\overline{\text{RAS}}$ cycling<br>LCAS / UCAS = $V_{IH}$<br>$t_{RC} = \text{min}$                          | -             | 160 | -   | 145 | mA            | 1, 2  |
| EDO page mode current   | $I_{CC4}$ | $t_{PC} = \text{min}$   | -             | 90  | -   | 80  | mA            | 1, 3  |
| $\overline{\text{CAS}}$ - before- $\overline{\text{RAS}}$ refresh current | $I_{CC5}$ | $t_{RC} = \text{min}$<br>RAS, LCAS / UCAS cycling   | -             | 160 | -   | 145 | mA            | 1, 2  |
| Self- refresh current   | $I_{CC6}$ | $t_{RASS} \geq 100\mu\text{s}$  | -             | 450 | -   | 550 | $\mu\text{A}$ |       |
| Input leakage current   | $I_{LI}$  | $0\text{V} \leq V_{in} \leq V_{CC} + 0.3\text{V}$   | -5            | 5   | -5  | 5   | $\mu\text{A}$ |       |
| Output leakage current  | $I_{LO}$  | $0\text{V} \leq V_{out} \leq V_{CC} + 0.3\text{V}$<br>Dout = Disable  | -5            | 5   | -5  | 5   | $\mu\text{A}$ |       |
| Output high Voltage   | $V_{OH}$  | $I_{OH} = -2\text{mA}$  | 2.4           | -   | 2.4 | -   | V             |       |
| Output low voltage  | $V_{OL}$  | $I_{OL} = +2\text{mA}$  | -             | 0.4 | -   | 0.4 | V             |       |

Notes:

1.  $I_{CC}$  is specified as an average current. It depends on output loading condition and cycle rate when the device is selected.  $I_{CC}$  max is specified at the output open condition.
2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .
3. For  $I_{CC4}$ , address can be changed once or less within one EDO page mode cycle time.



**AC Characteristics**( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$  or  $3.15\text{V}\sim 3.6\text{V}$ ,  $V_{SS} = 0\text{V}$ ) \*1, \*2, \*3, \*4, \*5

Test conditions

- Output load:  
two TTL Loads and 50pF ( $V_{CC} = 5.0\text{V} \pm 10\%$ ); one TTL Load and 50pF ( $V_{CC} = 3.15\text{V}\sim 3.6\text{V}$ )
- Input timing reference levels:  
 $V_{IH} = 2.4\text{V}$ ,  $V_{IL} = 0.8\text{V}$  ( $V_{CC} = 5.0\text{V} \pm 10\%$ );  $V_{IH} = 2.0\text{V}$ ,  $V_{IL} = 0.8\text{V}$  ( $V_{CC} = 3.15\text{V}\sim 3.6\text{V}$ )
- Output timing reference levels:  
 $V_{OH} = 2.0\text{V}$ ,  $V_{OL} = 0.8\text{V}$  ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $3.15\text{V}\sim 3.6\text{V}$ )

**Read, Write, Read- Modify- Write and Refresh Cycles**

**(Common Parameters)**

| Parameter   | Symbol    | VG26(V)(S) 18165 |     |     |     | Unit | Notes |
|---|-----------|------------------|-----|-----|-----|------|-------|
|   |           | -5               |     | -6  |     |      |       |
|   |           | Min              | Max | Min | Max |      |       |
| Random read or write cycle time   | $t_{RC}$  | 84               | -   | 104 | -   | ns   |       |
| $\overline{\text{RAS}}$ precharge time  | $t_{RP}$  | 30               | -   | 40  | -   | ns   |       |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ precharge time in normal mode             | $t_{CPN}$ | 10               | -   | 10  | -   | ns   |       |
| $\overline{\text{RAS}}$ pulse width   | $t_{RAS}$ | 50               | 10K | 60  | 10K | ns   | 6     |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ pulse width                               | $t_{CAS}$ | 8                | 10K | 10  | 10K | ns   | 7     |
| Row address setup time  | $t_{ASR}$ | 0                | -   | 0   | -   | ns   |       |
| Row address hold time   | $t_{RAH}$ | 8                | -   | 10  | -   | ns   |       |
| Column address setup time   | $t_{ASC}$ | 0                | -   | 0   | -   | ns   | 8     |
| Column address hold time  | $t_{CAH}$ | 8                | -   | 10  | -   | ns   |       |
| $\overline{\text{RAS}}$ to $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ delay time     | $t_{RCD}$ | 12               | 37  | 14  | 45  | ns   | 9     |
| $\overline{\text{RAS}}$ to column address delay time  | $t_{RAD}$ | 10               | 25  | 12  | 30  | ns   | 10    |
| Column address to $\overline{\text{RAS}}$ lead time   | $t_{RAL}$ | 25               | -   | 30  | -   | ns   |       |
| $\overline{\text{RAS}}$ hold time   | $t_{RSH}$ | 8                | -   | 10  | -   | ns   |       |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ hold time                                 | $t_{CSH}$ | 38               | -   | 40  | -   | ns   |       |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ to $\overline{\text{RAS}}$ precharge time | $t_{CRP}$ | 5                | -   | 5   | -   | ns   | 11    |
| $\overline{\text{OE}}$ to Din delay time  | $t_{OED}$ | 20               | -   | 20  | -   | ns   |       |
| Transition time (rise and fall)   | $t_T$     | 1                | 50  | 1   | 50  | ns   | 12    |
| Refresh period  | $t_{REF}$ | -                | 16  | -   | 16  | ms   |       |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ to output in Low- Z                       | $t_{CLZ}$ | 0                | -   | 0   | -   | ns   |       |
| $\overline{\text{LCAS}}$ / $\overline{\text{UCAS}}$ delay time from Din                       | $t_{DZC}$ | 0                | -   | 0   | -   | ns   |       |
| $\overline{\text{OE}}$ delay time from Din  | $t_{DZO}$ | 0                | -   | 0   | -   | ns   |       |

**Read Cycle**

| Parameter   | Symbol           | VG26(V)(S)18165 |     |     |     | Unit | Notes  |
|---|------------------|-----------------|-----|-----|-----|------|--------|
|   |                  | -5              |     | -6  |     |      |        |
|   |                  | Min             | Max | Min | Max |      |        |
| Access time from $\overline{\text{RAS}}$                                    | $t_{\text{RAC}}$ | -               | 50  | -   | 60  | ns   | 13     |
| Access time from $\overline{\text{LCAS}} / \overline{\text{UCAS}}$          | $t_{\text{CAC}}$ | -               | 13  | -   | 15  | ns   | 14, 15 |
| Access time from column address   | $t_{\text{AA}}$  | -               | 25  | -   | 30  | ns   | 15, 16 |
| Access time from $\overline{\text{OE}}$                                     | $t_{\text{OEA}}$ | -               | 12  | -   | 15  | ns   |        |
| Read command setup time   | $t_{\text{RCS}}$ | 0               | -   | 0   | -   | ns   | 8      |
| Read command hold time to $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ | $t_{\text{RCH}}$ | 0               | -   | 0   | -   | ns   | 11, 17 |
| Read command hold time to $\overline{\text{RAS}}$                           | $t_{\text{RRH}}$ | 10              | -   | 10  | -   | ns   | 17     |
| Output buffer turn-off time   | $t_{\text{OFF}}$ | 0               | 12  | 0   | 15  | ns   | 18     |
| Output buffer turn-off time from $\overline{\text{OE}}$                     | $t_{\text{OEZ}}$ | 0               | 12  | 0   | 15  | ns   | 18     |

**Write Cycle**

| Parameter  | Symbol           | VG26(V)(S)18165 |     |     |     | Unit | Notes |
|--|------------------|-----------------|-----|-----|-----|------|-------|
|  |                  | -5              |     | -6  |     |      |       |
|  |                  | Min             | Max | Min | Max |      |       |
| Write command setup time   | $t_{\text{WCS}}$ | 0               | -   | 0   | -   | ns   | 8, 19 |
| Write command hold time  | $t_{\text{WCH}}$ | 8               | -   | 10  | -   | ns   |       |
| Write command pulse width  | $t_{\text{WP}}$  | 8               | -   | 10  | -   | ns   |       |
| Write command to $\overline{\text{RAS}}$ lead time                           | $t_{\text{RWL}}$ | 13              | -   | 15  | -   | ns   |       |
| Write command to $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ lead time | $t_{\text{CWL}}$ | 8               | -   | 10  | -   | ns   | 20    |
| Data-in setup time   | $t_{\text{DS}}$  | 0               | -   | 0   | -   | ns   | 21    |
| Data-in hold time  | $t_{\text{DH}}$  | 8               | -   | 10  | -   | ns   | 21    |
| $\overline{\text{WE}}$ to Data-in delay                                      | $t_{\text{WED}}$ | 10              | -   | 10  | -   | ns   |       |

**Read- Modify- Write Cycle**

| Parameter  | Symbol           | VG26(V)(S)18165 |     |     |     | Unit | Notes |
|--|------------------|-----------------|-----|-----|-----|------|-------|
|  |                  | -5              |     | -6  |     |      |       |
|  |                  | Min             | Max | Min | Max |      |       |
| Read-modify- write cycle time  | $t_{\text{RWC}}$ | 108             | -   | 133 | -   | ns   |       |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time                           | $t_{\text{RWD}}$ | 64              | -   | 77  | -   | ns   | 19    |
| $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ to $\overline{\text{WE}}$ delay time | $t_{\text{CWD}}$ | 26              | -   | 32  | -   | ns   | 19    |
| Column address to $\overline{\text{WE}}$ delay time                                    | $t_{\text{AWD}}$ | 39              | -   | 47  | -   | ns   | 19    |
| $\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$                           | $t_{\text{OEH}}$ | 8               | -   | 10  | -   | ns   |       |

### Refresh Cycle

| Parameter  | Symbol            | VG26(V)(S)18165 |     |     |     | Unit          | Notes |
|--|-------------------|-----------------|-----|-----|-----|---------------|-------|
|  |                   | -5              |     | -6  |     |               |       |
|  |                   | Min             | Max | Min | Max |               |       |
| $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ setup time (CBR refresh)     | $t_{\text{CSR}}$  | 5               | -   | 5   | -   | ns            |       |
| $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ hold time (CBR refresh)      | $t_{\text{CHR}}$  | 8               | -   | 10  | -   | ns            | 11    |
| $\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time         | $t_{\text{RPC}}$  | 5               | -   | 5   | -   | ns            | 8     |
| $\overline{\text{RAS}}$ pulse width (self refresh)                             | $t_{\text{RASS}}$ | 100             | -   | 100 | -   | $\mu\text{s}$ |       |
| $\overline{\text{RAS}}$ precharge time (self refresh)                          | $t_{\text{RPS}}$  | 90              | -   | 110 | -   | ns            |       |
| $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ hold time (CBR self refresh) | $t_{\text{CHS}}$  | -50             | -   | -50 | -   | ns            |       |
| $\overline{\text{WE}}$ setup time  | $t_{\text{WSR}}$  | 0               | -   | 0   | -   | ns            |       |
| $\overline{\text{WE}}$ hold time   | $t_{\text{WHR}}$  | 10              | -   | 10  | -   | ns            |       |

### EDO Page Mode Cycle

| Parameter   | Symbol            | VG26(V)(S)18165 |        |     |        | Unit | Notes  |
|---|-------------------|-----------------|--------|-----|--------|------|--------|
|   |                   | -5              |        | -6  |        |      |        |
|   |                   | Min             | Max    | Min | Max    |      |        |
| EDO page mode cycle time  | $t_{\text{PC}}$   | 20              | -      | 25  | -      | ns   |        |
| EDO page mode $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ precharge time                                    | $t_{\text{CP}}$   | 10              | -      | 10  | -      | ns   |        |
| EDO page mode $\overline{\text{RAS}}$ pulse width   | $t_{\text{RASP}}$ | 50              | $10^5$ | 60  | $10^5$ | ns   | 22     |
| Access time from $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ precharge                                      | $t_{\text{CPA}}$  | -               | 30     | -   | 35     | ns   | 11, 15 |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ pre-charge               | $t_{\text{CPRH}}$ | 30              | -      | 35  | -      | ns   |        |
| $\overline{\text{OE}}$ high hold time from $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ high                 | $t_{\text{OEHC}}$ | 5               | -      | 5   | -      | ns   |        |
| $\overline{\text{OE}}$ high pulse width   | $t_{\text{OEP}}$  | 10              | -      | 10  | -      | ns   |        |
| Data output hold time after $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ low                                 | $t_{\text{COH}}$  | 5               | -      | 5   | -      | ns   |        |
| Output disable delay from $\overline{\text{WE}}$  | $t_{\text{WHZ}}$  | 3               | 10     | 3   | 10     | ns   |        |
| $\overline{\text{WE}}$ pulse width for output disable when $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ high | $t_{\text{WPZ}}$  | 10              | -      | 10  | -      | ns   |        |

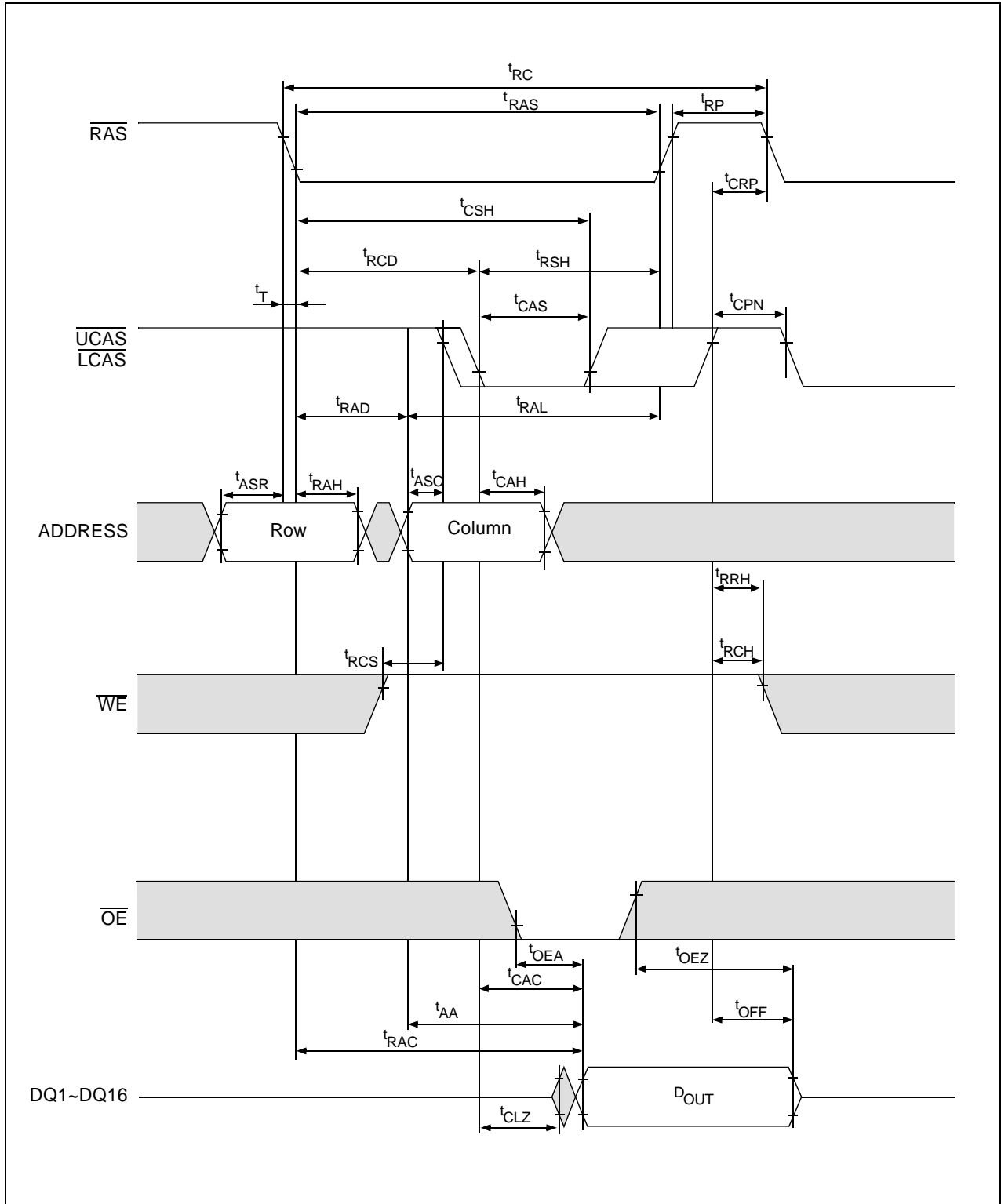
### EDO Page Mode Read Modify Write Cycle

| Parameter  | Symbol            | VG26(V)(S)18165 |     |     |     | Unit | Notes |
|--|-------------------|-----------------|-----|-----|-----|------|-------|
|  |                   | -5              |     | -6  |     |      |       |
|  |                   | Min             | Max | Min | Max |      |       |
| EDO page mode read- modify- write cycle $\overline{\text{LCAS}} / \overline{\text{UCAS}}$ precharge to $\overline{\text{WE}}$ delay time | $t_{\text{CPW}}$  | 45              | -   | 55  | -   | ns   | 11    |
| EDO page mode read- modify- write cycle time   | $t_{\text{PRWC}}$ | 56              | -   | 68  | -   | ns   |       |

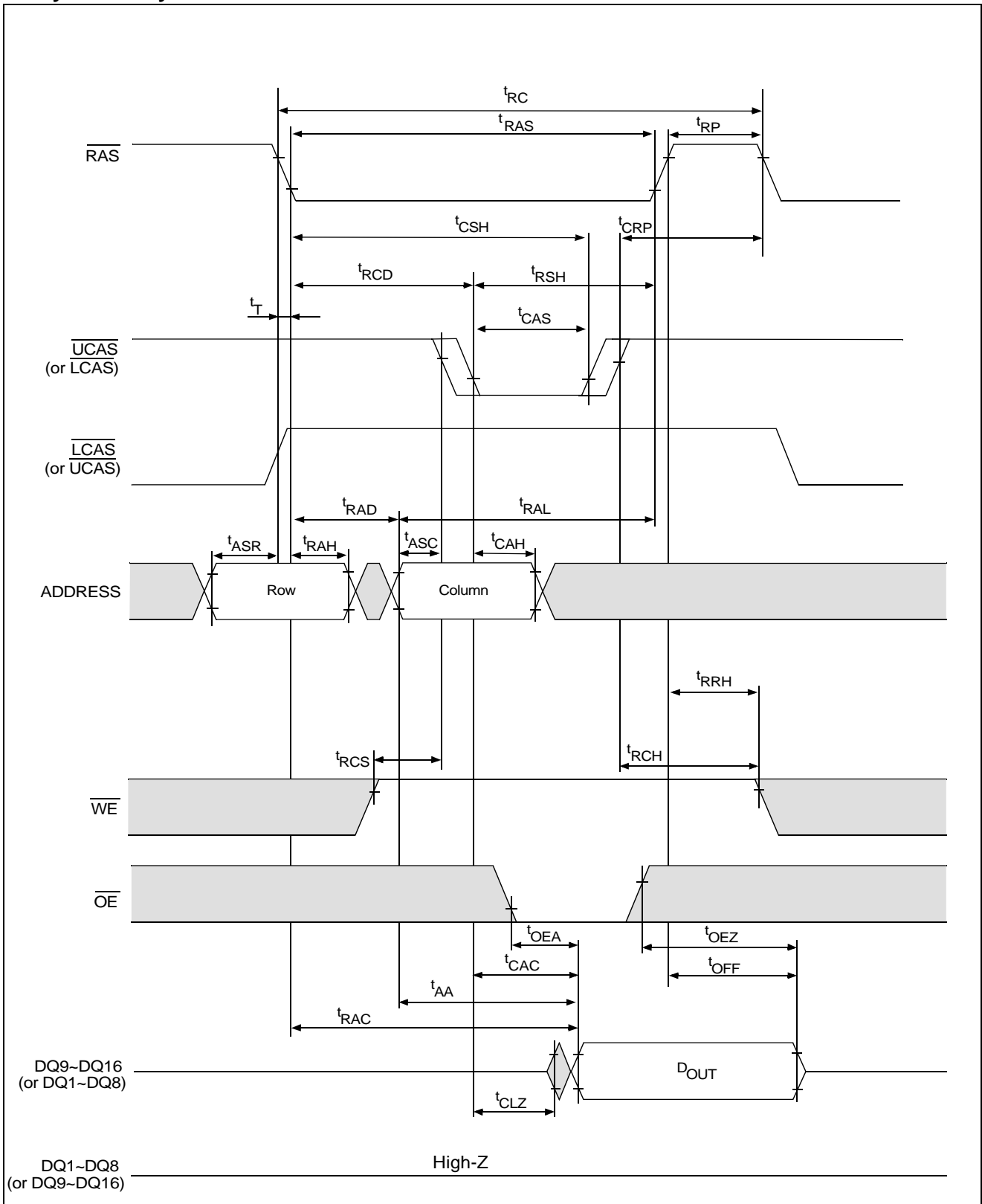
Notes :

1. AC measurements assume  $t_T = 1\text{ns}$ .
2. An initial pause of  $100\ \mu\text{s}$  is required after power up, and it followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$  - only refresh cycle or  $\overline{\text{CAS}}$  - before -  $\overline{\text{RAS}}$  refresh cycle). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$  - before -  $\overline{\text{RAS}}$  refresh cycles are required.
3. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
4. All the  $V_{CC}$  and  $V_{SS}$  pins shall be supplied with the same voltages.
5. When both  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  go low at the same time, all 16-bits data are written into the device.  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  cannot be staggered within the same write/read cycles.
6.  $t_{\text{RAS}}(\text{min}) = t_{\text{RWD}}(\text{min}) + t_{\text{RWL}}(\text{min}) + t_T$  in read-modify-write cycle.
7.  $t_{\text{CAS}}(\text{min}) = t_{\text{CWD}}(\text{min}) + t_{\text{CWL}}(\text{min}) + t_T$  in read-modify-write cycle.
8.  $t_{\text{ASC}}(\text{min})$ ,  $t_{\text{RCS}}(\text{min})$ ,  $t_{\text{WCS}}(\text{min})$ , and  $t_{\text{RPC}}$  are determined by the falling edge of  $\overline{\text{CAS}}$ .
9.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only, and  $t_{\text{RAC}}(\text{max})$  can be met with the  $t_{\text{RCD}}(\text{max})$  limit. Otherwise,  $t_{\text{RAC}}$  is controlled exclusively by  $t_{\text{CAC}}$  if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit.
10.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only, and  $t_{\text{RAC}}(\text{max})$  can be met with the  $t_{\text{RAD}}(\text{max})$  limit. Otherwise,  $t_{\text{RAC}}$  is controlled exclusively by  $t_{\text{AA}}$  if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit.
11.  $t_{\text{CRP}}$ ,  $t_{\text{CHR}}$ ,  $t_{\text{RCH}}$ ,  $t_{\text{CPA}}$  and  $t_{\text{CPW}}$  are determined by the rising edge of  $\overline{\text{CAS}}$ .
12.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing or input signals. Therefore, transition time is measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ .
13. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
14. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ .
15. Access time is determined by the maximum of  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$ ,  $t_{\text{CPA}}$ .
16. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ .
17. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
18.  $t_{\text{OFF}}(\text{max})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the output achieves the open circuit condition (high impedance).  $t_{\text{OFF}}$  is determined by the later rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ .
19.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ , and  $t_{\text{AWD}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
20.  $t_{\text{CWL}}$  shall be satisfied by both  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$ .
21. These parameters are referenced to  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  separately in an early write cycle and to  $\overline{\text{WE}}$  edge in a delayed write or a read-modify-write cycle.
22.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in EDO page mode cycles.

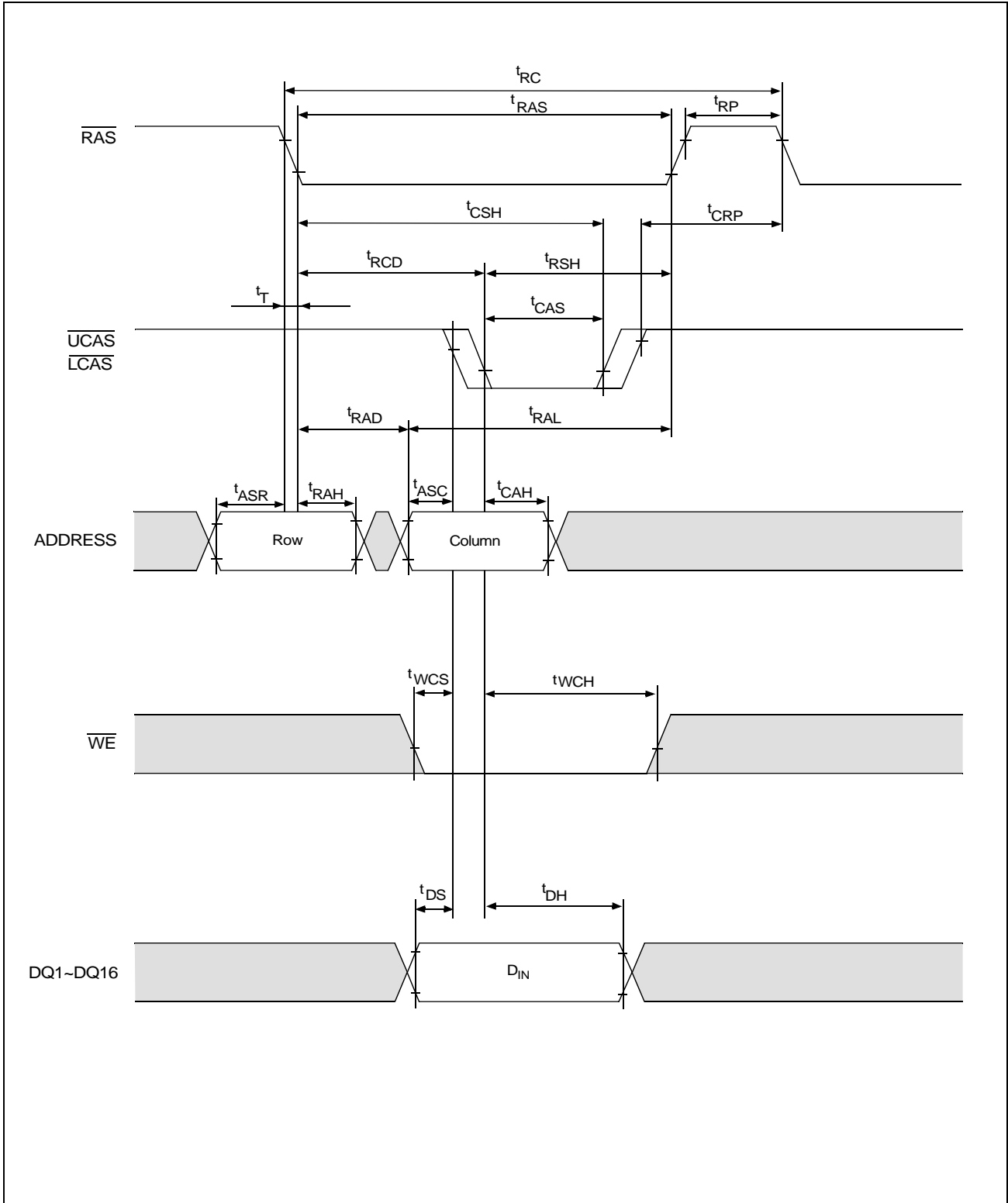
Timing Waveforms  
 • Word Read Cycle



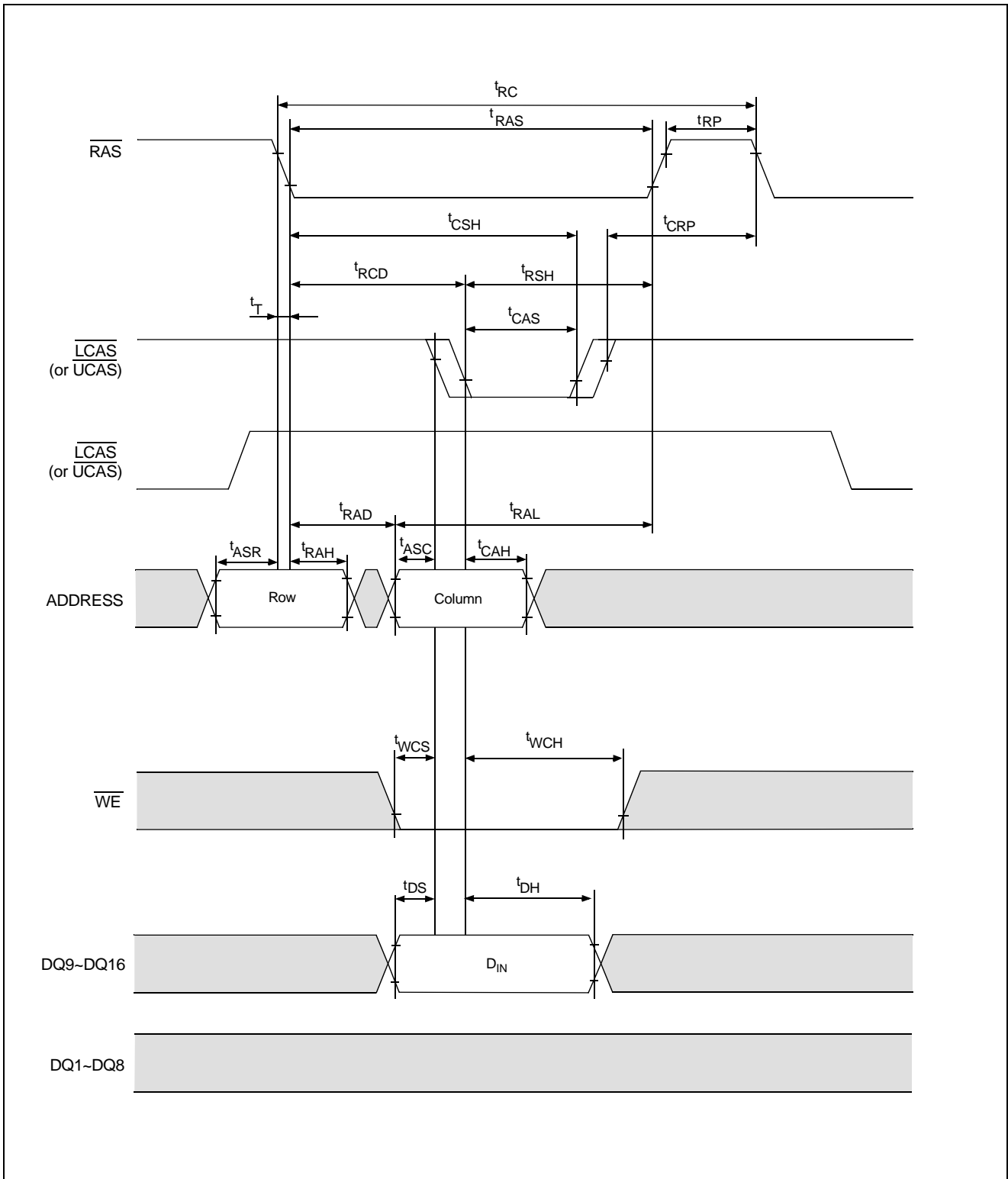
• Byte Read Cycle



• Word Early Write Cycle

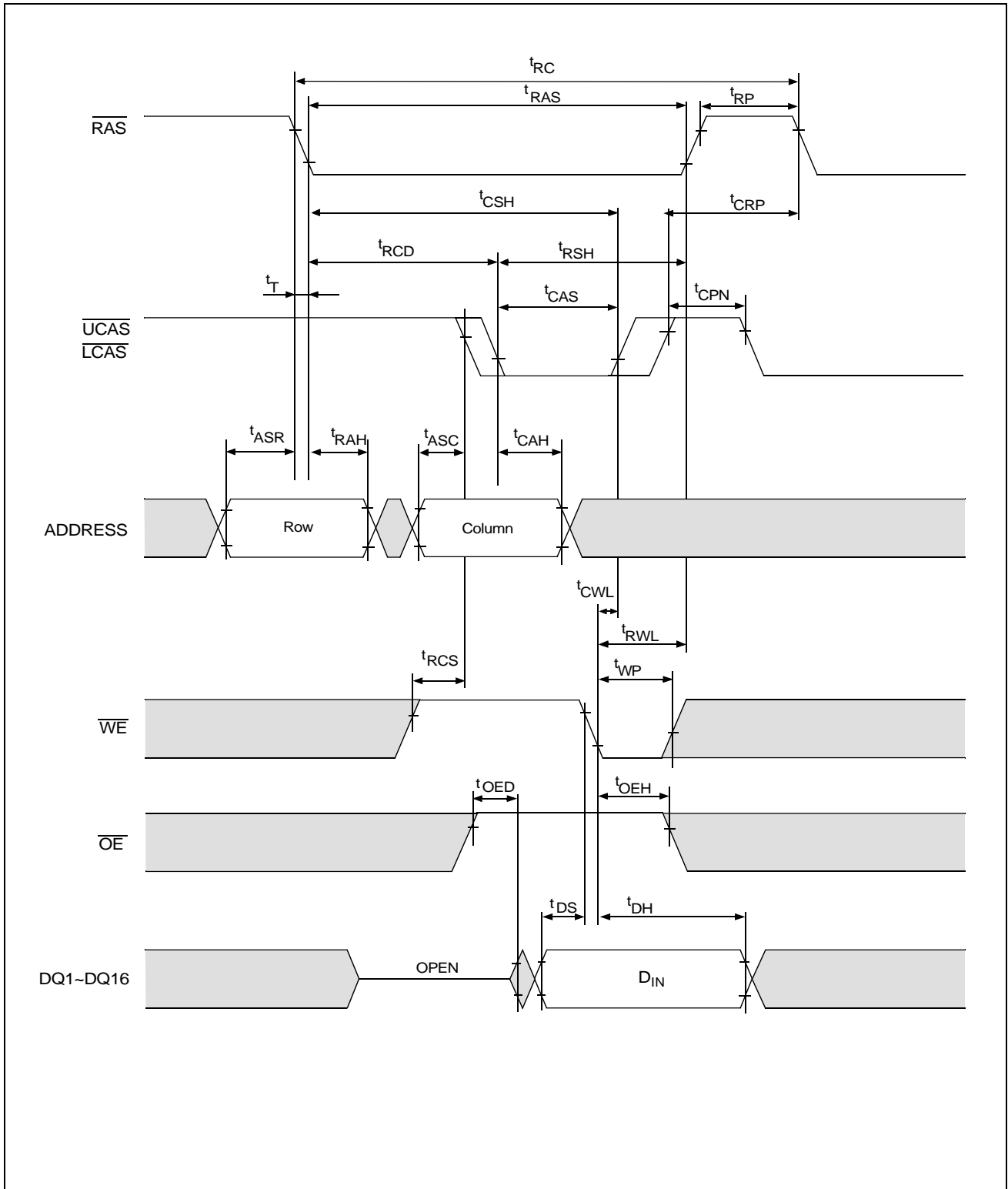


• Byte Early Write Cycle

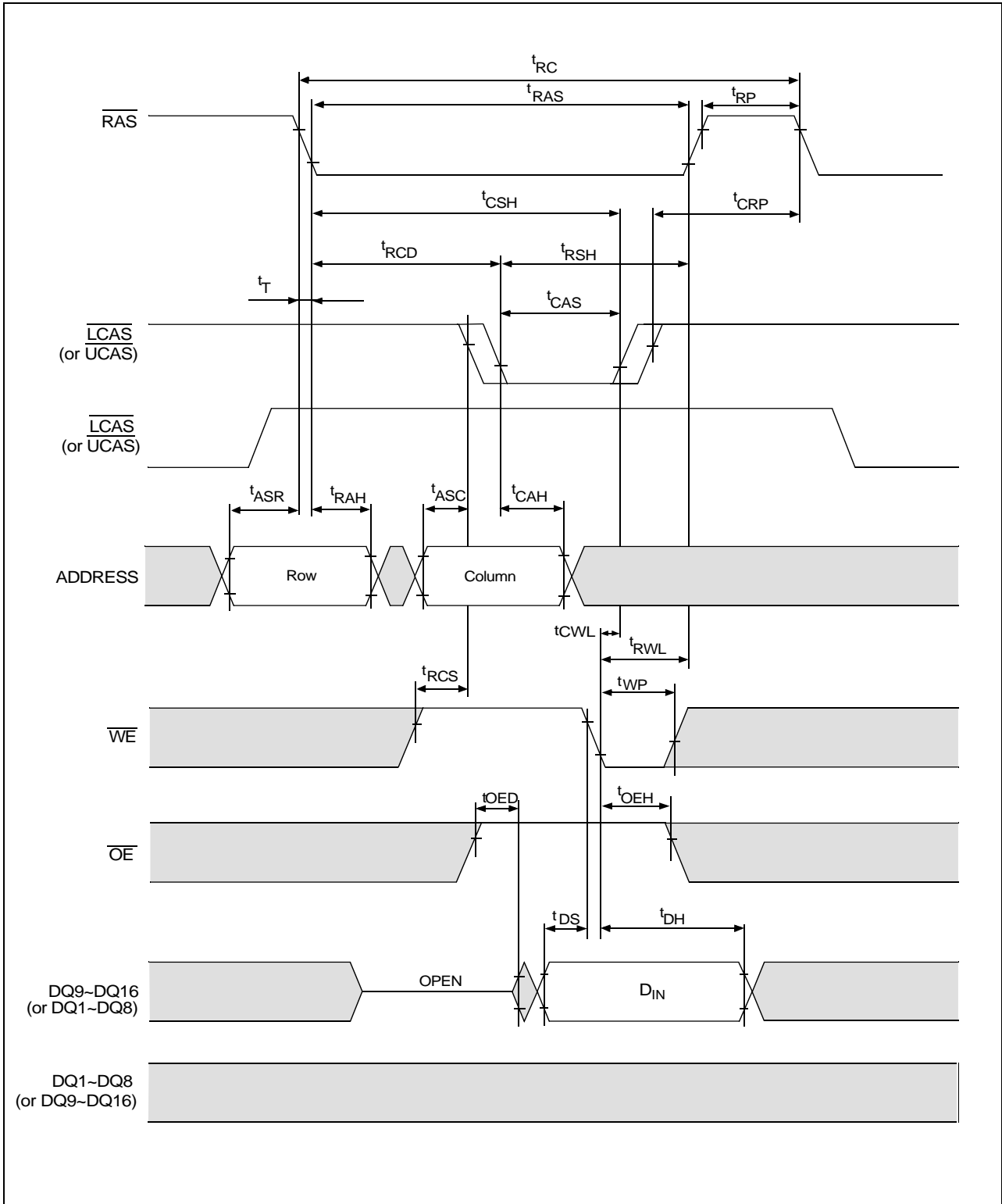




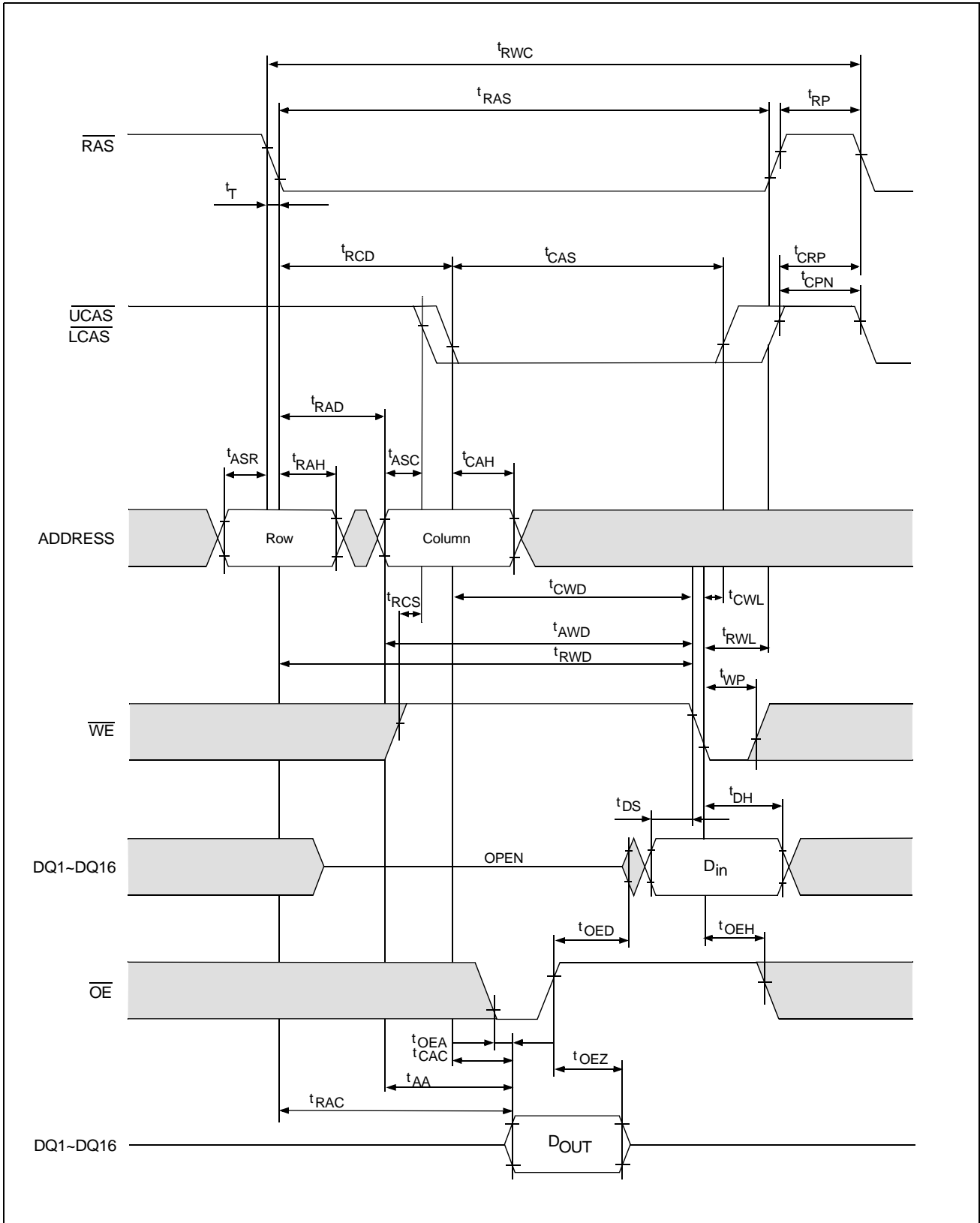
• Word Delayed Write Cycle



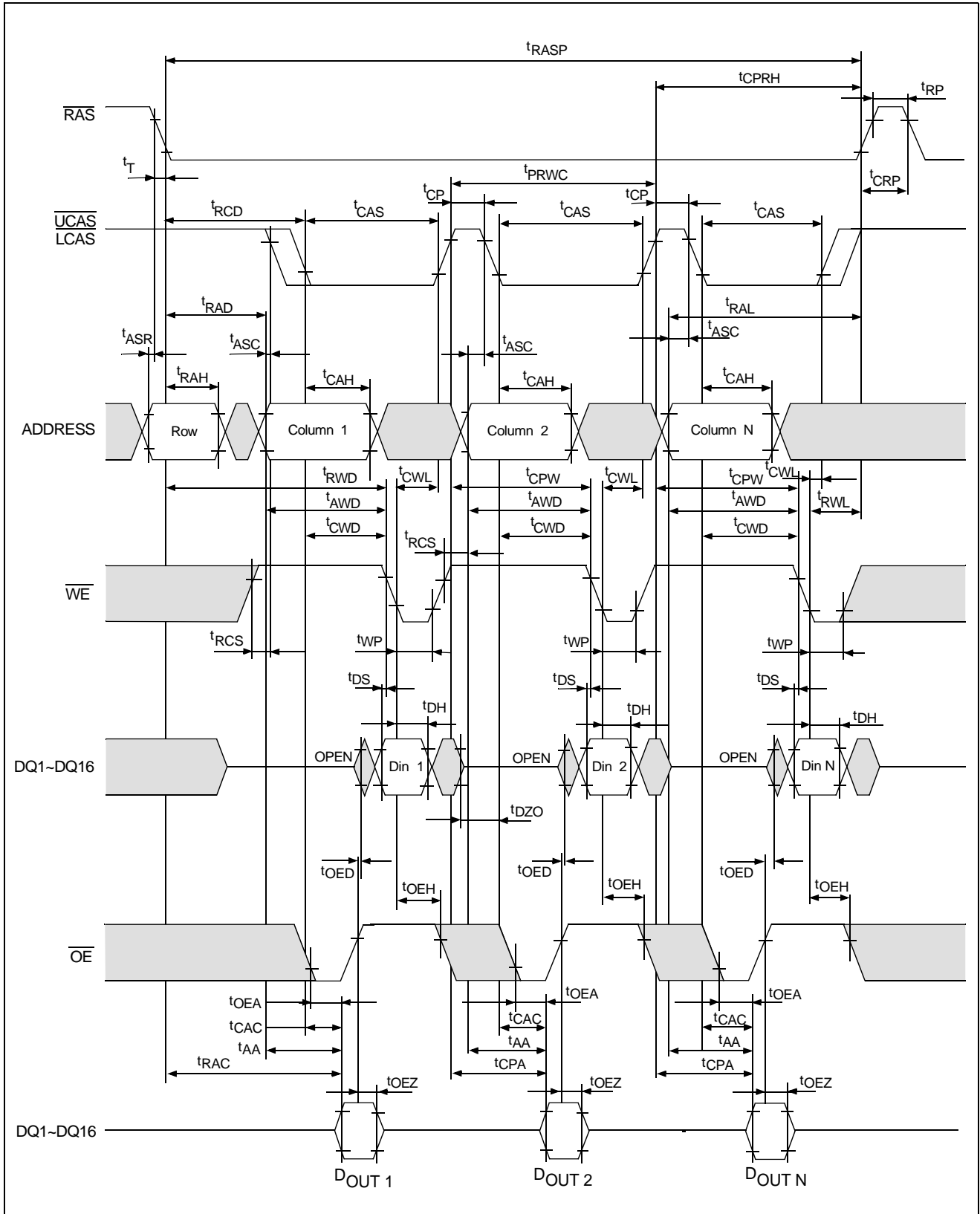
• Byte Delayed Write Cycle



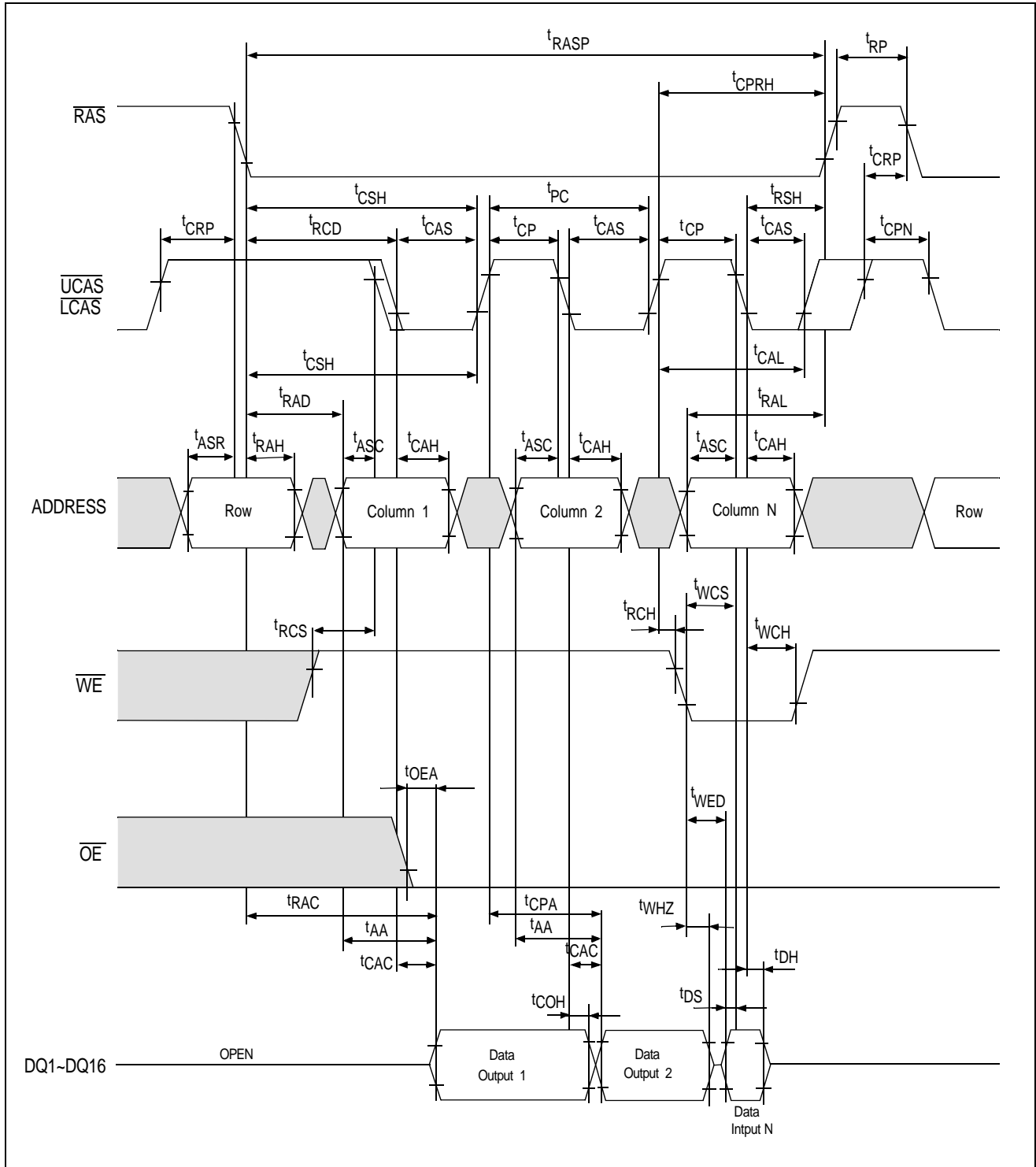
• Word Read-Modify-Write Cycle



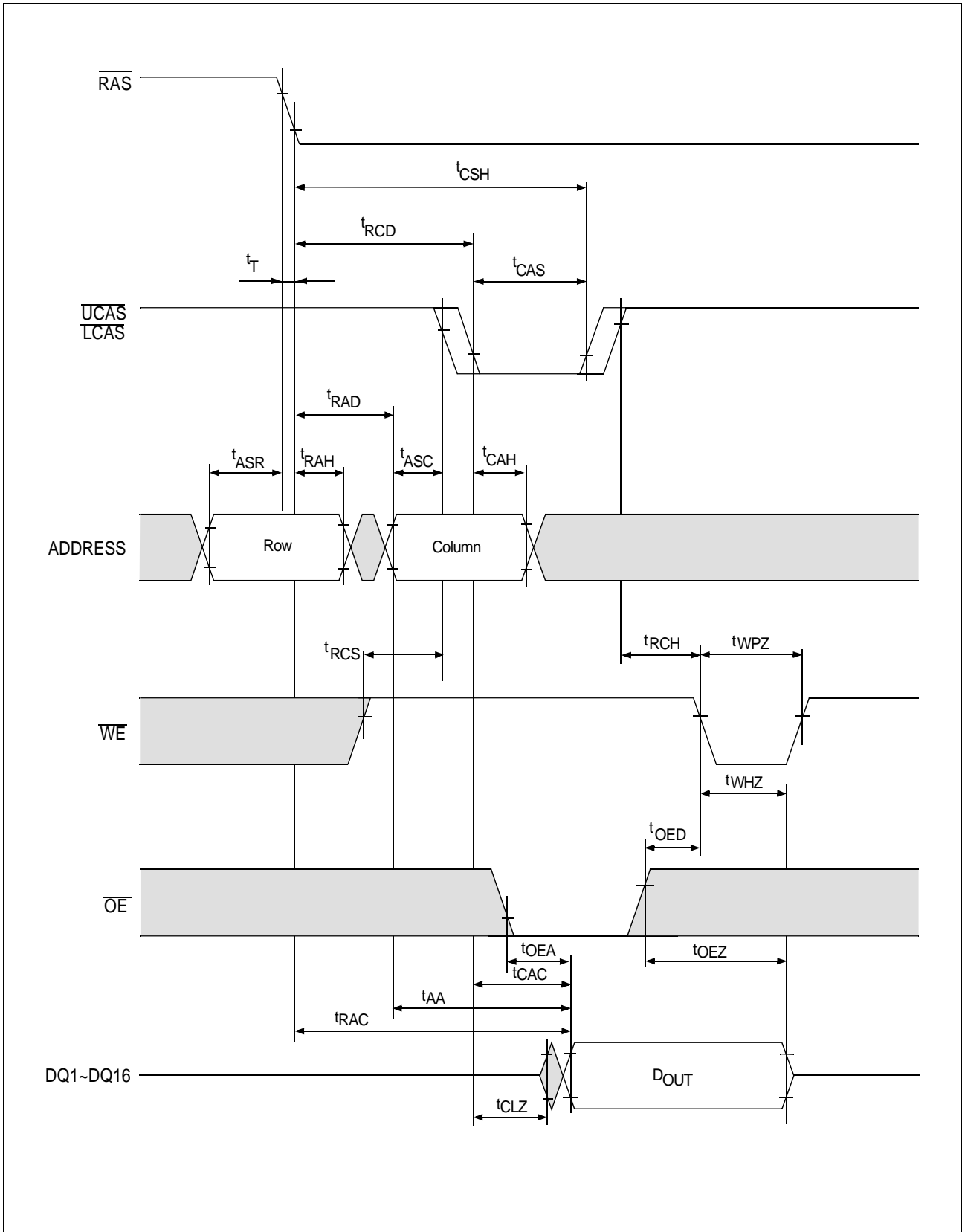
• EDO Page Mode Word Read-Modify-Write Cycle



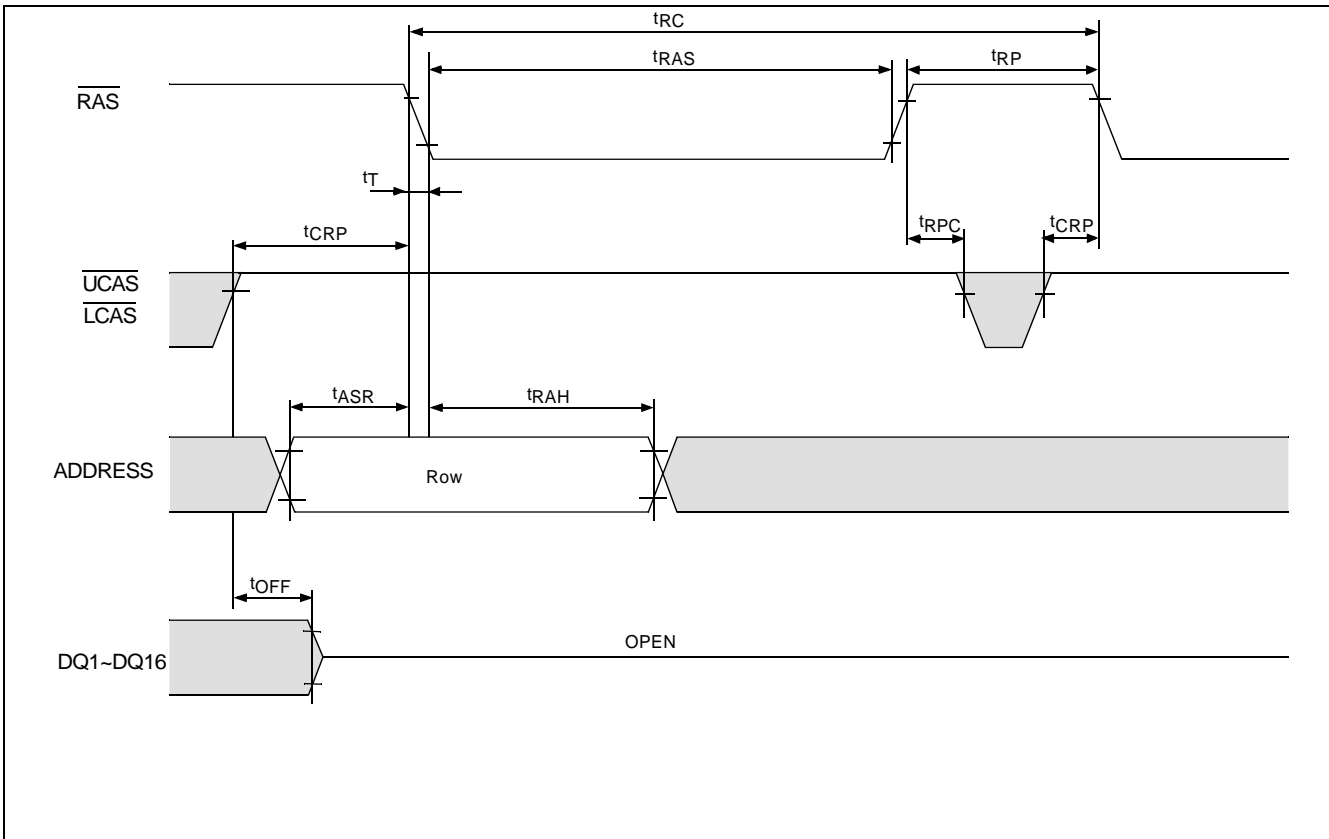
• EDO Page Mode Word Read-Early-Write Cycle



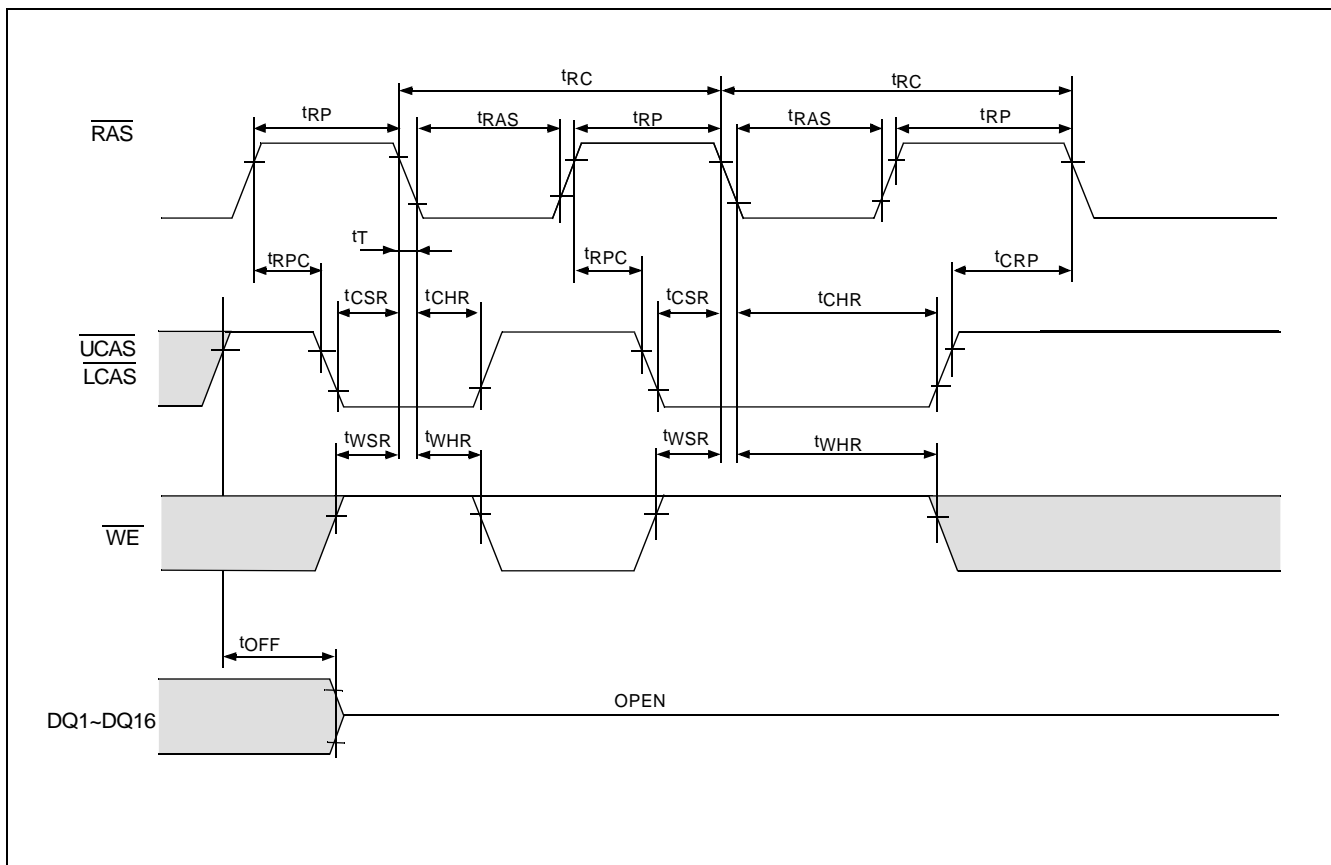
• Read Cycle with  $\overline{WE}$  Controlled Disable



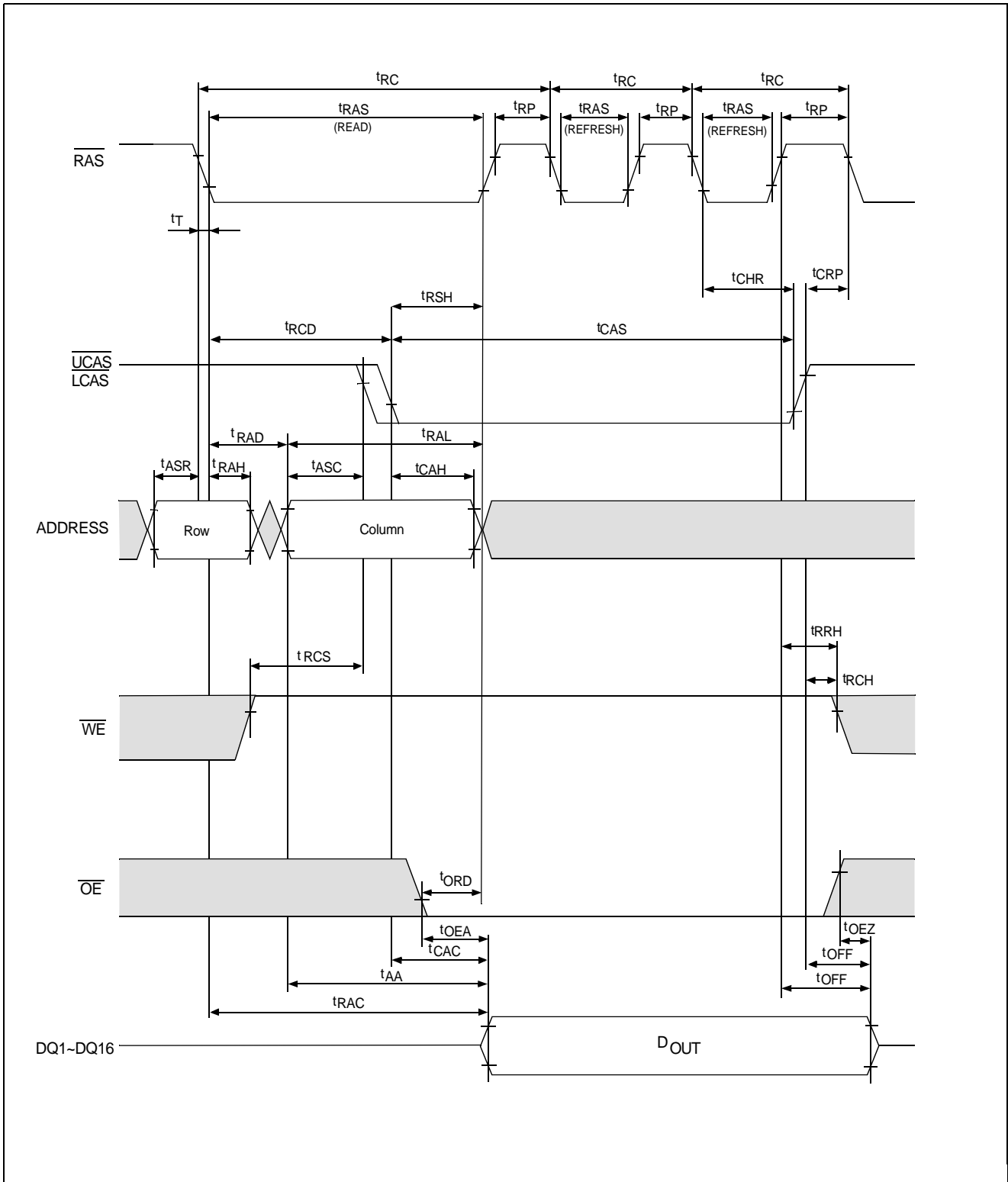
## RAS - Only Refresh Cycle



## CAS-Before-RAS Refresh Cycle

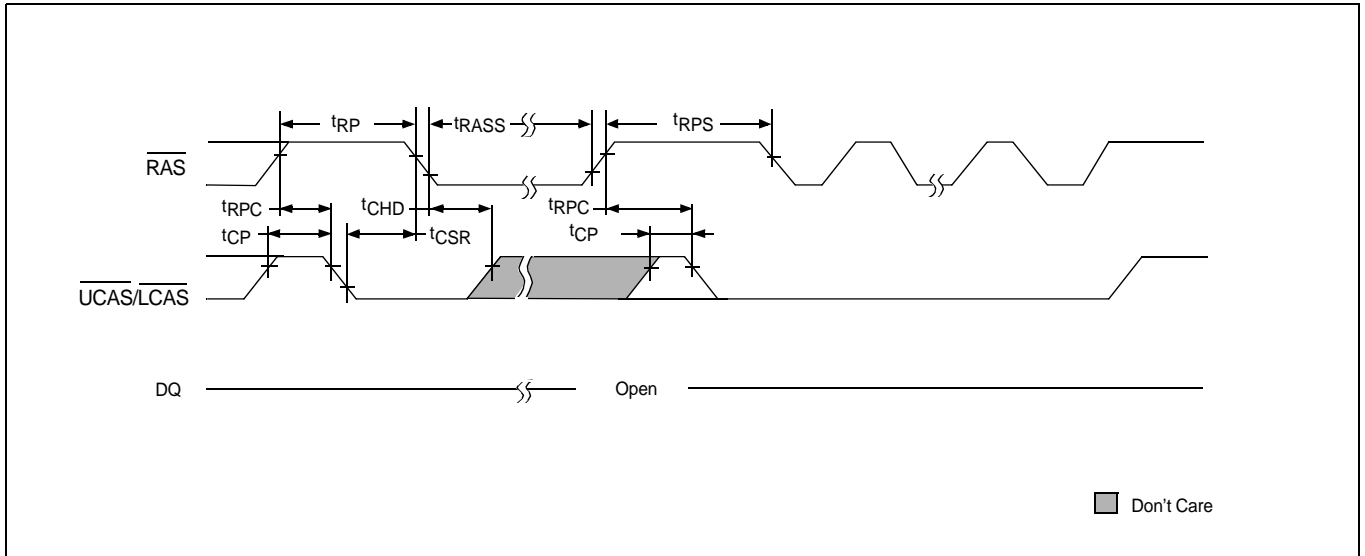


• Hidden Refresh Cycle





• SELF REFRESH CYCLE (Addresses,  $\overline{WE}$  and  $\overline{OE}$  = DON'T CARE)



**Ordering information**

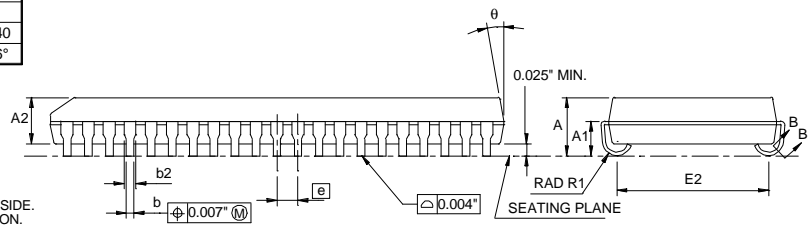
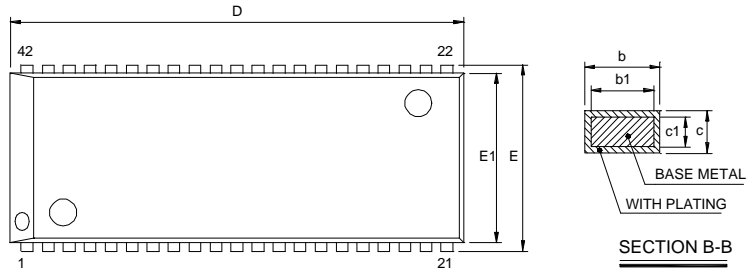
| Part Number         | Access time | Package                   |
|---------------------|-------------|---------------------------|
| VG26(V)(S)18165CJ-5 | 50 ns       | 400mil 42-Pin Plastic SOJ |
| VG26(V)(S)18165CJ-6 | 60 ns       |                           |
| VG26(V)(S)18165CT-5 | 50 ns       | 400mil 50(44) -Pin TSOPII |
| VG26(V)(S)18165CT-6 | 60 ns       |                           |

**VG26(V)(S)18165CJ-5**

- VG → • VIS Memory Product
- 26 → • Technology
- V → • V: 3.3V Version; Non: 5V
- S → • S: Self Refresh; Non: Non Self Refresh
- 18165 → • Device Type and Configuration
- C → • Revision (C and D)
- J → • Package Type (J : SOJ, T : TSOP II)
- 5 → • Speed (5: 50 ns, 6: 60 ns)

**Package Information 42-pin SOJ**

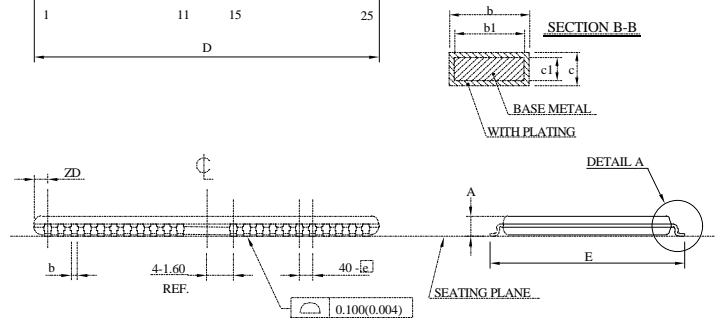
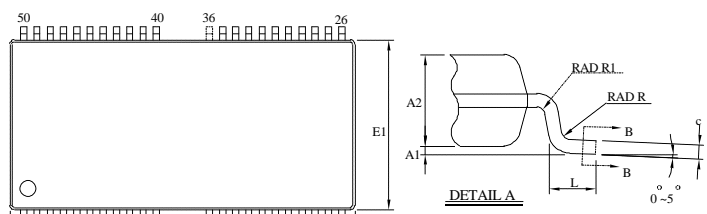
| DIM | MILLIMETERS |       |       | INCHES      |       |       |
|-----|-------------|-------|-------|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  | MIN.        | NOM.  | MAX.  |
| A   | 3.25        | 3.51  | 3.76  | 0.128       | 0.138 | 0.148 |
| A1  | 2.08        | ---   | ---   | 0.082       | ---   | ---   |
| A2  | 2.79 REF.   |       |       | 0.110 REF.  |       |       |
| b   | 0.38        | ---   | 0.51  | 0.015       | ---   | 0.020 |
| b1  | 0.38        | ---   | 0.46  | 0.015       | ---   | 0.018 |
| b2  | 0.66        | 0.71  | 0.81  | 0.026       | 0.028 | 0.032 |
| c   | 0.18        | ---   | 0.33  | 0.007       | ---   | 0.013 |
| c1  | 0.18        | 0.20  | 0.28  | 0.007       | 0.008 | 0.011 |
| e   | 1.27 BASIC  |       |       | 0.050 BASIC |       |       |
| D   | 27.18       | 27.31 | 27.43 | 1.070       | 1.075 | 1.080 |
| E   | 11.05       | 11.18 | 11.30 | 0.435       | 0.440 | 0.445 |
| E1  | 10.03       | 10.16 | 10.29 | 0.395       | 0.400 | 0.405 |
| E2  | 9.40 BASIC  |       |       | 0.370 BASIC |       |       |
| R1  | 0.76        | 0.89  | 1.02  | 0.030       | 0.035 | 0.040 |
| θ   | 3°          | ---   | 16°   | 3°          | ---   | 16°   |



NOTE:  
 1. CONTROLLING DIMENSION : INCHES  
 2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.  
 MOLD PROTRUSION SHALL NOT EXCEED 0.006"(0.15) PER SIDE.  
 DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.  
 INTERLEAD PROTRUSION SHALL NOT EXCEED 0.01"(0.25) PER SIDE.  
 3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION OR  
 INTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE  
 SHOULDER WIDTH TO EXCEED b2 MAX BY MORE THAN 0.005"(0.127)  
 DAMBAR INTRUSION SHALL NOT REDUCE THE SHOULDER WIDTH  
 TO LESS THAN 0.001"(0.025) BELOW b2 MIN.

**Package Information 50(44)-pin TSOPII**

| DIM | MILLIMETERS |       |       | INCHES       |       |       |
|-----|-------------|-------|-------|--------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  | MIN.         | NOM.  | MAX.  |
| A   | ---         | ---   | 1.20  | ---          | ---   | 0.047 |
| A1  | 0.05        | ---   | 0.15  | 0.002        | ---   | 0.006 |
| A2  | 0.95        | 1.00  | 1.05  | 0.037        | 0.039 | 0.041 |
| b   | 0.30        | ---   | 0.45  | 0.012        | ---   | 0.018 |
| b1  | 0.30        | ---   | 0.40  | 0.012        | ---   | 0.016 |
| c   | 0.12        | ---   | 0.21  | 0.005        | ---   | 0.008 |
| c1  | 0.11        | ---   | 0.16  | 0.0045       | ---   | 0.006 |
| D   | 20.82       | 20.95 | 21.08 | 0.820        | 0.825 | 0.830 |
| ZD  | 0.875 BASIC |       |       | 0.0344 BASIC |       |       |
| e   | 0.80 BASIC  |       |       | 0.0315 BASIC |       |       |
| E   | 11.56       | 11.76 | 11.96 | 0.455        | 0.463 | 0.471 |
| E1  | 10.03       | 10.16 | 10.29 | 0.395        | 0.400 | 0.405 |
| L   | 0.40        | 0.50  | 0.60  | 0.016        | 0.020 | 0.024 |
| R   | 0.11        | ---   | 0.25  | 0.004        | ---   | 0.010 |
| R1  | 0.11        | ---   | ---   | 0.004        | ---   | ---   |



NOTE:  
 1. CONTROLLING DIMENSION : MILLIMETERS  
 2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.  
 MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE.  
 DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.  
 INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.  
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.  
 ALLOWABLE DAMBAR PROTRUSIONS SHALL NOT CAUSE THE LEAD TO  
 BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.  
 DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER  
 THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.