

CGS64/74B305

Octal Divide-by-2 Skew Clock Driver

General Description

These minimum skew clock drivers are designed for high frequency Clock Generation & Support (CGS) applications. These devices are ideal for duty cycle recovery applications with internal frequency divide-by-2 circuitry. The devices guarantee minimum skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems.

Functional Description

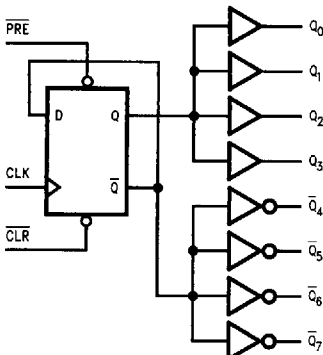
The CGS74B305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. PRE and CLR inputs are provided to set Q and \bar{Q} outputs high or low independent of CLK pin.

Features

- Clock Generation & Support (CGS) devices ideal for high frequency signal generation or clock distribution applications
- Fabricated on National's Advanced Bipolar FAST™ LSI process
- 750 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- Current sourcing 24 mA and current sinking of 48 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Ordering Code: See Section 5

Logic Diagram



Circuit description of the '305 TL/F/11751-3

Pin Description

| Pin Names | Description |
|--------------------------------|-------------|
| CLK | Clock Input |
| Q ₀ -Q ₇ | Outputs |
| PRE | Preset |
| CLR | Clear |

Truth Table

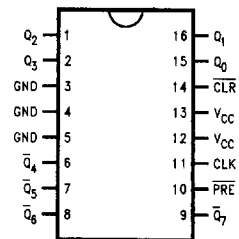
CGS74B305

| Inputs | | | Outputs | |
|--------|-----|-----|--------------------------------|---------------------------|
| CLR | PRE | CLK | Q ₀ -Q ₃ | \bar{Q}_4 - \bar{Q}_7 |
| L | H | X | L | H |
| H | L | X | H | L |
| L | L | X | L* | L* |
| H | H | ↑ | \bar{Q}_0 | Q ₀ |
| H | H | L | Q ₀ | \bar{Q}_0 |

*This state will not persist when CLR/PRE returns to high.

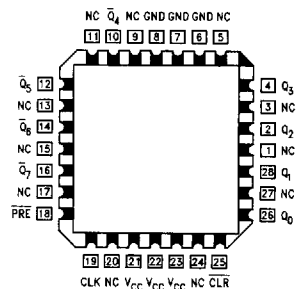
Connection Diagrams

Pin Assignment for DIP (N) and SOIC (M)



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Pin Assignment 28-Pin PLCC



TL/F/11751-2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | | | | |
|-----------------------------|--------|-----------------|-----|------|
| Supply Voltage (V_{CC}) | | 7.0V | | |
| Input Voltage (V_i) | | 7.0V | | |
| Operating Free | 74B305 | 0°C to +70°C | | |
| Air Temperature | 64B305 | -40°C to +85°C | | |
| Storage Temperature Range | | -65°C to +150°C | | |
| Typical θ_{JA} | | | | |
| Airflow (LFM) | 0 | 225 | 500 | °C/W |
| Plastic (N) Package | 95 | 70 | 60 | °C/W |
| Jedec SOIC (M) Package | 118 | 96 | 86 | °C/W |
| PLCC (V) Package | 69 | 53 | 45 | °C/W |

Recommended Operating Conditions

| | |
|---|--------------|
| Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| Input Rise and Fall Times (0.8V to 2.0V) | 2 ns max |
| Free Air Operating Temperature (T_A) | 0°C to 70°C |

NOTE: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics CGS64/74B305

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-----------------------------------|------------------------------------|--------------|------|-------|---------|
| V_{IK} | Input Clamp Voltage | $V_{CC} = 4.5V$, $I_i = -18 mA$ | | | -1.2 | V |
| V_{IH} | Minimum Input High Level Voltage | | 2.0 | | | V |
| V_{IL} | Maximum Input Low Level Voltage | | | | 0.8 | V |
| V_{OH} | High Level Output Voltage | $I_{OH} = -2 mA$, $V_{CC} = 4.5V$ | $V_{CC} - 2$ | | | V |
| | | $I_{OH} = 24 mA$, $V_{CC} = 4.5V$ | 2.0 | | | |
| V_{OL} | Low Level Output Voltage | $V_{CC} = 4.5V$, $I_{OL} = 48 mA$ | | 0.35 | 0.5 | V |
| I_i | Input Current @ Max Input Voltage | $V_{CC} = 5.5V$, $V_{IH} = 7V$ | | | 0.1 | mA |
| I_{IH} | High Level Input Current | $V_{CC} = 5.5V$, $V_{IH} = 2.7V$ | | | 20 | μA |
| I_{IL} | Low Level Input Current | $V_{CC} = 5.5V$, $V_{IL} = 0.4V$ | | -0.1 | -0.50 | mA |
| I_O | Output Drive Current | $V_{CC} = 5.5V$, $V_O = 2.25V$ | -50 | | -150 | mA |
| I_{CC} | Supply Current 303 | $V_{CC} = 5.5V$ | Outputs High | 27 | 60 | mA |
| | | | Outputs Low | 45 | 60 | mA |
| I_{CC} | Supply Current 304 | $V_{CC} = 5.5V$ | Outputs High | 20 | 30 | mA |
| | | | Outputs Low | 42 | 55 | mA |
| I_{CC} | Supply Current | $V_{CC} = 5.5V$ | Outputs High | 35 | 45 | mA |
| | | | Outputs Low | 42 | 55 | mA |
| C_{IN} | Input Capacitance | $V_{CC} = 5V$ | | 5 | | pF |

AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$

| Symbol | Parameter | CGS74B305 | | | CGS64B305 | | | Units |
|--------------------------|---|---|-----|-----|--|-----|-----|-------|
| | | $V_{CC} = 4.5V \text{ to } 5.5V$ $T_A = 0^\circ C \text{ to } 70^\circ C$ $C_L = 0 \text{ pF} - 50 \text{ pF}$ $R_L = 500\Omega$ | | | $V_{CC} = 4.5V \text{ to } 5.5V$ $T_A = -40^\circ C \text{ to } +85^\circ C$ $C_L = 0 \text{ pF} - 50 \text{ pF}$ $R_L = 500\Omega$ | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Input Frequency (Note 2) | 110 | | | 100 | | | MHz |
| t_{PLH} , t_{PHL} | Propagation Delay CLKn to O_n (Note 2) | 4 | | 8.5 | 4 | | 8.5 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay PRE/CLR (Note 2) | 4 | | 11 | 4 | | 11 | ns |
| t_{SU} | Set Up Time before CLK | 5 | | | 5 | | | ns |
| t_w | CLK HI CLK LO CLR/PRE | 4 4 4 | | | 4 4 4 | | | ns |

Extended AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$

| Symbol | Parameter | CGS74B305 | | | CGS64B305 | | | Units |
|----------------------------|--|---|------------|------------|--|------------|------------|-------|
| | | $V_{CC} = 4.5V \text{ to } 5.5V$ $T_A = 0^\circ C \text{ to } 70^\circ C$ $C_L = 0 \text{ pF} - 50 \text{ pF}$ $R_L = 500\Omega$ | | | $V_{CC} = 4.5V \text{ to } 5.5V$ $T_A = -40^\circ C \text{ to } +85^\circ C$ $C_L = 0 \text{ pF} - 50 \text{ pF}$ $R_L = 500\Omega$ | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{OSLH Q}$ | Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2) | | 0.4 | 0.75 | | 0.4 | 0.75 | ns |
| $t_{OSLH Q}$ | Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2) | | 0.4 | 0.75 | | 0.4 | 0.75 | ns |
| $t_{OSHL \bar{Q}}$ | Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2) | | 0.4 | 0.75 | | 0.4 | 0.75 | ns |
| $t_{OSLH \bar{Q}}$ | Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2) | | 0.4 | 0.75 | | 0.4 | 0.75 | ns |
| $t_{OSLH/HL Q, \bar{Q}}$ | Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 2) | | 0.9 | 1.45 | | 0.9 | 1.45 | ns |
| t_{PS} | Maximum Skew Pin (Signal) Transition Variation (Note 1) | PDIP | | 1.45 | | | 1.45 | ns |
| | | SOIC | | 1.45 | | | 1.45 | |
| | | PLCC | | 1.35 | | | 1.35 | |
| t_{rise} , t_{fall} | Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) 0 pF–30 pF Loads (Note 2) | | 1.1 0.9 | 2.0 2.0 | | 1.1 0.9 | 2.0 2.0 | ns |

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 2: This device is sensitive to noise due to the large transient currents which occur during multiple switching of the outputs. V_{CC} bypass capacitor(s), chip types, must be placed as closely as possible to the V_{CC} pin.

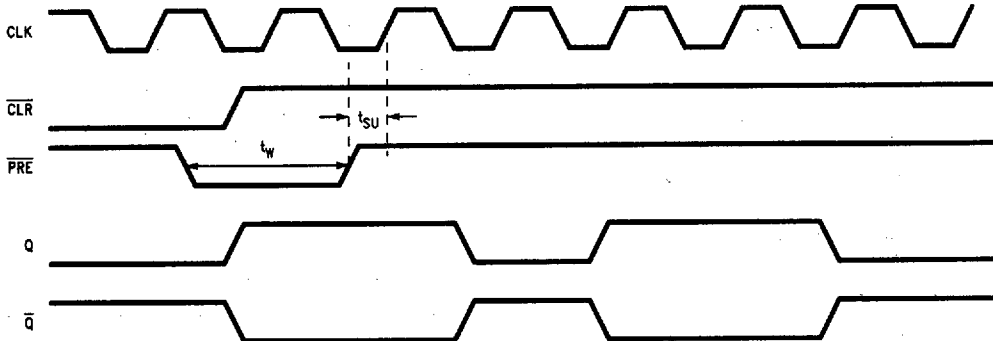
Note 3: Refer to Minimum Skew Parameters Measurement Information Chart for definitions of each skew specification.

Note 4: All input pulses are from 3.5V to 0.3V with rise and fall times of 2.0 ns.

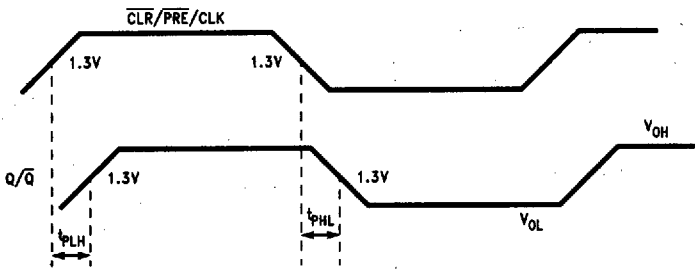
Note 5: Load capacitance includes the test jig.

Timing Diagrams

Minimum Skew Divide-by-2 Clock Drivers
CGS64/74B305

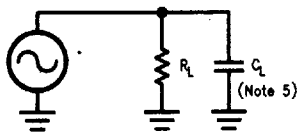


TL/F/11751-4



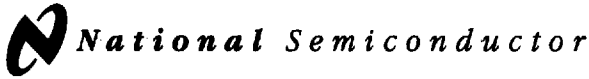
TL/F/11751-5

Test Circuit



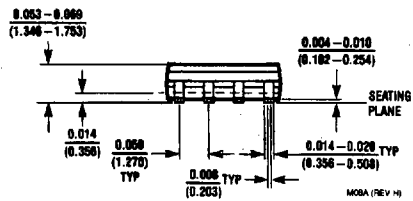
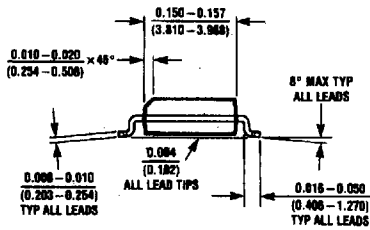
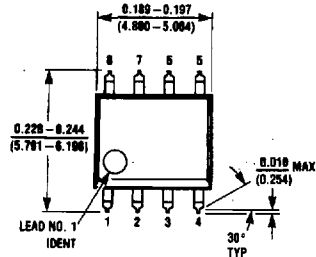
R_L is 500 Ω .
 C_L is 50 pF for all prop delays and skew measurements.
 C_L is 30 pF for t_{rise} and t_{fall} measurements.

TL/F/11751-6



8 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M08A

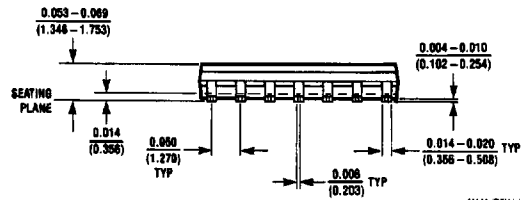
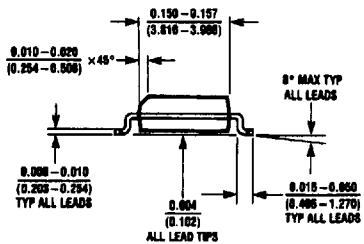
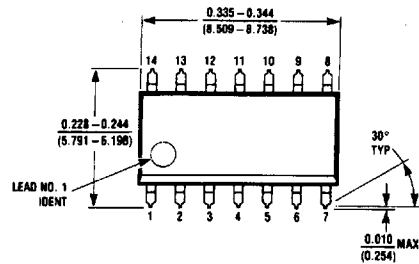
All dimensions are in inches (millimeters)



M08A (REV H)

14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M14A

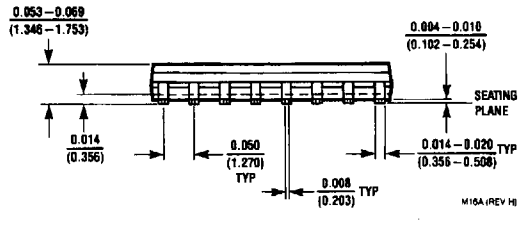
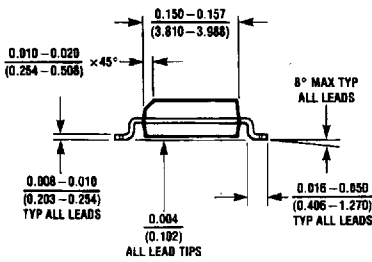
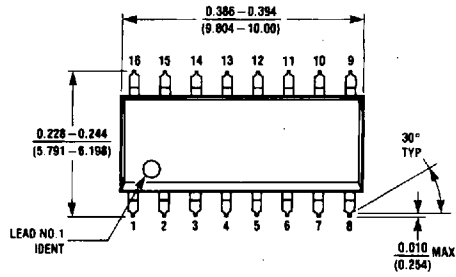
All dimensions are in inches (millimeters)



M14A (REV H)

16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M16A

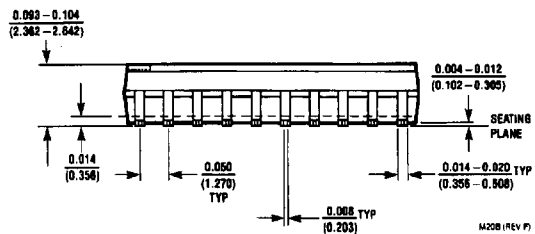
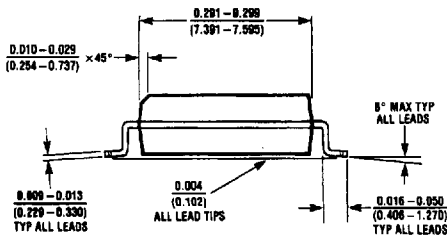
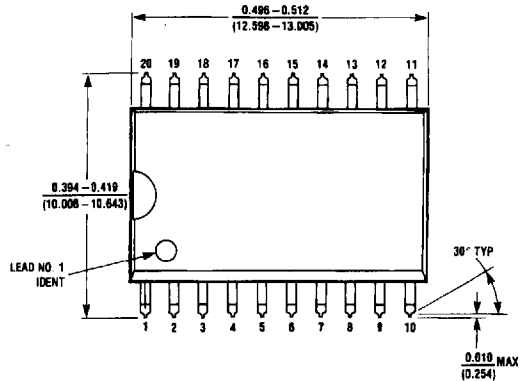
All dimensions are in inches (millimeters)



M16A (REV B)

20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC NS Package Number M20B

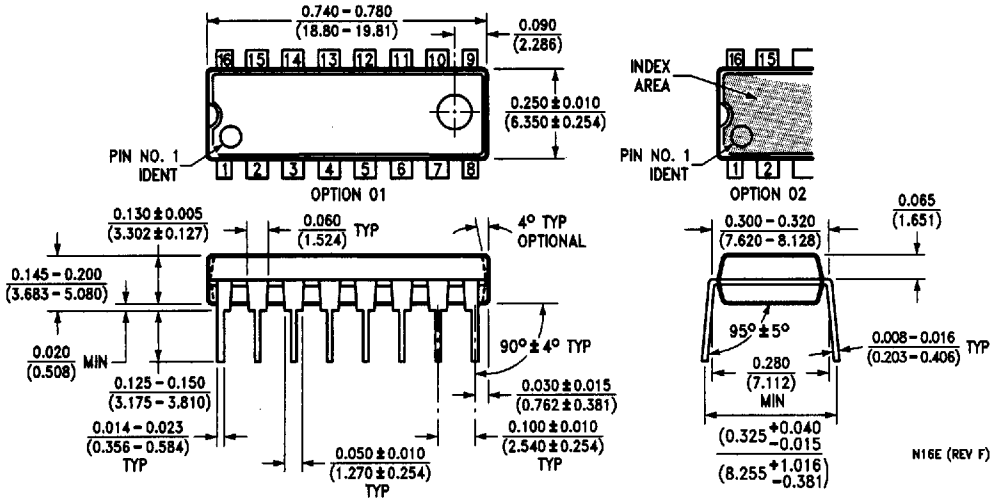
All dimensions are in inches (millimeters)



M20B (REV F)

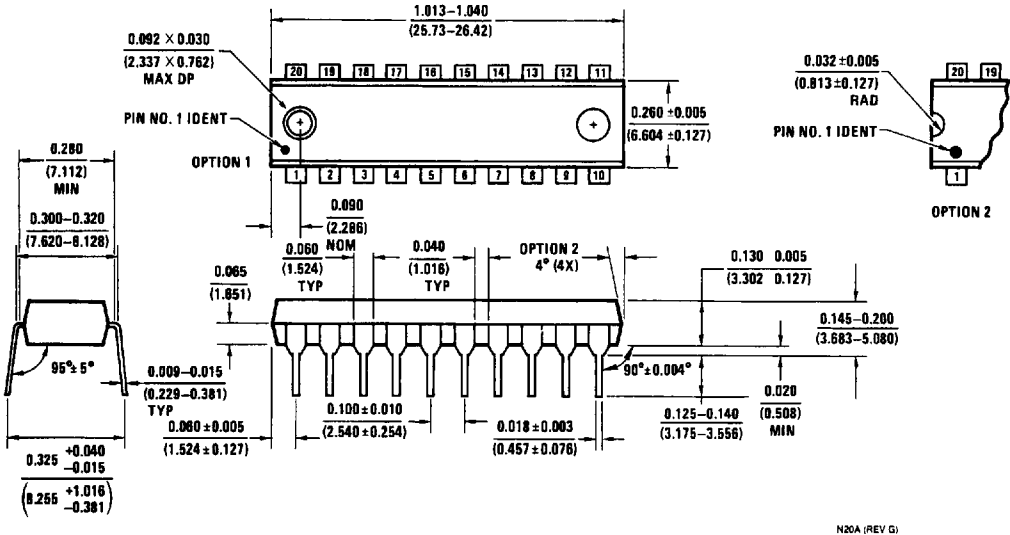
16 Lead (0.300" Wide) Molded Dual-in-Line Package NS Package Number N16E

All dimensions are in inches (millimeters)



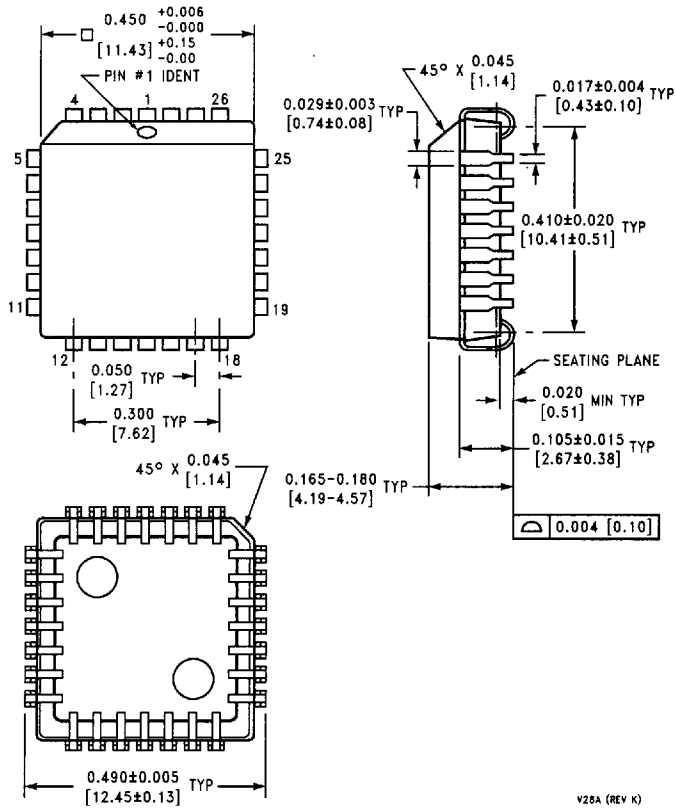
20 Lead (0.300" Wide) Molded Dual-in-Line Package NS Package Number N20A

All dimensions are in inches (millimeters)



28 Lead Molded Plastic Leaded Chip Carrier NS Package Number V28A

All dimensions are in inches [millimeters]



V28A (REV K)