CMOS DUAL J-K FLIP-FLOP

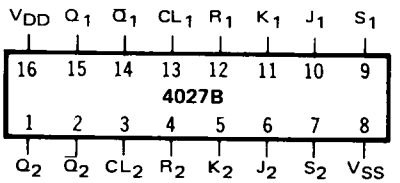
FEATURES

- Individual Set and Reset Controls
- Fully Static Operation
- Logic Edge-Clocked Design
- 8MHz Toggle Rate @ 10Vdc

DESCRIPTION

The 4027B consists of two identical independent CMOS J-K master-slave Flip-Flops. The 4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the Clock pulse. Set and Reset functions are independent of the Clock and are initiated when a high level signal is present at either the Set or Reset input.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

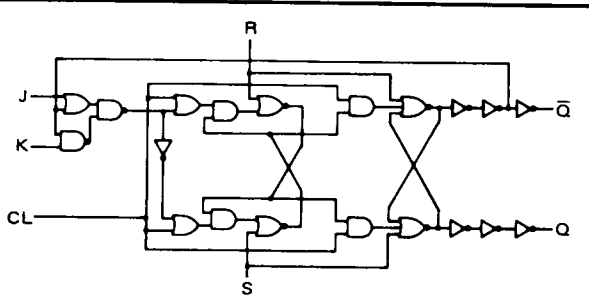
●t_{n-1} INPUTS						†t_n OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\bar{Q}$	
⌐	1	X	0	0	0	1	0	
⌐	X	0	0	0	1	1	0	
⌐	0	X	0	0	0	0	1	
⌐	X	1	0	0	1	0	1	
¬	X	X	0	0	X	(No Change)		
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL
▲ - LEVEL CHANGE
X - DON'T CARE

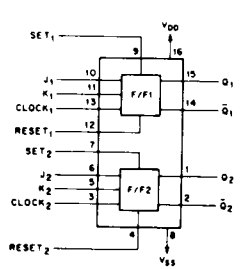
● - t_{n-1} REFERS TO THE INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION

† - t_n REFERS TO THE TIME INTERVAL AFTER THE POSITIVE CLOCK PULSE TRANSITION

LOGIC DIAGRAM (one of two Flip-Flops)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

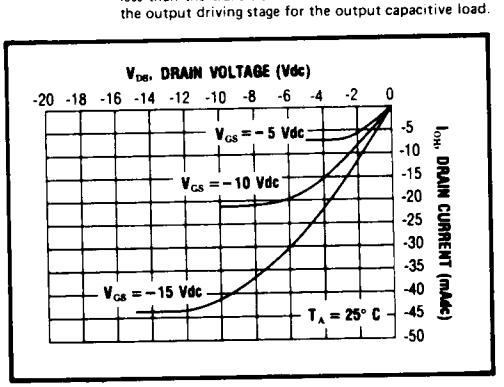
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

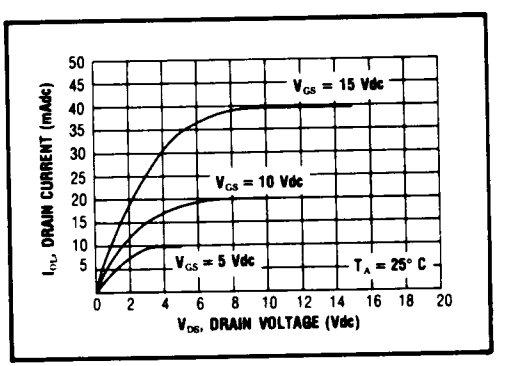
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	165	330	ns
		10	–	60	120	
		15	–	50	100	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	4.0	8.0	–	
		15	5.0	10		
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	3	–	–	
MINIMUM SETUP TIME	t_{setup}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM HOLD TIME	t_{hold}	5	–	-25	0	ns
		10	–	-10	0	
		15	–	-5	0	
SET AND RESET OPERATION						
PROPAGATION DELAY TIME S to Q, R to $\overline{Q}$	t_{PLH}	5	–	150	300	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM SET AND RESET PULSE WIDTH	PW_S, PW_R	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
SET AND RESET REMOVAL TIME	t_{rem}	5	–	0	25	ns
		10	–	0	10	
		15	–	0	5	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics