L8C201/202/203/204
512/1K/2K/4K x 9-bit Asynchronous FIFO

LOGIC DEVICES INCORPORATED

FEATURES

- First-In/First-Out (FIFO) using Dual-Port Memory
- Advanced CMOS Technology
- High Speed — to 10 ns Access Time
- Asynchronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Empty and Full Warning Flags
- Half-Full Flag Capability
- Auto Retransmit Capability
- Package Styles Available:
  - 28-pin Plastic DIP
  - 32-pin Plastic LCC
  - 28-pin Ceramic Flatpack

DESCRIPTION

The **L8C201, L8C202, L8C203,** and **L8C204** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C201 — 512 x 9-bit
L8C202 — 1024 x 9-bit
L8C203 — 2048 x 9-bit
L8C204 — 4096 x 9-bit

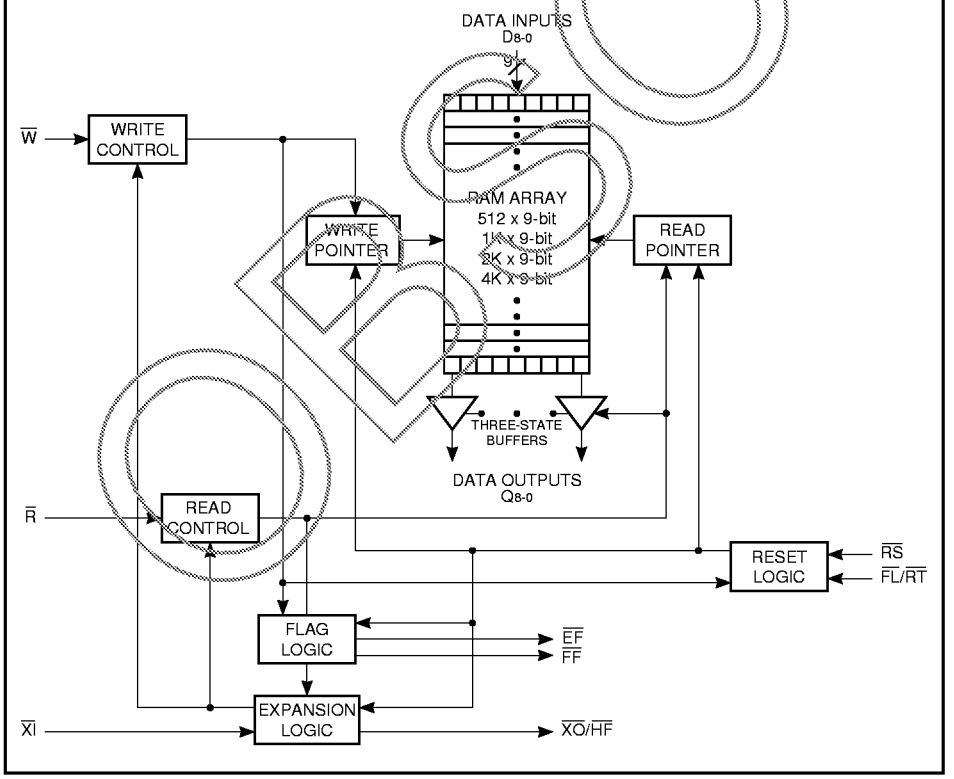
Each device utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty flags are provided to prevent data overflow and underflow. Three additional pins are also provided to allow for unlimited expansion in both word size and depth. Depth Expansion does not result in a flow-through penalty. Multiple devices are connected with the data and control signals in parallel. The active device is determined by the Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals which are daisy chained from device to device.

The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The nine data outputs go to the high impedance state when R is HIGH. Retransmit ($\overline{RT}$) capability allows for reset of the read pointer when $\overline{RT}$ is pulsed LOW, allowing for retransmission of data from the beginning. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data. A Half-Full ($\overline{HF}$) output flag is available in the single device and width expansion modes. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

These FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

The FIFOs are designed for those applications requiring asychronous and simultaneous read/writes in multiprocessing and rate buffer applications.

L8C201/202/203/204 BLOCK DIAGRAM



SIGNAL DEFINITIONS

Inputs

$\overline{RS}$ — Reset

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown (i.e., tWHSH before the rising edge of $\overline{RS}$) and should not change until tSHWL after the rising edge of $\overline{RS}$. Hall-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

$\overline{W}$ — Write Enable

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold time must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after tRHFH, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

$\overline{R}$ — Read Enable

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (D_{8-0}) will return to a high impedance condition until the next read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operating has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after tWHEH and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO.

$\overline{FL}/\overline{RT}$ — First Load/Retransmit

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The FIFOs can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than the full memory has been written between resets. Retransmit will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers. The retransmit feature is not compatible with the Depth Expansion Mode.

$\overline{XI}$ — Expansion In

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

D_{8-0} — Data Input

Data input signals for 9-bit wide data. Data has setup and hold time requirements with respect to the rising edge of $\overline{W}$.

Outputs

$\overline{FF}$ — Full Flag

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 512 writes for the **L8C201**, 1024 writes for the **L8C202**, 2048 writes for the **L8C203**, and 4096 writes for the **L8C204**.

$\overline{EF}$ — Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

$\overline{XO}/\overline{HF}$ — Expansion Out/Half-Full Flag

This is a dual-purpose output. In the Single Device Mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then deasserted by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the daisy chain by providing a pulse to the next device when the previous device reaches the last location of memory.

Q_{8-0} — Data Output

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read Enable ($\overline{R}$) is in a HIGH state or the device is empty.

OPERATING MODES

Single Device Mode

A single FIFO may be used when the application requirements are for the number of words in a single device. The FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. In this mode the Half-Full Flag ($\overline{HF}$), which is an active-low output, is the active function of the combination pin $\overline{XO}$/$\overline{HF}$.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be detected from any one device. Any word width can be attained by adding additional FIFOs. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. **Do not connect any output signals together.**

Depth Expansion (Daisy Chain) Mode

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. Any depth can be attained by adding additional FIFOs. The FIFOs operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device with the last device connecting back to the first.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing FIFOs. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device when $\overline{W}$ is used; $\overline{EF}$ is monitored on the device when $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	L8C201/202/203/204 Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–0.5		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}			±1	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}			±10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	All Inputs = V_{IH} MIN (Note 6)			15	mA
I_{CC3}	V_{CC} Current, CMOS Standby	All Inputs = V_{CC} (Note 12)			5	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 9)			7	pF

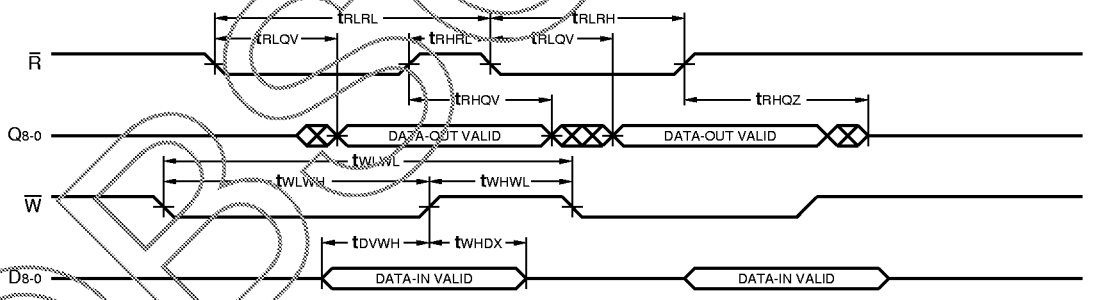
Symbol	Parameter	Test Condition	L8C201/202/203/204- 40	30	25	20	15	12	10	Unit
I_{CC1}	V_{CC} Current, Active	(Note 5)	90	95	100	110	120	150	180	mA

SWITCHING CHARACTERISTICS *Over Commercial and Industrial Operating Range*

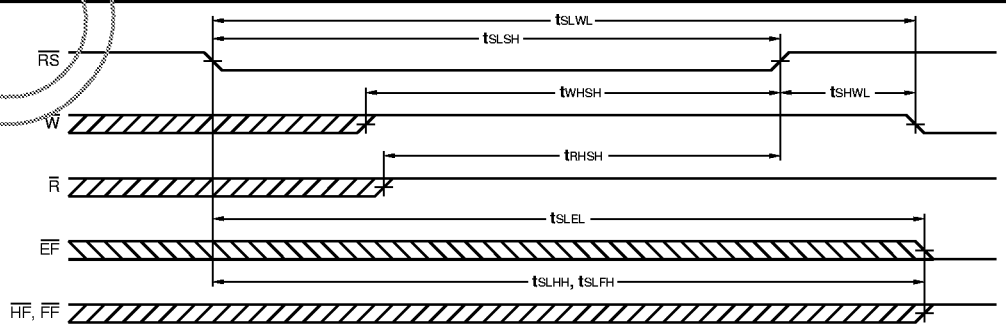
ASYNCHRONOUS AND RESET TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RLRL}	Read Cycle Time (MHz)	35		25		20		15	
t_{RLQV}	Read Low to Output Valid (Access Time)		25		15		12		10
t_{RHRL}	Read High to Read Low (Notes 8, 9)	10		10		8		5	
t_{RLRH}	Read Low to End of Read Cycle (Notes 8, 9)	25		15		12		10	
t_{RHQV}	Read High to Output Valid	5		5		5		5	
t_{RHQZ}	Read High to Output High Z (Note 14)		20		15		15		15
t_{WLWL}	Write Cycle Time (Note 9)	35		25		20		15	
t_{WLWH}	Write Low to Write High (Notes 8, 9)	25		15		12		10	
t_{WHWL}	Write High to End of Write Cycle (Notes 8, 9)	10		10		8		5	
t_{DVWH}	Data Valid to Write High (Notes 8, 9)	15		10		8		8	
t_{WHDX}	Write High to Data Change (Notes 8, 9)	0		0		0		0	
t_{SLSH}	Reset Cycle Time (Notes 9, 10)	25		15		12		10	
t_{SLWL}	Reset Low to Write Low (Notes 9, 10)	35		25		20		15	
t_{WHSH}	Write High to Reset High (Notes 9, 10)	25		15		12		10	
t_{RHSH}	Read High to Reset High (Notes 9, 10)	25		15		12		10	
t_{SHWL}	Reset High to Write Low (Notes 9, 10)	10		10		8		5	
t_{SLEL}	Reset Low to Empty Flag Low		25		15		12		10
t_{SLHH}	Reset Low to Half-Full Flag High		25		15		12		10
t_{SLFH}	Reset Low to Full Flag High		25		15		12		10

ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING

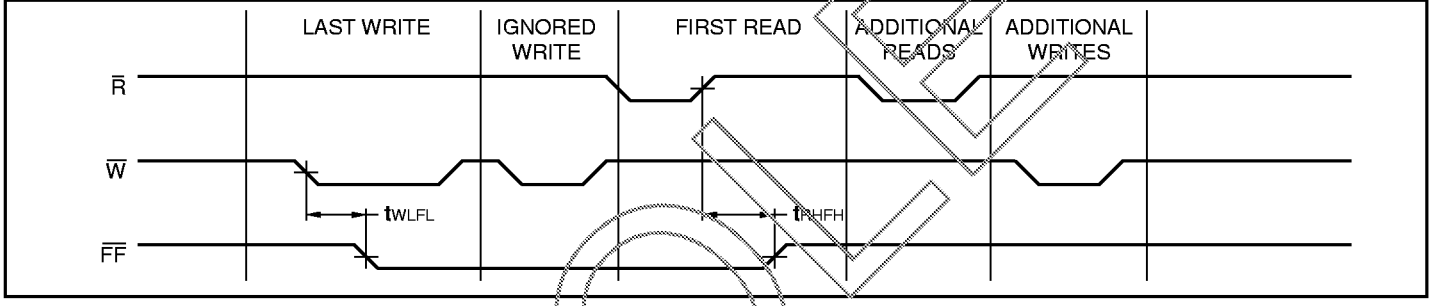


SWITCHING CHARACTERISTICS *Over Commercial and Industrial Operating Range*

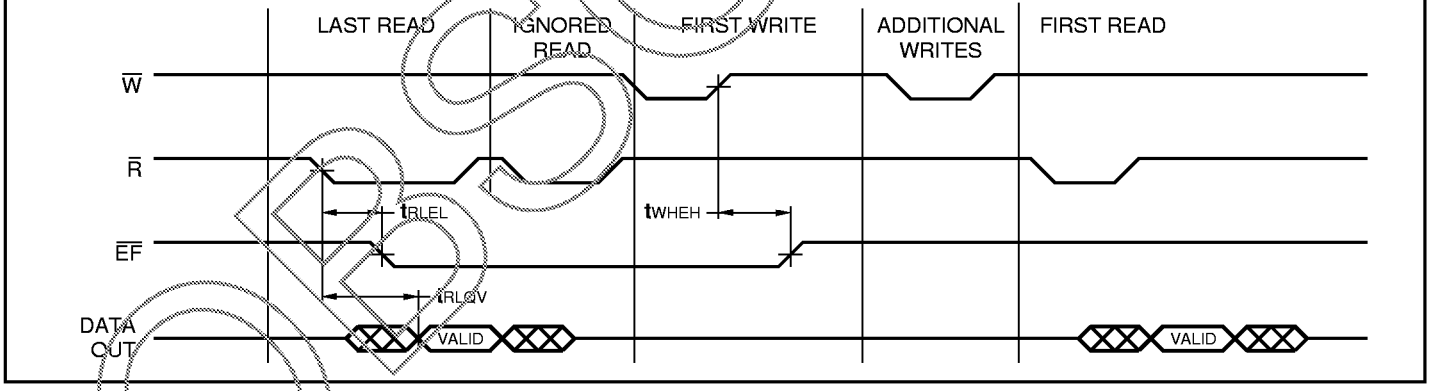
FULL/EMPTY FLAG AND RETRANSMIT TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RLQV}	Read Low to Output Valid (Access Time)		25		15		12		10
t_{RLEL}	Read Low to Empty Flag Low		25		15		12		10
t_{RHFH}	Read High to Full Flag High		25		15		12		10
t_{WHEH}	Write High to Empty Flag High		25		15		12		10
t_{WLFL}	Write Low to Full Flag Low		25		15		12		10
t_{TLAL}	Retransmit Cycle Time	35		25		20		15	
t_{TLTH}	Retransmit Low to End of Retransmit Cycle (Notes 8, 9, 10)	25		15		12		10	
t_{AHTH}	Read/Write High to Retransmit High (Notes 8, 9, 10)	25		15		12		10	
t_{THAL}	Retransmit High to Read/Write Low (Note 9)	10		10		8		5	

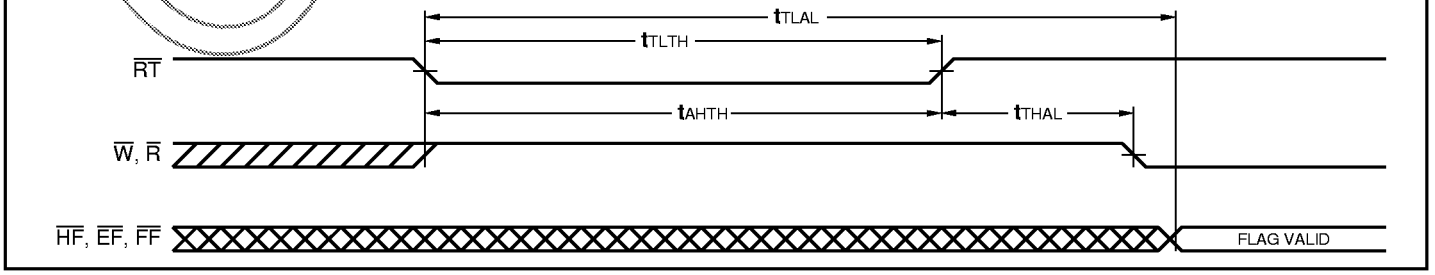
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT

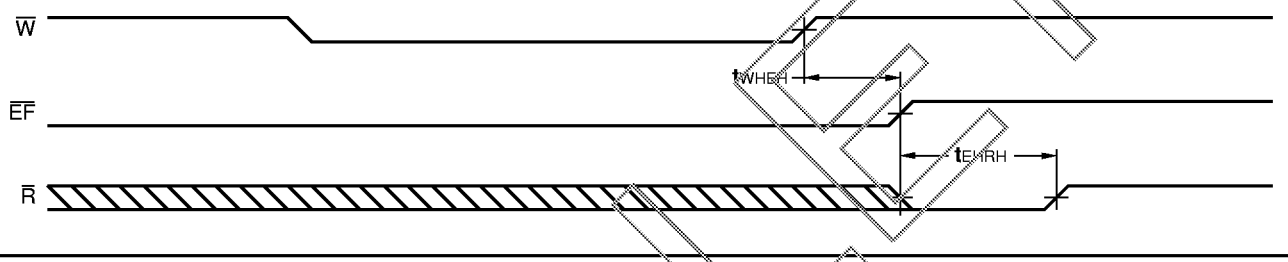


SWITCHING CHARACTERISTICS *Over Commercial and Industrial Operating Range*

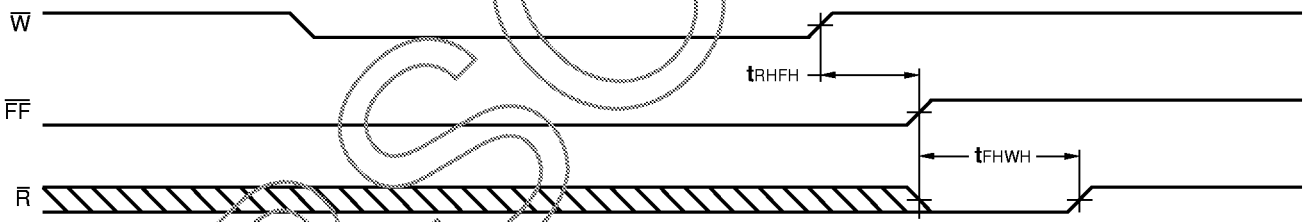
FULL/HALF-FULL/EMPTY FLAG TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RHFH}	Read High to Full Flag High		25		15		12		10
t_{EHRH}	Read Pulse Width After Empty Flag High	25		15		12		10	
t_{RHHH}	Read High to Half-Full Flag High		25		15		12		10
t_{WHEH}	Write High to Empty Flag High		25		15		12		10
t_{WLHL}	Write Low to Half-Full Flag Low		25		15		12		10
t_{FHWH}	Write Pulse Width After Full Flag High (Note 9)	25		15		12		10	

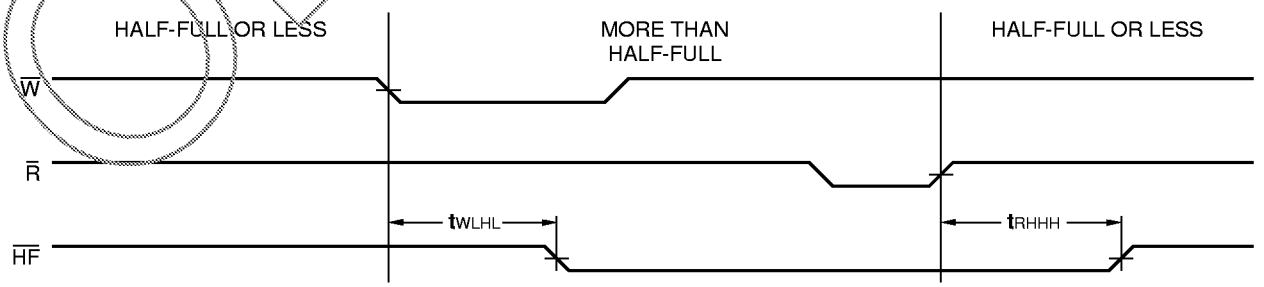
EMPTY FLAG TIMING



FULL FLAG TIMING



HALF-FULL FLAG TIMING

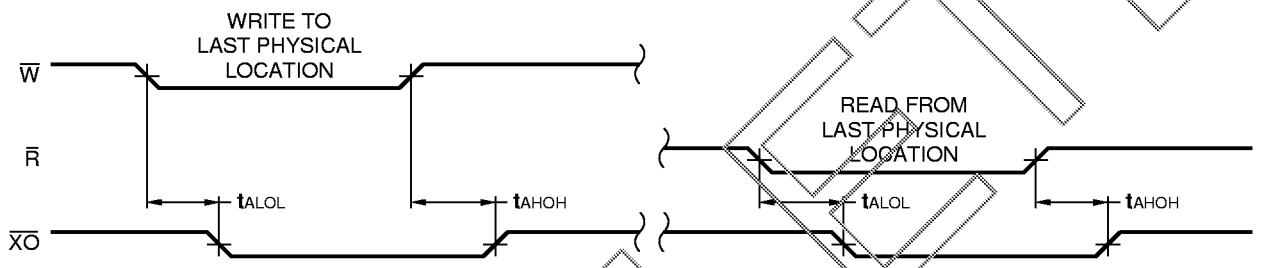


SWITCHING CHARACTERISTICS *Over Commercial and Industrial Operating Range*

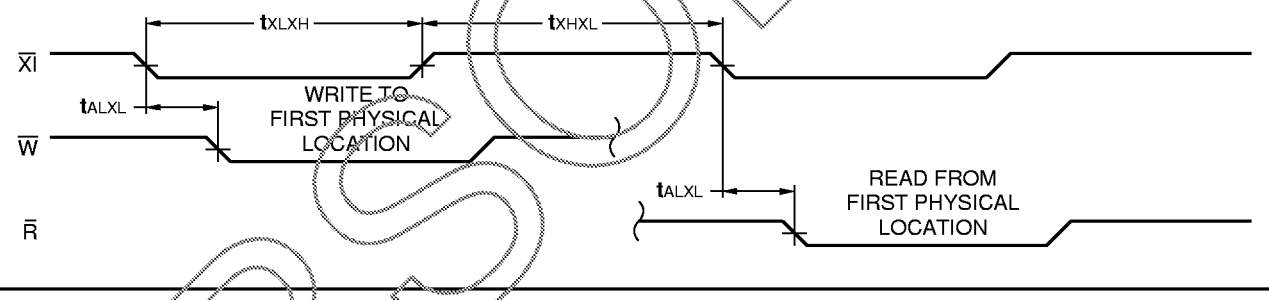
EXPANSION TIMING *(ns)*

		L8C201/202/203/204–							
		25		15		12		10	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{ALOL}	Read/Write to Expansion Out Low (Note 11)		25		15		12		12
t_{AHOH}	Read/Write to Expansion Out High (Note 11)		25		15		12		12
t_{XLXH}	Expansion In Pulse Width (Notes 9, 11)	25		15		12		10	
t_{XHXL}	Expansion In High to Expansion In Low (Notes 9, 11)	10		10		10		10	
t_{ALXL}	Read/Write Low to Expansion In Low (Notes 9, 11)	15		12		8		8	

EXPANSION OUT



EXPANSION IN

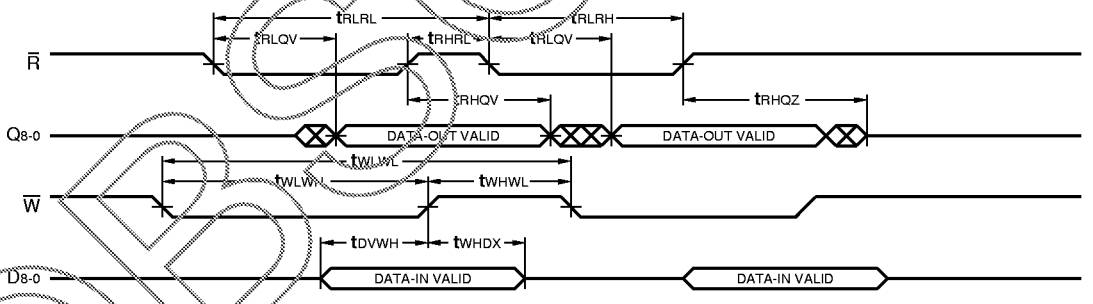


SWITCHING CHARACTERISTICS *Over Military Operating Range*

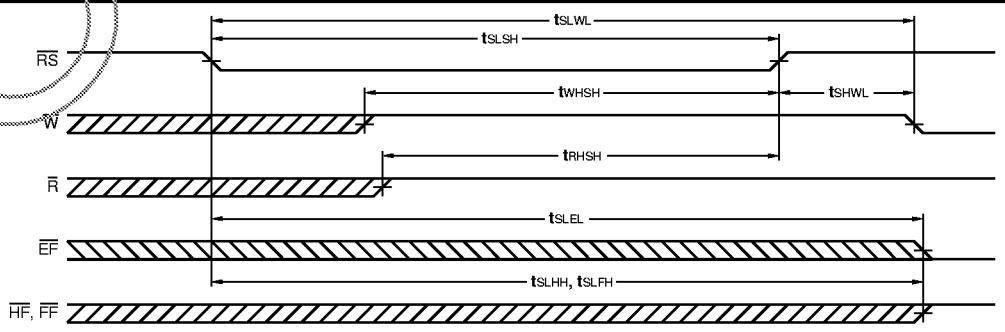
ASYNCHRONOUS AND RESET TIMING *(ns)*

		L8C201/202/203/204–					
		40		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{RLRL}	Read Cycle Time (MHz)	50		40		30	
t_{RLQV}	Read Low to Output Valid (Access Time)		40		30		20
t_{RHRL}	Read High to Read Low (Notes 8, 9)	10		10		10	
t_{RLRH}	Read Low to End of Read Cycle (Notes 8, 9)	40		30		20	
t_{RHQV}	Read High to Output Valid	5		5		5	
t_{RHQZ}	Read High to Output High Z (Note 14)		25		20		15
t_{WLWL}	Write Cycle Time (Note 9)	50		40		30	
t_{WLWH}	Write Low to Write High (Notes 8, 9)	40		30		20	
t_{WHWL}	Write High to End of Write Cycle (Notes 8, 9)	10		10		10	
t_{DVWH}	Data Valid to Write High (Notes 8, 9)	20		18		12	
t_{WHDX}	Write High to Data Change (Notes 8, 9)	0		0		0	
t_{SLSH}	Reset Cycle Time (Notes 9, 10)	40		30		20	
t_{SLWL}	Reset Low to Write Low (Notes 9, 10)	50		40		30	
t_{WHSH}	Write High to Reset High (Notes 9, 10)	40		30		20	
t_{RHSH}	Read High to Reset High (Notes 9, 10)	40		30		20	
t_{SHWL}	Reset High to Write Low (Notes 9, 10)	10		10		10	
t_{SLEL}	Reset Low to Empty Flag Low		50		40		30
t_{SLHH}	Reset Low to Half-Full Flag High		50		40		30
t_{SLFH}	Reset Low to Full Flag High		50		40		30

ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING

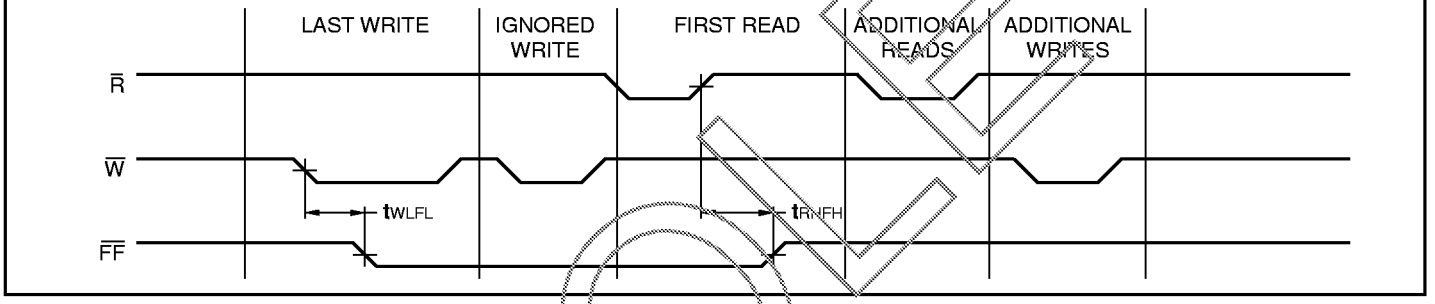


SWITCHING CHARACTERISTICS *Over Military Operating Range*

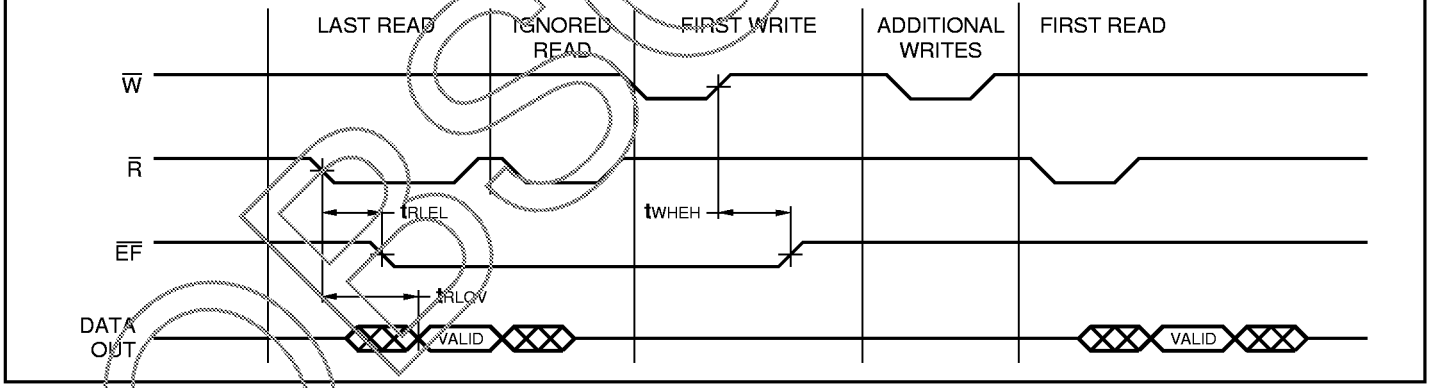
FULL/EMPTY FLAG AND RETRANSMIT TIMING *(ns)*

		L8C201/202/203/204–					
		40		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{RLQV}	Read Low to Output Valid (Access Time)		40		30		20
t_{RLEL}	Read Low to Empty Flag Low		30		30		20
t_{RHFH}	Read High to Full Flag High		35		30		20
t_{WHEH}	Write High to Empty Flag High		35		30		20
t_{WLFL}	Write Low to Full Flag Low		35		30		20
t_{TLAL}	Retransmit Cycle Time	50		40		30	
t_{TLTH}	Retransmit Low to End of Retransmit Cycle (Notes 8, 9, 10)	40		30		20	
t_{AHTH}	Read/Write High to Retransmit High (Notes 8, 9, 10)	40		30		20	
t_{THAL}	Retransmit High to Read/Write Low (Note 9)	10		10		10	

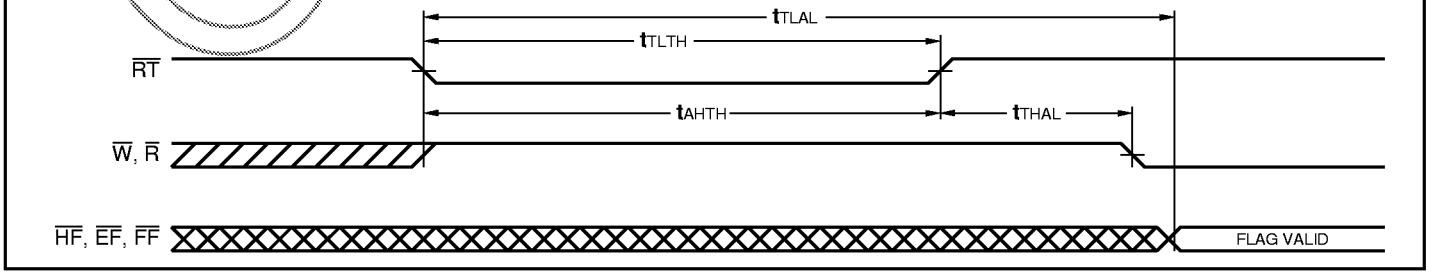
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT

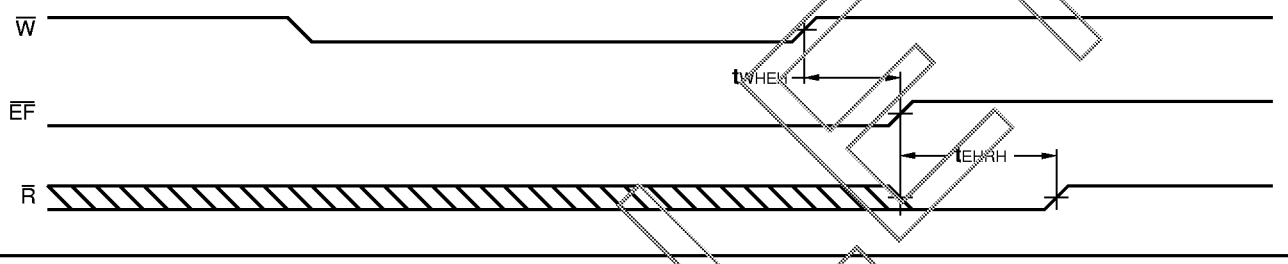


SWITCHING CHARACTERISTICS *Over Military Operating Range*

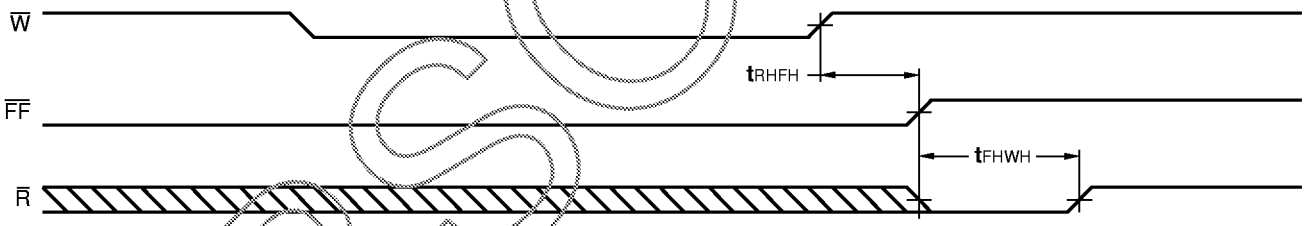
FULL/HALF-FULL/EMPTY FLAG TIMING *(ns)*

		L8C201/202/203/204–					
		40		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{RHFH}	Read High to Full Flag High		35		30		20
t_{EHRH}	Read Pulse Width After Empty Flag High	40		30		20	
t_{RHHH}	Read High to Half-Full Flag High		50		40		30
t_{WHEH}	Write High to Empty Flag High		35		30		20
t_{WLHL}	Write Low to Half-Full Flag Low		50		40		30
t_{FHWH}	Write Pulse Width After Full Flag High (Note 9)	40		30		20	

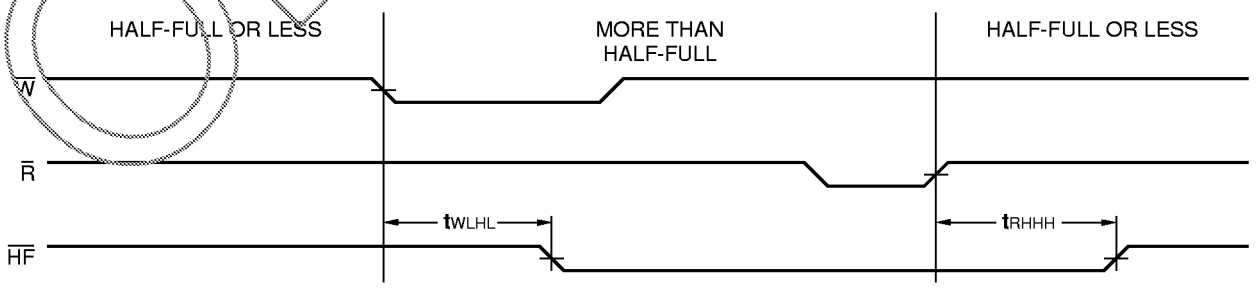
EMPTY FLAG TIMING



FULL FLAG TIMING



HALF-FULL FLAG TIMING

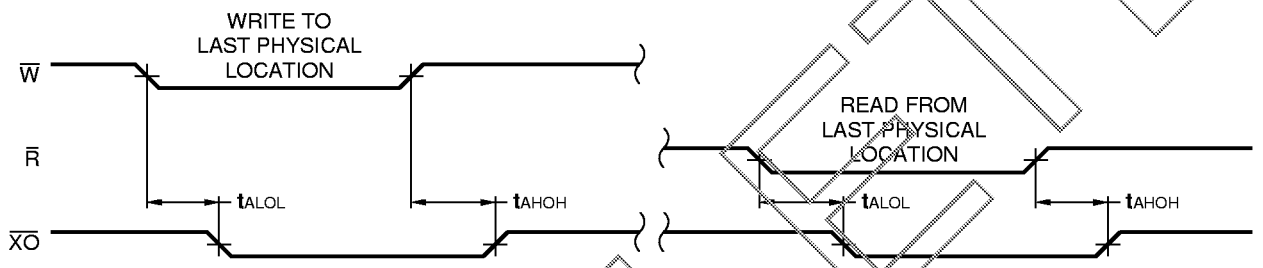


SWITCHING CHARACTERISTICS *Over Military Operating Range*

EXPANSION TIMING *(ns)*

Symbol	Parameter	L8C201/202/203/204– 40 Min	40 Max	30 Min	30 Max	20 Min	20 Max
t_{ALOL}	Read/Write to Expansion Out Low (Note 11)		40		30		20
t_{AHOH}	Read/Write to Expansion Out High (Note 11)		40		30		20
t_{XLXH}	Expansion In Pulse Width (Notes 9, 11)	40		30		20	
t_{XHXL}	Expansion In High to Expansion In Low (Notes 9, 11)	10		10		10	
t_{ALXL}	Read/Write Low to Expansion In Low (Notes 9, 11)	10		10		10	

EXPANSION OUT



EXPANSION IN

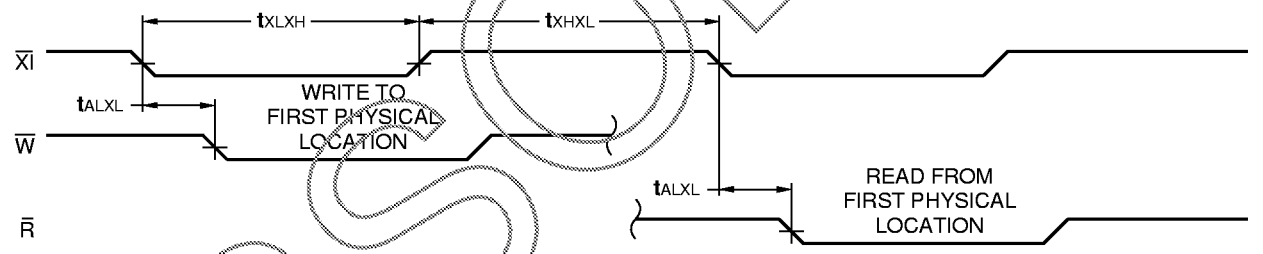


FIGURE 1. FIFO MEMORY (DEPTH EXPANSION) BLOCK DIAGRAM

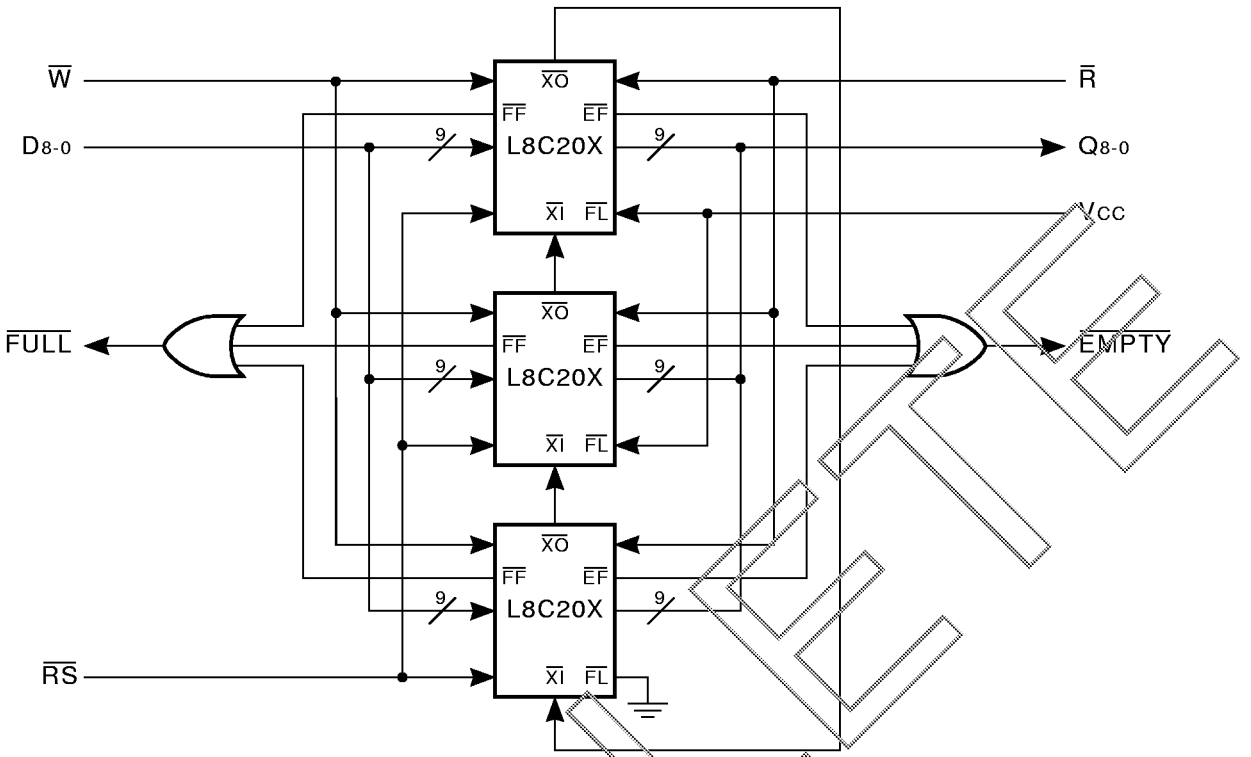


TABLE 1. RESET AND RETRANSMIT *(SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE)*

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X

TABLE 2. RESET AND FIRST LOAD TRUTH TABLE *(DEPTH EXPANSION/COMPOUND EXPANSION MODE)*

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Others	0	1	(1)	Location Zero Disabled	Location Zero Disabled	0	1
Read/Write	1	(2)	(1)	X	X	X	X

(1) See Figure 1 (Depth Expansion Block Diagram)
(2) Unchanged

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. "Typical" supply current values are not shown but may be approximated. At a V_{CC} of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

5. Tested with outputs open and data inputs changing at the specified read and write cycle rate. The device is neither full or empty for the test.

6. Tested with outputs open in the worst static input control signal combination (i.e., $\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{FL}$, and $\overline{RS}$).

7. These parameters are guaranteed but not 100% tested.

8. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH}, plus 30 pF (Fig. 2a), and input pulse levels of 0 to 3.0 V (Fig. 3).

9. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RLRH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

10. When cascading devices, the reset pulse width must be increased to equal t_{SLSH} + t_{SLHH}.

11. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

12. Tested with output open and $\overline{RS}$ = $\overline{FL}$ = $\overline{XI}$ = $\overline{R}$ = $\overline{W}$ = V_{CC}.

13. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

14. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 2b. This parameter is sampled and not 100% tested.

15. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 2a.

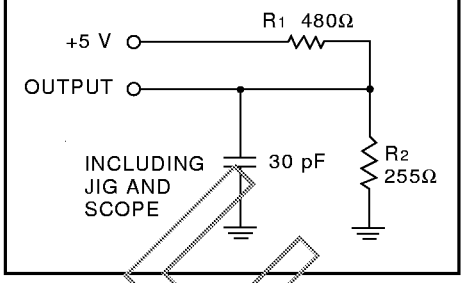


FIGURE 2b.

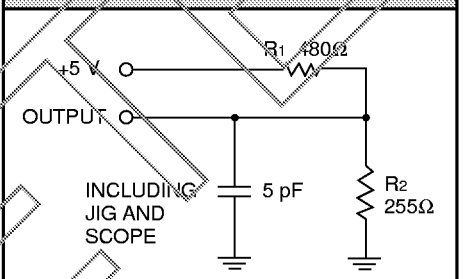
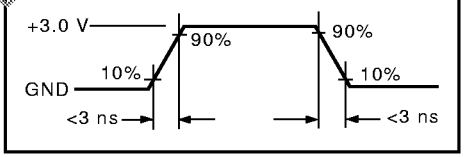
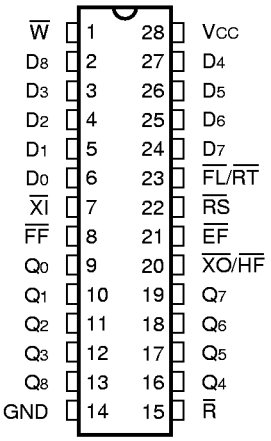


FIGURE 3.

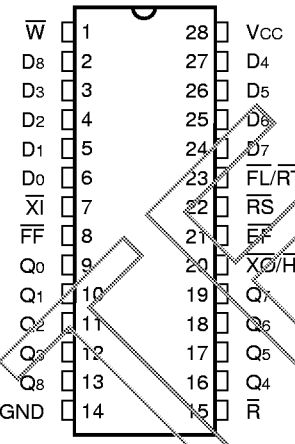


L8C201 — ORDERING INFORMATION

28-pin — 0.3" wide



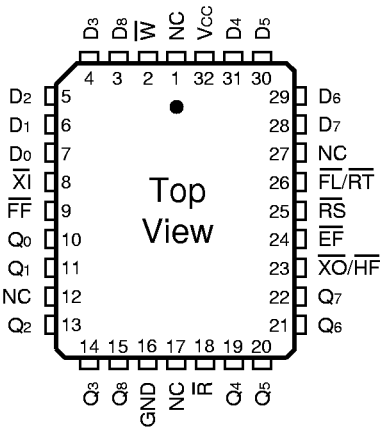
28-pin — 0.6" wide



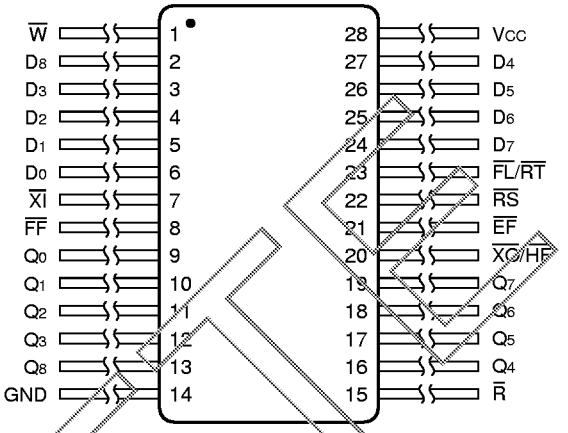
Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C201PC25	L8C201NC25
15 ns	L8C201PC15	L8C201NC15
12 ns	L8C201PC12	L8C201NC12
10 ns	L8C201PC10	L8C201NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C201PI25	L8C201NI25
15 ns	L8C201PI15	L8C201NI15
12 ns	L8C201PI12	L8C201NI12
10 ns	L8C201PI10	L8C201NI10

L8C201 — ORDERING INFORMATION

32-pin — 0.490" x 0.590"



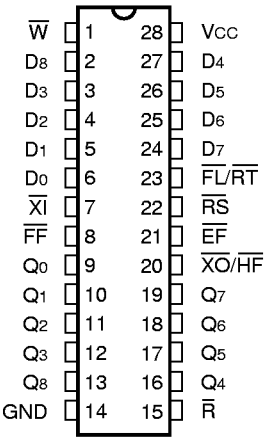
28-pin



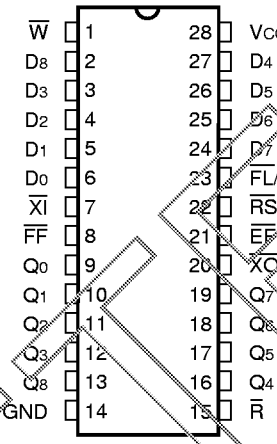
Speed	Plastic J-Lead Chip Carrier (J6)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L8C201JC25	
15 ns	L8C201JC15	
12 ns	L8C201JC12	
10 ns	L8C201JC10	
	–40°C to +85°C — Commercial Screening	
25 ns	L8C201JI25	
15 ns	L8C201JI15	
12 ns	L8C201JI12	
10 ns	L8C201JI10	
	–55°C to +125°C — Commercial Screening	
40 ns		L8C201MM40
30 ns		L8C201MM30
20 ns		L8C201MM20
	–55°C to +125°C — MIL-STD-883 Compliant	
40 ns		L8C201MMB40
30 ns		L8C201MMB30
20 ns		L8C201MMB20

L8C202 — ORDERING INFORMATION

28-pin — 0.3" wide



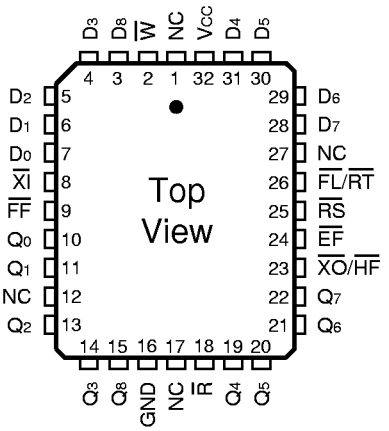
28-pin — 0.6" wide



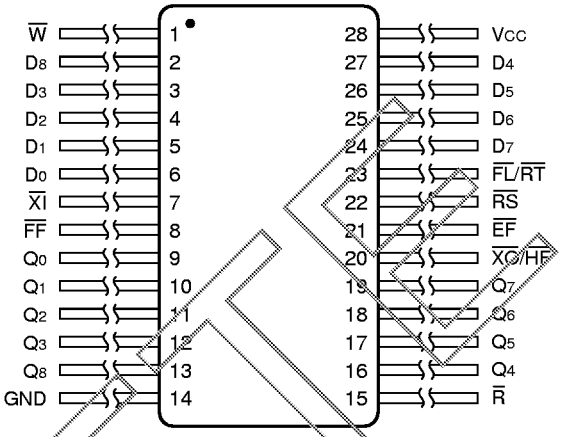
Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C202PC25	L8C202NC25
15 ns	L8C202PC15	L8C202NC15
12 ns	L8C202PC12	L8C202NC12
10 ns	L8C202PC10	L8C202NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C202PI25	L8C202NI25
15 ns	L8C202PI15	L8C202NI15
12 ns	L8C202PI12	L8C202NI12
10 ns	L8C202PI10	L8C202NI10

L8C202 — ORDERING INFORMATION

32-pin — 0.490" x 0.590"



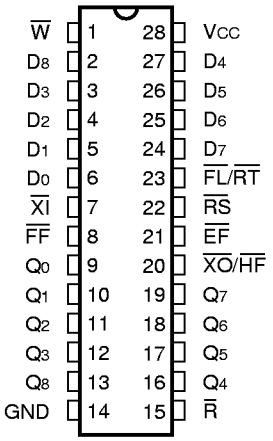
28-pin



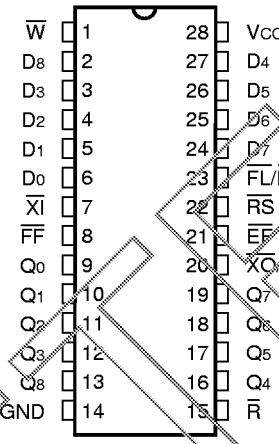
Speed	Plastic J-Lead Chip Carrier (J6)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L8C202JC25	
15 ns	L8C202JC15	
12 ns	L8C202JC12	
10 ns	L8C202JC10	
	–40°C to +85°C — Commercial Screening	
25 ns	L8C202JI25	
15 ns	L8C202JI15	
12 ns	L8C202JI12	
10 ns	L8C202JI10	
	–55°C to +125°C — Commercial Screening	
40 ns		L8C202MM40
30 ns		L8C202MM30
20 ns		L8C202MM20
	–55°C to +125°C — MIL-STD-883 Compliant	
40 ns		L8C202MMB40
30 ns		L8C202MMB30
20 ns		L8C202MMB20

L8C203 — ORDERING INFORMATION

28-pin — 0.3" wide



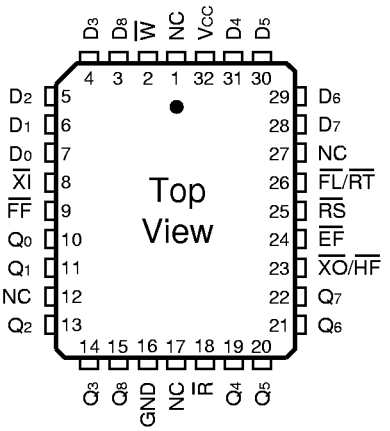
28-pin — 0.6" wide



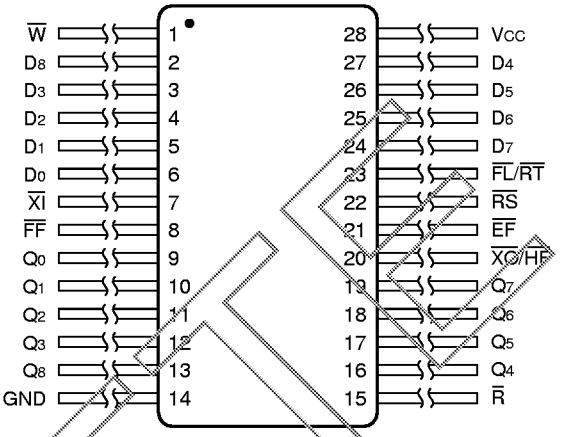
Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C203PC25	L8C203NC25
15 ns	L8C203PC15	L8C203NC15
12 ns	L8C203PC12	L8C203NC12
10 ns	L8C203PC10	L8C203NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C203PI25	L8C203NI25
15 ns	L8C203PI15	L8C203NI15
12 ns	L8C203PI12	L8C203NI12
10 ns	L8C203PI10	L8C203NI10

L8C203 — ORDERING INFORMATION

32-pin — 0.490" x 0.590"



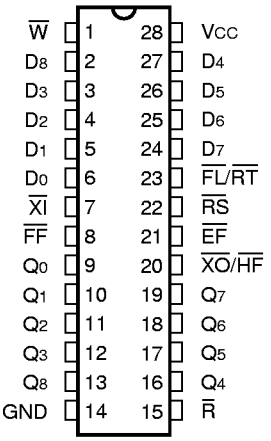
28-pin



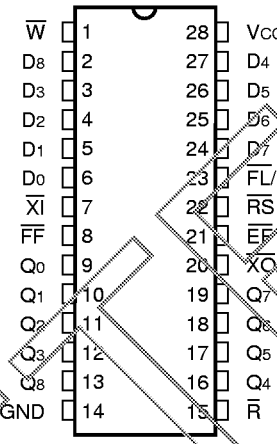
Speed	Plastic J-Lead Chip Carrier (J6)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L8C203JC25	
15 ns	L8C203JC15	
12 ns	L8C203JC12	
10 ns	L8C203JC10	
	–40°C to +85°C — Commercial Screening	
25 ns	L8C203JI25	
15 ns	L8C203JI15	
12 ns	L8C203JI12	
10 ns	L8C203JI10	
	–55°C to +125°C — Commercial Screening	
40 ns		L8C203MM40
30 ns		L8C203MM30
20 ns		L8C203MM20
	–55°C to +125°C — MIL-STD-883 Compliant	
40 ns		L8C203MMB40
30 ns		L8C203MMB30
20 ns		L8C203MMB20

L8C204 — ORDERING INFORMATION

28-pin — 0.3" wide



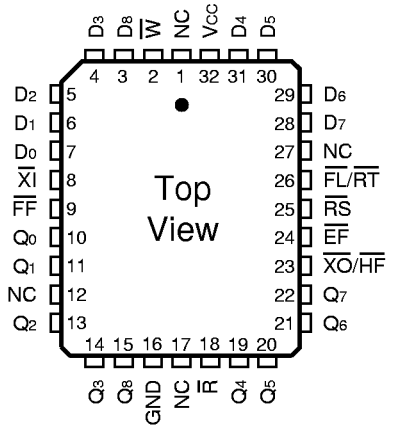
28-pin — 0.6" wide



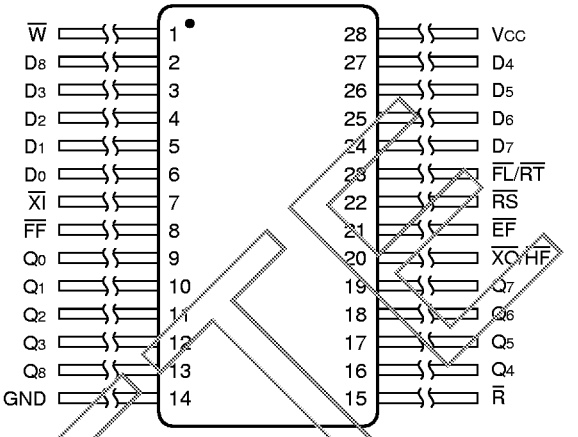
Speed	Plastic DIP (P10)	Plastic DIP (P9)
	0°C to +70°C — Commercial Screening	
25 ns	L8C204PC25	L8C204NC25
15 ns	L8C204PC15	L8C204NC15
12 ns	L8C204PC12	L8C204NC12
10 ns	L8C204PC10	L8C204NC10
	–40°C to +85°C — Commercial Screening	
25 ns	L8C204PI25	L8C204NI25
15 ns	L8C204PI15	L8C204NI15
12 ns	L8C204PI12	L8C204NI12
10 ns	L8C204PI10	L8C204NI10

L8C204 — ORDERING INFORMATION

32-pin — 0.490" x 0.590"



28-pin



Speed	Plastic J-Lead Chip Carrier (J6)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
25 ns	L8C204JC25	
15 ns	L8C204JC15	
12 ns	L8C204JC12	
10 ns	L8C204JC10	
	–40°C to +85°C — Commercial Screening	
25 ns	L8C204JI25	
15 ns	L8C204JI15	
12 ns	L8C204JI12	
10 ns	L8C204JI10	
	–55°C to +125°C — Commercial Screening	
40 ns		L8C204MM40
30 ns		L8C204MM30
20 ns		L8C204MM20
	–55°C to +125°C — MIL-STD-883 Compliant	
40 ns		L8C204MMB40
30 ns		L8C204MMB30
20 ns		L8C204MMB20