High Speed CMOS Bus Interface 8, 9 & 10-bit Latches

QS54/74FCT841T
QS54/74FCT843T
QS54/74FCT845T

QS54/74FCT2841T
QS54/74FCT2843T
QS54/74FCT2845T

FEATURES/BENEFITS

- Pin and function compatible to the Am29841/3/5 74FCT 841/3/5 and 74FCT841T/3T/5T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot Clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 841T, 843T, 845T

- JEDEC-FCT spec compatible
- Fastest CMOS Logic family Available
- A, B and C speed grades with 5.5ns tPD for C
- Iol = 48 mA Com, 32 mA Mil

FCT-T 2841T, 2843T, 2845T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B and C speed grades with 5.5ns tPD for C
- Iol = 12mA Com

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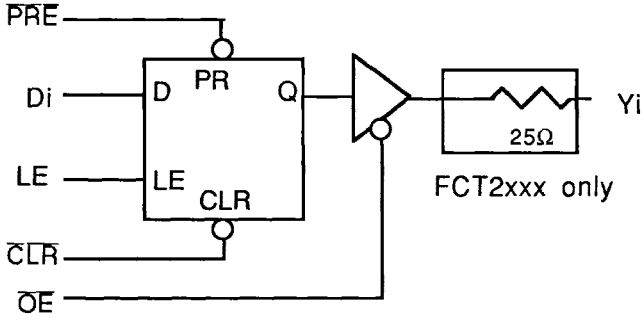
DESCRIPTION

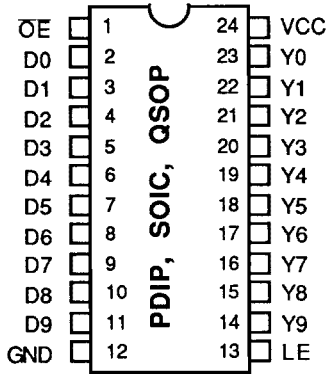
The QSFCT841T, 843T, and 845T are 10, 9, and 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The devices come in A, B, and C speed grades with 5.5ns (Max.) tPLH/tPHL for the C grade. The 2841/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 284x eliminate the need for external series resistor in high speed systems and can replace the 84x series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression , and outputs will not load an active bus when Vcc is removed from the device.

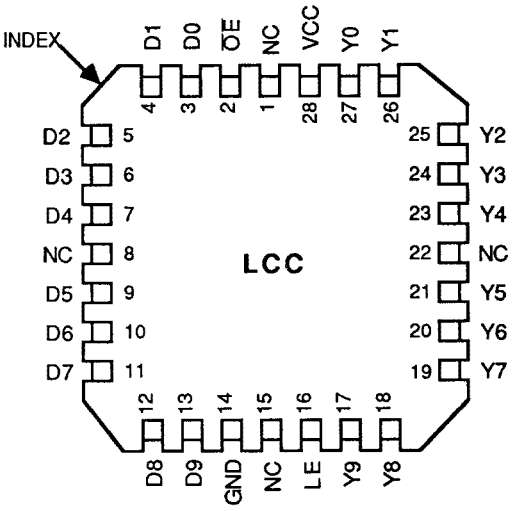
FUNCTIONAL BLOCK DIAGRAM

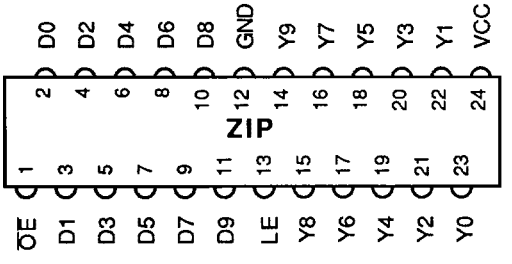


PINOUTS

FCT841 PIN CONFIGURATIONS

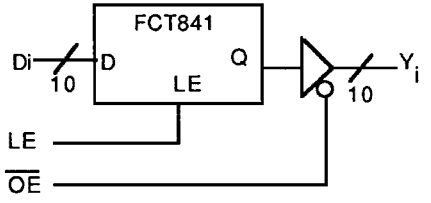






• ALL PINS TOP VIEW

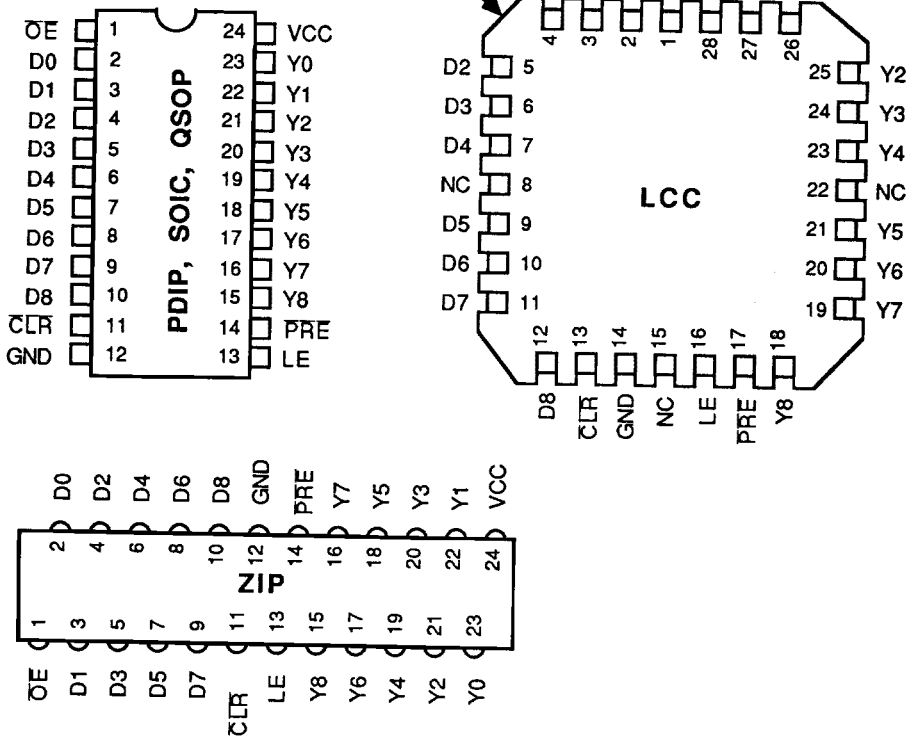
FCT841 LOGIC SYMBOL



PIN DESCRIPTIONS

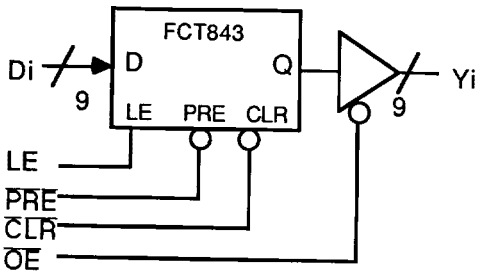
Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

FCT843 PIN CONFIGURATIONS



• ALL PINS TOP VIEW

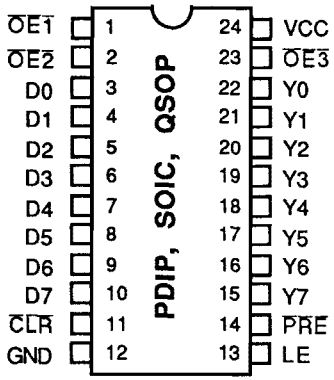
FCT843 LOGIC SYMBOL

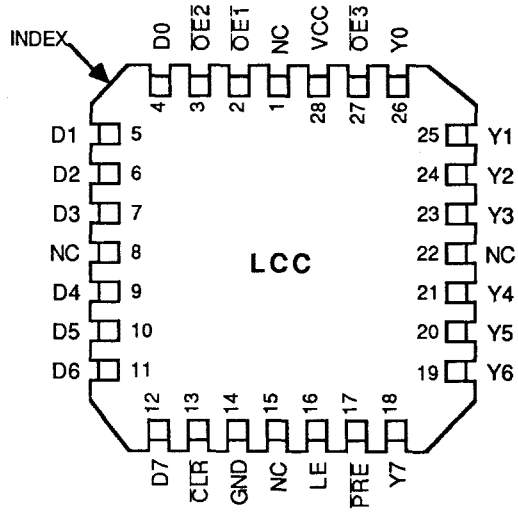


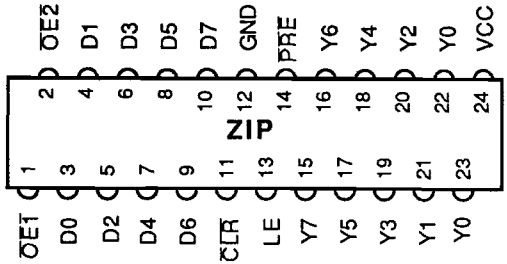
PIN DESCRIPTIONS

Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
$\overline{OE}$	I	Output Enable
LE	I	Latch Enable
$\overline{PRE}$	I	Preset
$\overline{CLR}$	I	Asynchronous Reset

FCT845 PIN CONFIGURATIONS

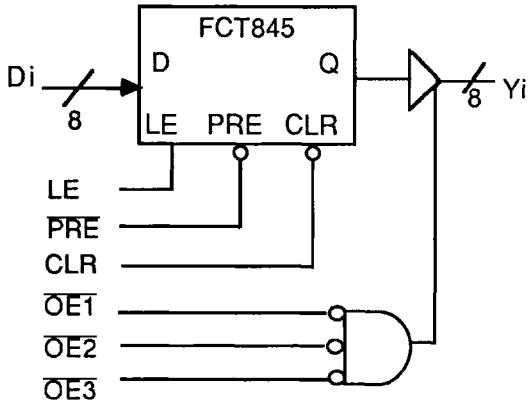






• ALL PINS TOP VIEW

FCT845 LOGIC SYMBOL



PIN DESCRIPTIONS

Name	I/O	Function
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
$\overline{OEi}$	I	Output Enable
LE	I	Latch Enable
$\overline{PRE}$	I	Preset
$\overline{CLR}$	I	Asynchronous Reset

FUNCTION TABLES -

QSFCT841, 2841

Inputs			Int.	O/P	Function
$\overline{OE}$	LE	DI	QI	YI	
H	X	X	X	Z	Hi-Z
L	X	X	H	H	Output Enabled
L	X	X	L	L	Output Enabled
X	H	H	H	X	Transparent
X	H	L	L	X	Transparent
X	L	X	NC	X	Latched

QSFCT843/5, 2843/5

Inputs					Int.	O/P	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	DI	QI	YI	
H	H	H	X	X	X	Z	Hi-Z
X	X	L	X	X	H	H	Output Enabled
X	X	L	X	X	L	L	Output Enabled
H	H	L	H	H	H	H	Transparent
H	H	L	H	L	L	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset

Notes:
NC = No Change from the previous state
H = HIGH
L = LOW,
Z = High Impedance
Int. = Internal

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,3-10,13	4	4	5	7	pF
15-22	6	6	7	9	pF
2,11,14,23	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 15 mA (MIL)	2.4	-	-	Volts
			Ioh = 24 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 32 mA (MIL)	-	-	0.50	
			Iol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-		0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes: 1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes (1)	841A 843A 845A 2841A 2843A 2845A		841B 843B 845B 2841B 2843B 2845B		841C 843C 845C 2841C 2843C 2845C		Unit
t PHL t PLH	Data to Y Delay $\overline{OE}$=low, FCT841/3/5	Com			9		6.5		5.5	ns
		Mil			10		7.5		6.3	
		Com	2,3		13		13		13	
		Mil	2,3		15		15		15	
	Data to Y Delay $\overline{OE}$=low, FCT2841/3/5	Com			9.5		6.5		5.5	
		Mil			11		7.5		6.3	
		Com	2,3		20		13		13	
		Mil	2,3		20		15		15	
t S	Data to LE Setup Time	Com		2.5		2.5		2.5		
		Mil		2.5		2.5		2.5		
t H	Data to LE Hold Time	Com		2.5		2.5		2.5		
		Mil		3		2.5		2.5		
t LEY	LE to Y Delay $\overline{OE}$=low, FCT841/3/5	Com			12		8		6.4	
		Mil			13		10.5		6.8	
		Com	2,3		16		15.5		15	
		Mil	2,3		20		18		16	
	LE to Y Delay $\overline{OE}$=low, FCT2841/3/5	Com			12		8		8	
		Mil			13		10.5		10.5	
		Com	2,3		16		15.5		15	
		Mil	2,3		20		18		16	

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Cload = 300 pF
4) Cload = 5 pF

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes (1)	841A 843A 845A 2841A 2843A 2845A		841B 843B 845B 2841B 2843B 2845B		841C 843C 845C 2841C 2843C 2845C		Unit
t SLEC	$\overline{CLR}$ to LE Setup Time	Com		3		2.5		2.5		ns
		Mil		3		2.5		2.5		
t CLR t PRE	$\overline{CLR}$, $\overline{PRE}$ to Y Delay 843/5	Com			12		8		7	
		Mil			14		10		9	
	$\overline{CLR}$, $\overline{PRE}$ to Y Delay 2843/5	Com			12		8		7	
		Mil			14		10		9	
t CLRR t PRER	$\overline{CLR}$, $\overline{PRE}$ Recovery Time	Com	2		14		8		8	
		Mil	2		17		10		9	
t LEH	LE Pulse Width High	Com	2	6		4		4		
		Mil	2	6		4		4		
t PREL	$\overline{PRE}$, $\overline{CLR}$ Pulse Width Low	Com	2	8		4		4		
		Mil	2	9		4		4		
t PZH t PZL	Output Enable Time $\overline{OE}$ to Yi, FCT841	Com			12		8		6.5	
		Mil			14		8.5		8.5	
		Com	2,3		23		14		14	
		Mil	2,3		25		15		15	
	Output Enable Time $\overline{OE}$ to Yi, FCT2841	Com			12		8		6.5	
		Mil			14		8.5		8.5	
		Com	2,3		23		8		8	
		Mil	2,3		25		8.5		8.5	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	Com	2,4		7		6		5.7	
		Mil	2,4		9		9		6.0	
		Com	2		8		8		7	
		Mil	2		10		10		7.5	

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Cload = 300 pF
4) Cload = 5 pF