

Signetics

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Status	Product Specification
FAST Products	

FAST 74F640 Transceiver

Octal Bus Transceiver, Inverting (3-State)

FEATURES

- High-impedance NPN base inputs for reduced loading (70 μ A in High and Low states)
- Ideal for applications which require high-output drive and minimal bus loading
- Inverting version of 'F245
- Octal bidirectional bus interface
- 3-state buffer outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F640N
20-Pin Plastic SOL	N74F640D

DESCRIPTION

The 74F640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics. The device features an Output Enable (\overline{OE}) input for easy cascading and Transmit/Receive (T/R) input for direction control. The 3-state outputs, B_0 - B_7 , have been designed to prevent output bus loading if the power is removed from the device.

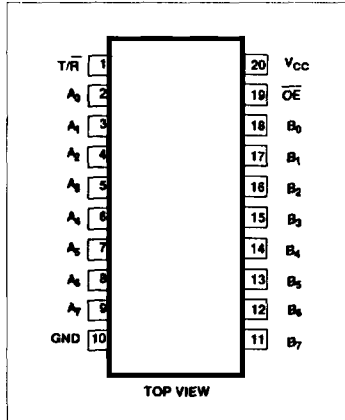
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7 , B_0 - B_7	Data inputs	3.5/0.115	70 μ A/70 μ A
\overline{OE}	Output enable input (active Low)	2.0/0.067	40 μ A/40 μ A
T/R	Transmit/Receive input	2.0/0.067	40 μ A/40 μ A
A_0 - A_7	A port outputs	150/40	3.0mA/24mA
B_0 - B_7	B Port outputs	750/106.7	15mA/64mA

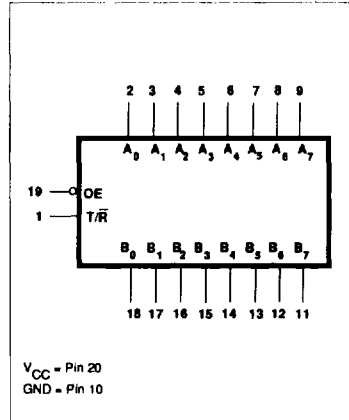
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

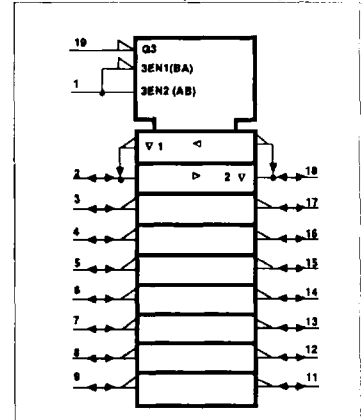
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



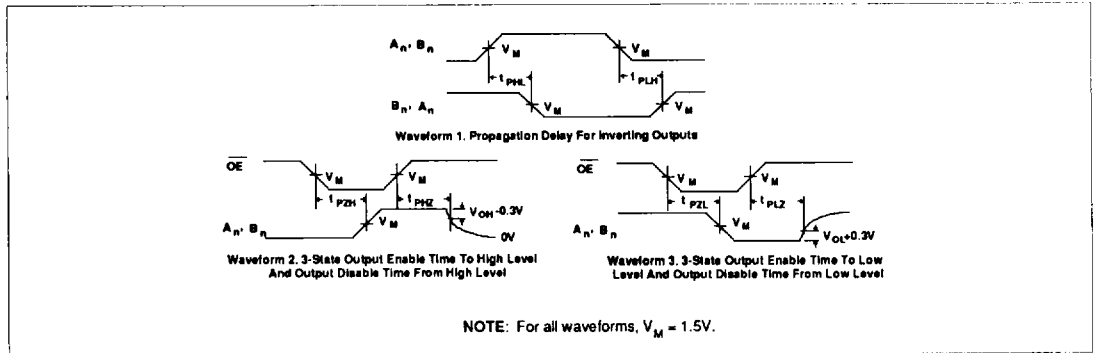
Transceiver

FAST 74F640

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n , B_n to A_n	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

