



**4066**

**CMOS IC**

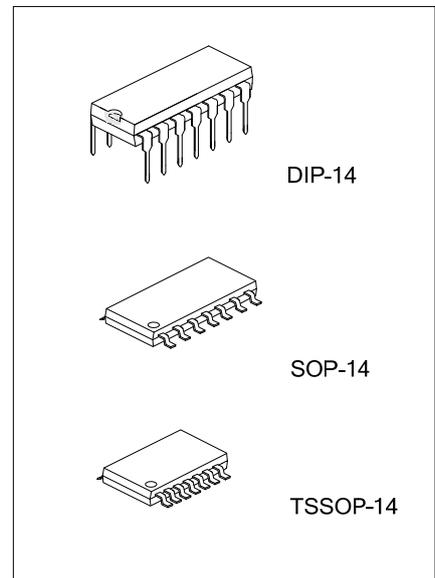
**QUAD BILATERAL SWITCH**

■ **DESCRIPTION**

The UTC **4066** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals.

■ **FEATURES**

- \* Wide supply voltage range: 3V ~ 15V.
- \* High noise immunity : 0.45V<sub>DD</sub> (typ.)
- \* Wide range of digital and ± 7.5V<sub>PEAK</sub> analog switching
- \* "ON" resistance for 15V operation : 80Ω
- \* Matched "ON" resistance : ΔR<sub>ON</sub>=5Ω (typ.) over 15V signal input
- \* "ON" resistance flat over peak-to-peak signal range
- \* High "ON" / "OFF" : 65 dB (typ.)
- output voltage ratio @ f<sub>IS</sub>=10kHz, R<sub>L</sub>=10kΩ
- \* High degree linearity: 0.1% distortion (typ.)  
@ f<sub>IS</sub>=1kHz, V<sub>IS</sub>=5Vp-p.  
V<sub>DD</sub>-V<sub>SS</sub>=10V, R<sub>L</sub>=10kΩ
- \* Extremely low "OFF" : 0.1nA (typ.)
- \* switch leakage @V<sub>DD</sub>-V<sub>SS</sub>=10V, T<sub>A</sub>=25°C
- \* Extremely high control input impedance : 10<sup>12</sup>Ω (typ.)
- \* Low crosstalk : -50dB (typ.)
- between switches @ f<sub>IS</sub>=0.9MHz, R<sub>L</sub>=1kΩ
- \* Frequency response, switch "ON" : 40MHz (typ.)



■ **ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
4066L-D14-T	4066G-D14-T	DIP-14	Tube
4066L-S14-R	4066G-S14-R	SOP-14	Tape Reel
4066L-P14-R	4066G-P14-R	TSSOP-14	Tape Reel

<p>4066G-D14-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: R: Tape Reel (2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ **MARKING**

DIP-14	SOP-14 / TSSOP-14
<p>14 13 12 11 10 9 8 → Date Code UTC □□□□ 4066 □ → L: Lead Free           □ → G: Halogen Free           □□ → Lot Code 1 2 3 4 5 6 7</p>	<p>14 13 12 11 10 9 8 → Date Code UTC □□□□ 4066 □ → L: Lead Free           □ → G: Halogen Free           □□ → Lot Code 1 2 3 4 5 6 7</p>



■ ABSOLUTE MAXIMUM RATINGS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	-0.5 ~ +18	V
Input Voltage	$V_{IN}$	-0.5 ~ $V_{CC}+0.5$	V
Power Dissipation	DIP-14	700	mW
	SOP-14/TSSOP-14	500	
Junction Temperature	$T_J$	+125	°C
Storage Temperature	$T_{STG}$	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	3 ~ 15	V
Input Voltage	$V_{IN}$	0 ~ $V_{DD}$	V
Operating Temperature Range	$T_A$	-40 ~ +125	°C

■ DC ELECTRICAL CHARACTERISTICS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Device Current	$I_{DD}$	$V_{DD}=5V$		0.01	1.0	$\mu A$
		$V_{DD}=10V$		0.01	2.0	
		$V_{DD}=15V$		0.01	4.0	
<b>SIGNAL INPUTS AND OUTPUTS</b>						
Input or Output Leakage Switch "OFF"	$I_{IS}$	$V_C=0$		$\pm 0.1$	$\pm 50$	nA
"ON" Resistance	$R_{ON}$	$R_L=10k\Omega \sim (V_{DD}-V_{SS}/2)$ $V_C=V_{DD}, V_{SS} \sim V_{DD}$	$V_{DD}=5V$	270	1050	$\Omega$
			$V_{DD}=10V$	120	400	
			$V_{DD}=15V$	80	240	
$\Delta$ "ON" Resistance Between Any 2 of 4 Switches	$\Delta R_{ON}$	$R_L=10k\Omega \sim (V_{DD}-V_{SS}/2)$ $V_C=V_{DD}, V_{IS}=V_{SS} \sim V_{DD}$	$V_{DD}=5V$	20		$\Omega$
			$V_{DD}=10V$	10		
			$V_{DD}=15V$	5		
<b>CONTROL INPUTS</b>						
Low Level Input Voltage	$V_{ILC}$	$V_{IS}=V_{SS}$ and $V_{DD}$ $V_{OS}=V_{DD}$ and $V_{SS}$ $I_{IS}=\pm 10\mu A$	$V_{DD}=5V$	2.25	1.5	V
			$V_{DD}=10V$	4.5	3.0	
			$V_{DD}=15V$	6.75	4.0	
HIGH Level Input Voltage	$V_{IHC}$	$V_{DD}=5V$ $V_{DD}=10V$ (Note) $V_{DD}=15V$	3.5	2.75		V
			7.0	5.5		
			11.0	8.25		
Input Current	$I_{IN}$	$V_{DD}-V_{SS}=15V, V_{DD} \geq V_{IS} \geq V_{SS},$ $V_{DD} \geq V_C \geq V_{SS}$		$\pm 10^{-5}$	$\pm 0.3$	$\mu A$

Note: Conditions for  $V_{IHC}$ : (a)  $V_{IS}=V_{DD}$ ,  $I_{OS}$ =standard B series  $I_{OH}$ . (b)  $V_{IS}=0V$ ,  $I_{OL}$ =standard B series  $I_{OL}$

■ AC ELECTRICAL CHARACTERISTICS (AC Parameters are guaranteed by DC correlated testing)

( $T_A=25^\circ\text{C}$ ,  $t_R=t_F=20\text{ ns}$  and  $V_{SS}=0\text{V}$  unless otherwise)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time Signal Input to Signal Output	$T_{PHL}, T_{PLH}$	$V_C=V_{DD}, C_L=50\text{Pf}$ (Figure1) $R_L=200\text{k}$	$V_{DD}=5\text{V}$	25	55	ns
			$V_{DD}=10\text{V}$	15	35	
			$V_{DD}=15\text{V}$	10	25	
Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$t_{PZH}, t_{PLZ}$	$R_L=1.0\text{k}\Omega, C_L=50\text{pF}$ (Fig. 2, 3)	$V_{DD}=5\text{V}$		125	ns
			$V_{DD}=10\text{V}$		60	
			$V_{DD}=15\text{V}$		50	
Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$t_{PHZ}, t_{PLZ}$	$R_L=1.0\text{k}\Omega, C_L=50\text{pF}$ (Fig. 2, 3)	$V_{DD}=5\text{V}$		125	ns
			$V_{DD}=10\text{V}$		60	
			$V_{DD}=15\text{V}$		50	
Sine Wave Distortion	$t_{PHZ}, t_{PLZ}$	$V_C=V_{DD}=5\text{V}, V_{SS}= -5\text{V}$ $R_L=10\text{k}\Omega, V_{IS}=5\text{V}_{P-P}, f=1\text{kHz}$ , (Fig. 4)		0.1		%
Frequency Response -Switch "ON" (Frequency at -3dB)			$V_C=V_{DD}=5\text{V}, V_{SS}= -5\text{V}$ $R_L=1\text{k}\Omega, V_{IS}=5\text{V}_{P-P}$ $20 \text{Log}_{10} V_{OS}/V_{IS}$ (1kHz)-dB (Fig. 4)		40	
Feedthrough - Switch "OFF" (Frequency at -50 dB)		$V_{DD}=5.0\text{V}, V_{CC}=V_{SS}= -5.0\text{V}, R_L=1\text{k}\Omega,$ $V_{IS}=5.0\text{V}_{P-P}, 20\text{Log}_{10}, V_{OS}/V_{IS}= -50\text{dB}$ , (Fig. 4)		1.25		MHz
Crosstalk Between Any Two Switches(Frequency at -50dB)		$V_{DD}=V_C(A)=5.0\text{V}; V_{SS}=V_C(B)=5.0\text{V},$ $R_L=1\text{k}\Omega, V_{IS}(A)=5.0\text{V}_{P-P}, 20\text{Log}_{10},$ $V_{OS}(B)/V_{IS}(A)= -50\text{dB}$ (Fig. 5)		0.9		MHz
Crosstalk; Control Input to Signal Output		$V_{DD}=10\text{V}, R_L=10\text{k}\Omega, R_{IN}=1.0\text{k}\Omega,$ $V_{CC}=10\text{V}$ Square Wave, $C_L=50\text{pF}$ (Fig. 6)		150		$\text{mV}_{p-p}$
Maximum Control Input		$R_L=1.0\text{k}\Omega, C_L=50\text{pF}$ (Fig. 7) $V_{OS}(f) = 1/2V_{OS}(1.0\text{kHz})$	$V_{DD}=5.0\text{V}$	6.0		MHz
			$V_{DD}=10\text{V}$	8.0		
			$V_{DD}=15\text{V}$	8.5		
Signal Input Capacitance	$C_{IS}$			8.0		pF
Signal Output Capacitance	$C_{OS}$	$V_{DD}=10\text{V}$		8.0		pF
Feedthrough Capacitance	$C_{IOS}$	$V_C=0\text{V}$		0.5		pF
Control Input Capacitance	$C_{IN}$			5.0	7.5	pF

■ SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive  $V_{DD}$  and the signal input, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$ =effective external load of the UTC 4066 bilateral switches).This provision avoids any permanent current flow or clamp action of the  $V_{DD}$  supply when power is applied or removed from UTC 4066.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and Signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into terminals 1,4,8 or 11,the voltage drop across the bidirectional swith must not exceed 0.6V at  $T_A \leq 25^\circ\text{C}$ , or 0.4V at  $T_A > 25^\circ\text{C}$  (calculated from  $R_{ON}$  values shown).

NO  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9 or 10.

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

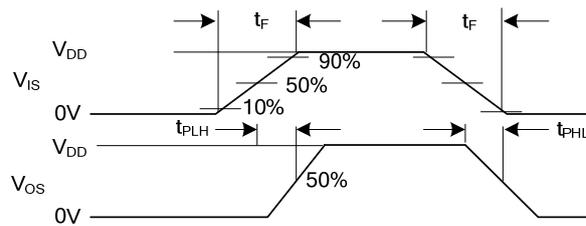
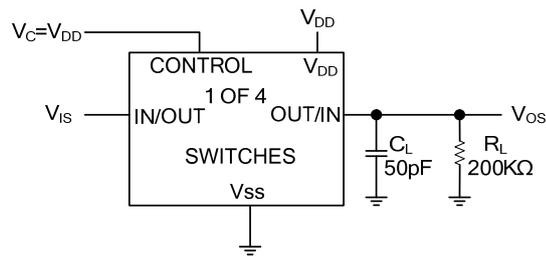


Fig.1  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

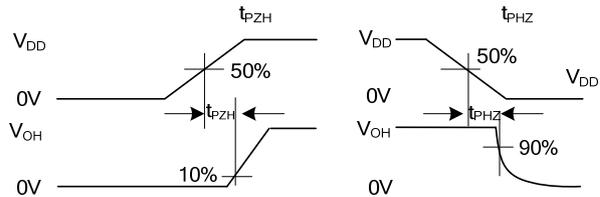
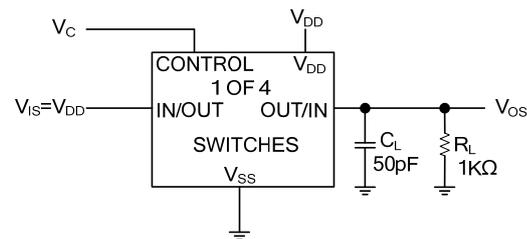


Fig. 2  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

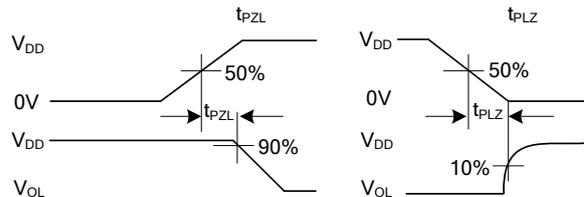
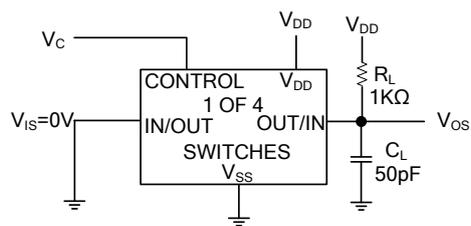
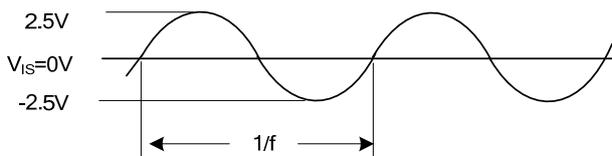
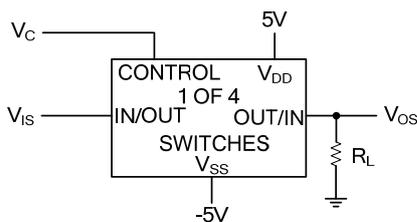


Fig. 3  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output



$V_C=V_{DD}$  for distortion and frequency response tests  
 $V_C=V_{SS}$  for feedthrough test

Fig. 4 Sine Wave Distortion, Frequency Response and Feedthrough

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS (Cont.)

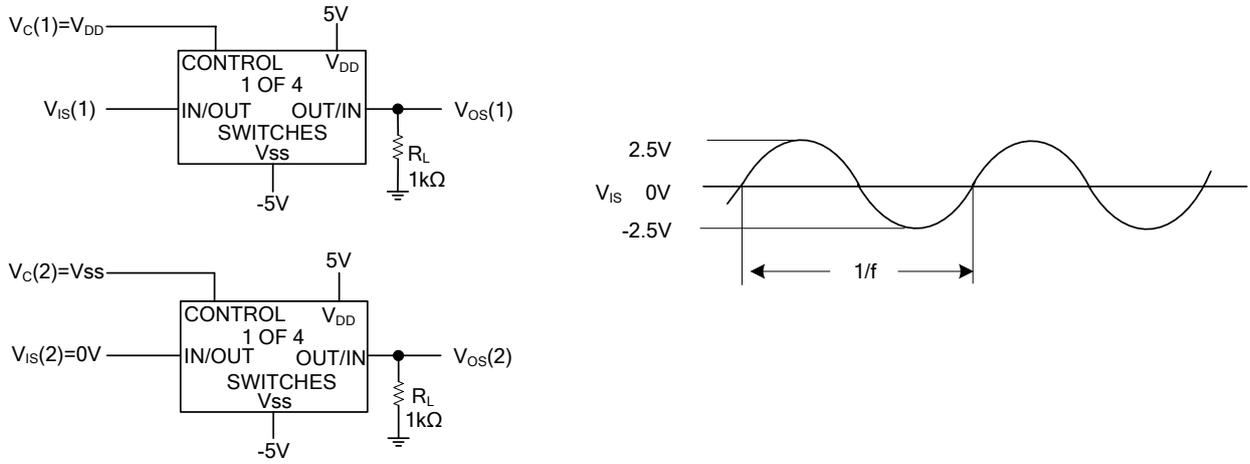


Fig. 5 Crosstalk Between Any Two Switches

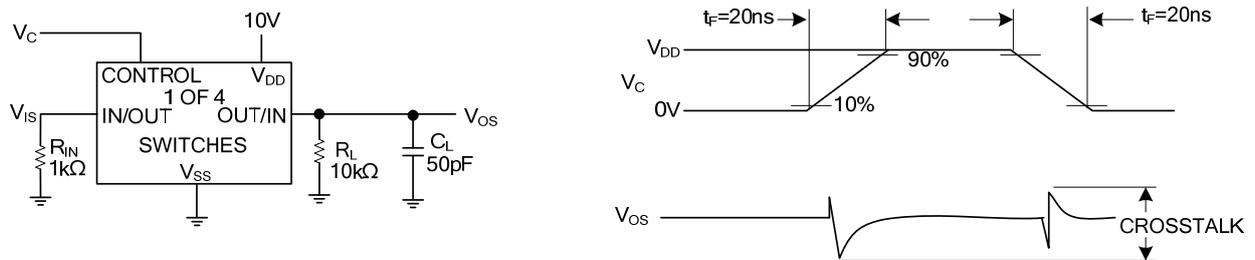


Fig.6 Crosstalk: Control Input to Signal Output

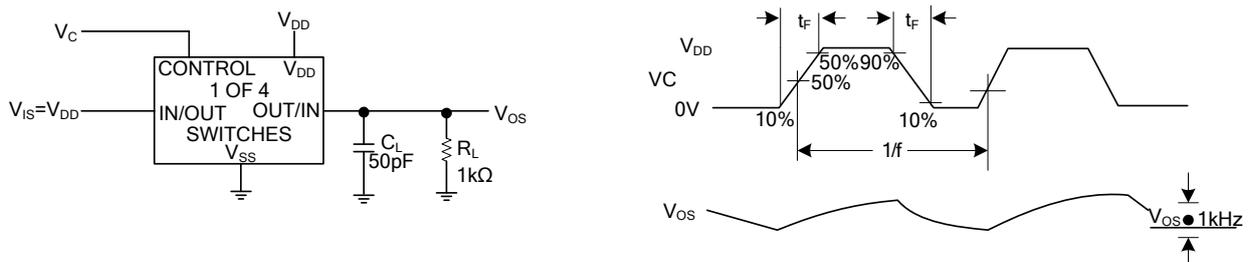


Fig. 7 Maximum Control Input Frequency

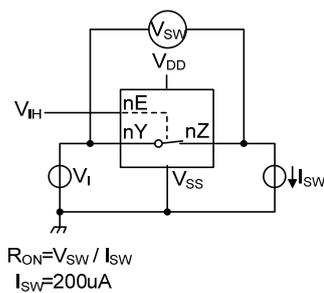
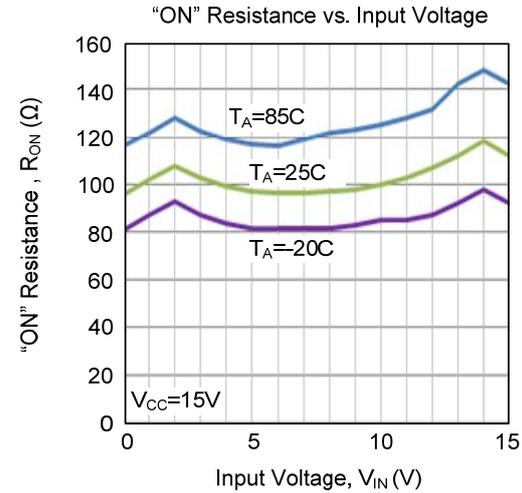
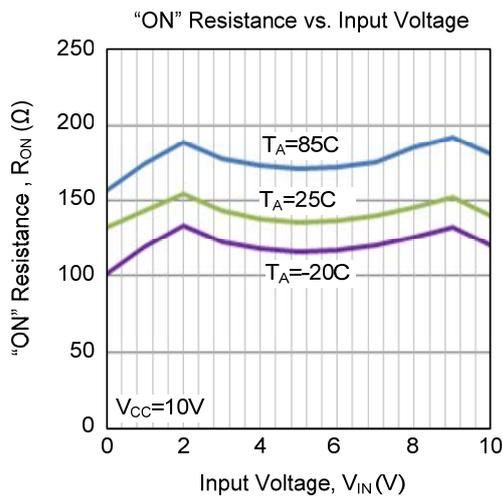
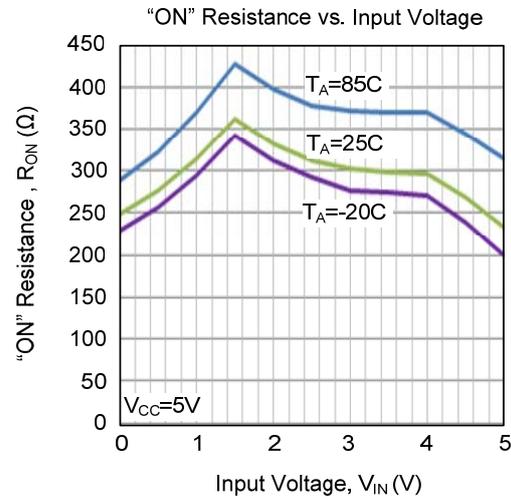
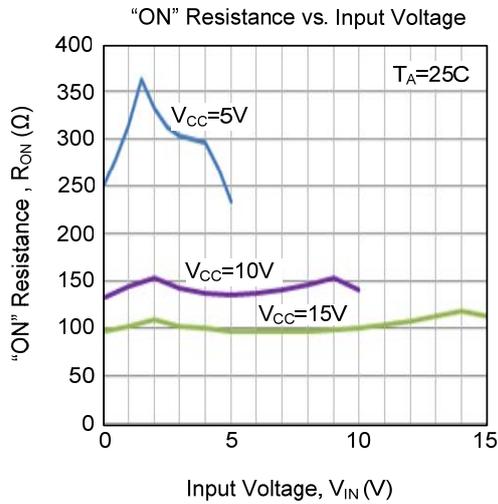


Fig. 8 Test circuit for measuring  $R_{ON}$

■ TYPICAL CHARACTERISTICS



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