EDH8808ACL
85/10/12/15/20
Monolithic

The future...today.

8Kx8 Static RAM
CMOS, Low Power
Monolithic

The EDH8808ACL is a high performance, low power CMOS Static RAM organized as 8192 words by 8 bits each. In addition to 13 address inputs and 8 common data inputs and outputs, the device contains 4 control lines. The $\overline{E1}$ and E2 lines perform chip enable functions and automatically power down the device when proper logic levels are applied. The $\overline{G}$ and $\overline{W}$ lines facilitate read and write operations.

The EDH8808ACL offers battery back-up data retention capability at VDD equal to 2V.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

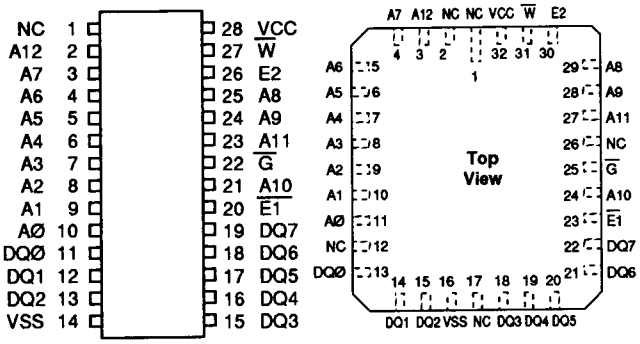
Features

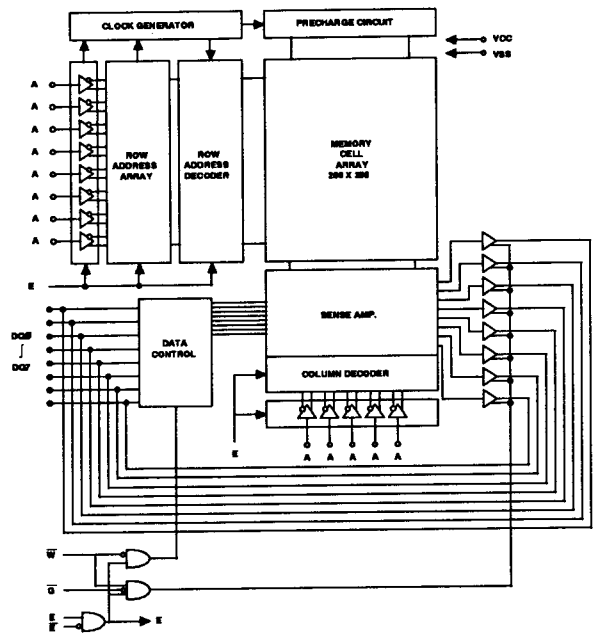
64K bit CMOS Static RAM
Organized as 8,192 x8 Bits
- Access Times of 85,100, 120, 150 and 200ns
- $\overline{E}$ and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Low Power Operation
  - Active: 250mW
  - Standby: 250µW
- TTL Compatible Inputs and Outputs

JEDEC Approved Pinout
- 32 Pin Leadless Chip Carrier
- 28 Pin CERDIP

Single 5V(±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A12	Address Inputs
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Data Input/Output
VCC	Power (+5V ±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.3V to 7.0V
Operating Temperature TA (Ambient)	
Military	-55°C to +125°C
Storage Temperature (Ambient/Ceramic)	-65°C to +150°C
Power Dissipation	1W
Output Current	20mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	Ø	Ø	Ø	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{E1}$= VIL, II/O = ØmA E2=VIH	--	50	70	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E1}$≥ VIH or E2≤ VIL	--	2	10	mA
Full Standby Power Supply Current	ICC3	$\overline{E1}$≥ VCC-0.2V or E2≤0.2V VIN ≥VCC-0.2V or VIN ≤0.2V	--	10	100	µA
Input Leakage Current	IIL	VIN = ØV to VCC	--	--	±5	µA
Output Leakage Current	IOL	$\overline{V}$ I/O = ØV to VCC $\overline{E1}$=VIH or E2=VIL or G=VIH	--	--	±5	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 2.1mA	--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E1}$	E2	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2,ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	READ	DOUT	ICC1
X	L	H	L	WRITE	DIN	ICC1

Capacitance

(f = 1.0MHz, VIN = VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (except D/Q)	CI	6	10	pF
Capacitance on D/Q pins	CD/Q	8	12	pF

A.C. Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load: 100-200ns..... 1 TTL, CL = 100pF
70ns..... 1 TTL, CL = 30pF
(Note: for TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym		85 ns		100ns		120ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		85		100		120		ns
Address Access Time	TAVQV			85		100		120	ns
Chip Enable Access Time	TE1LQV	$\overline{E1}$		85		100		120	ns
	TE2HQV	E2		85		100		120	ns
Chip Enable to Output Low Z (1)	TE1LQX	$\overline{E1}$	5		10		10		ns
	TE2HQX	E2	5		10		10		ns
Output Enable to Output Valid	TGLQV			40		40		45	ns
Output Enable to Output in Low Z (1)	TGLQX		5		10		10		ns
Chip Enable to Output in High Z (1)	TE1HQZ	$\overline{E1}$	Ø	35	Ø	35	Ø	35	ns
	TE2LQZ	E2	Ø	35	Ø	35	Ø	35	ns
Output Enable to Output in High Z (1)	TGHQZ			35		35		35	ns
Output Hold from Address Change	TAVQX		5		5		5		ns

Note1: Parameter is guaranteed, but not tested.

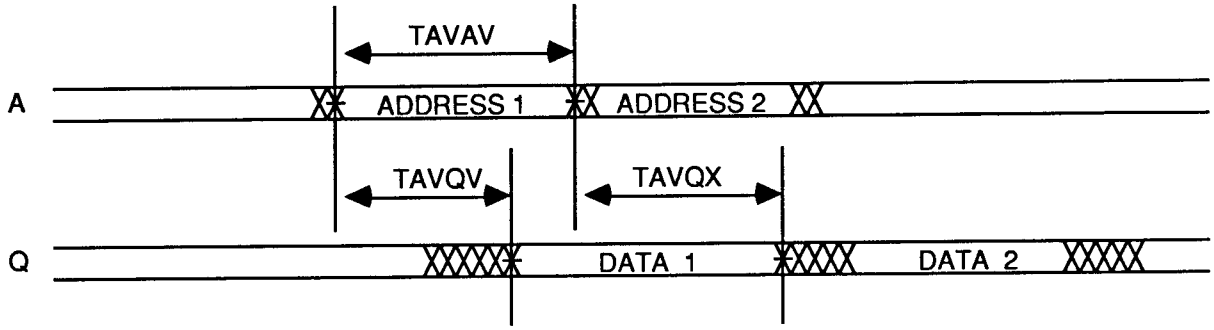
AC Characteristics
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

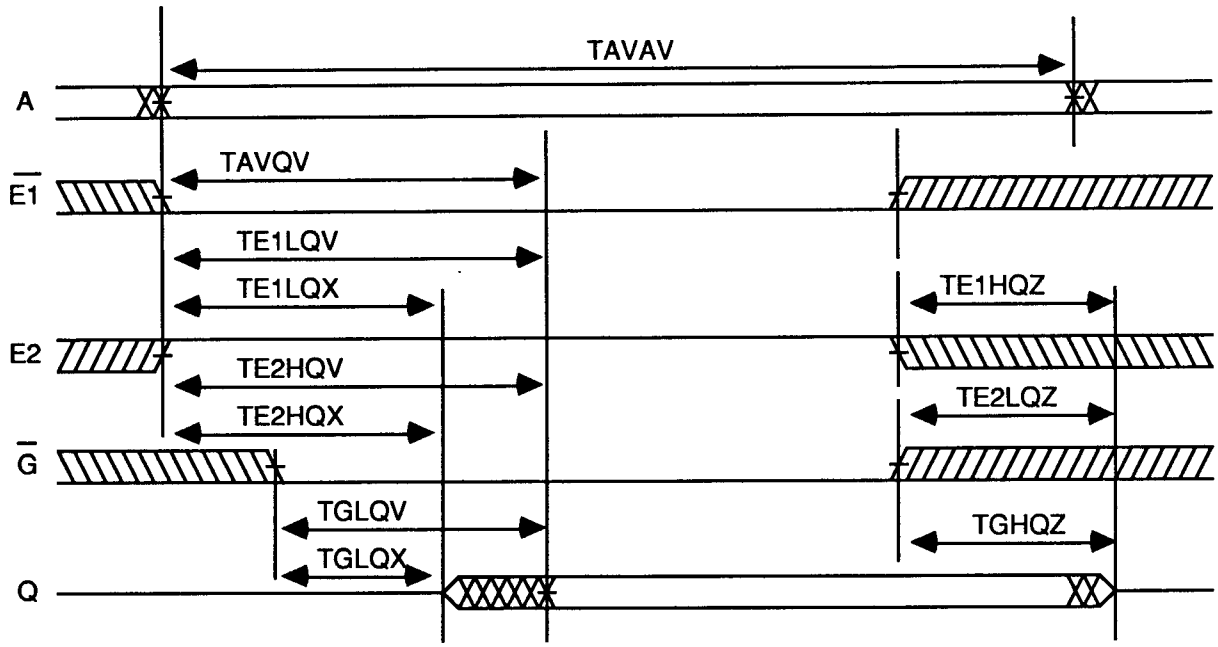
Parameter	Sym		150 ns		200ns		Units
			Min	Max	Min	Max	
Read Cycle Time	TAVAV		150		200		ns
Address Access Time	TAVQV			150		200	ns
Chip Enable Access Time	TE1LQV	$\overline{E1}$		150		200	ns
	TE2HQV	E2		150		200	ns
Chip Enable to Output Low Z (1)	TE1LQX	$\overline{E1}$	10		10		ns
	TE2HQX	E2	10		10		ns
Output Enable to Output Valid	TGLQV			45		60	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		ns
Chip Enable to Output in High Z (1)	TE1HQZ	$\overline{E1}$	Ø	45	Ø	70	ns
	TE2LQZ	E2	Ø	45	Ø	70	ns
Output Enable to Output in High Z (1)	TGHQZ			50		70	ns
Output Hold from Address Change	TAVQX		5		10		ns

Note1: Parameter is guaranteed, but not tested.

Read Cycle 1
$\overline{W}$, E2 High; G, $\overline{E1}$ Controlled



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym		85ns		100ns		120ns		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		85		100		120		ns
Chip Enable to End of Write	TE1LWH	$\overline{E1}$	70		85		85		ns
	TE2HWH	E2	70		85		85		ns
Address Setup Time	TAVWL	$\overline{W}$	Ø		Ø		Ø		ns
	TAVE1L	$\overline{E1}$	Ø		Ø		Ø		ns
	TAVE2H	E2	Ø		Ø		Ø		ns
Write Pulse Width	TWLWH	$\overline{W}$	60		70		70		ns
	TE1LE1H	$\overline{E1}$	60		70		70		ns
	TE2HE2L	E2	60		70		70		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TE1HAX	$\overline{E1}$	5		5		5		ns
	TE2LAX	E2	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		ns
	TE1HDX	$\overline{E1}$	5		5		5		ns
	TE2LDX	E2	5		5		5		ns
Write to Output in High Z (1)	TWLQZ			40		50		50	ns
Data to Write Time	TDVWH	$\overline{W}$	30		40		50		ns
	TDVE1H	$\overline{E1}$	30		40		50		ns
	TDVE2L	E2	30		40		50		ns
Output Active from End of Write (1)	TWHQX		5		5		5		ns
Address Valid to End of Write	TAVWH		65		100		120		ns

Note 1: Parameter is guaranteed, but not tested.

AC Characteristics

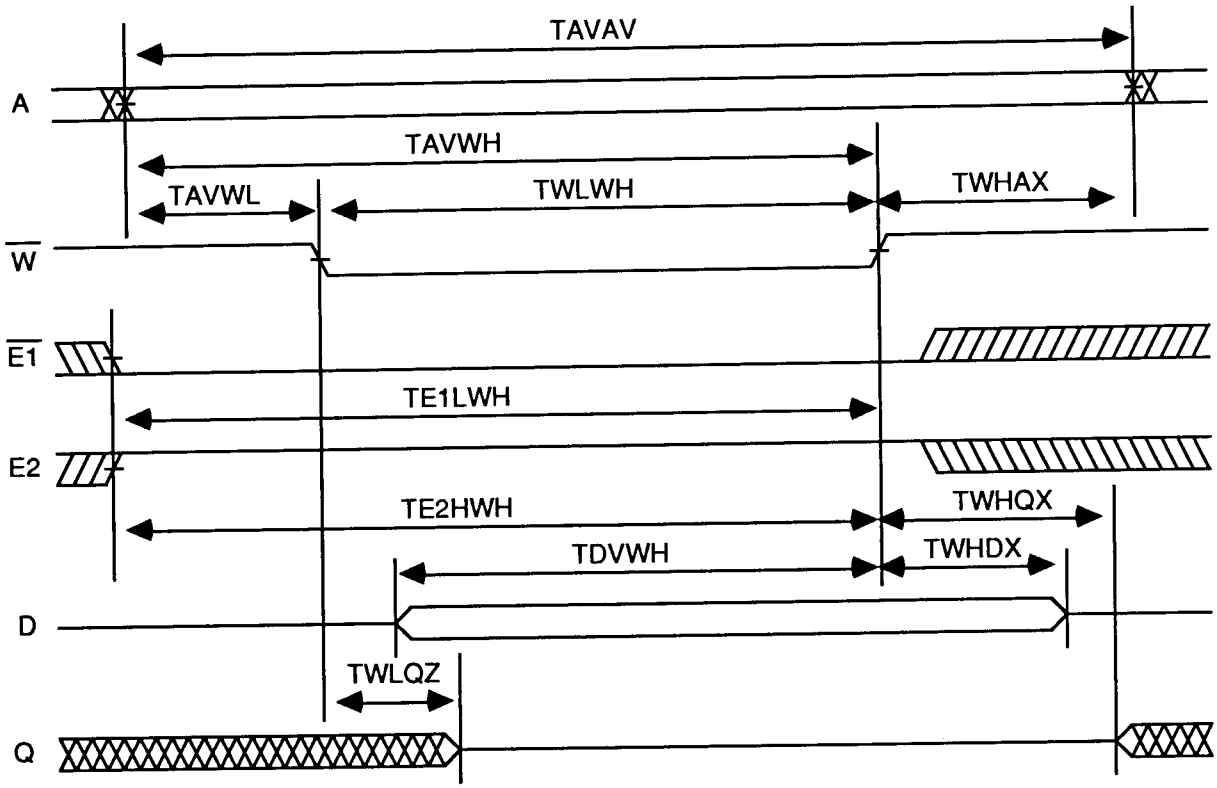
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

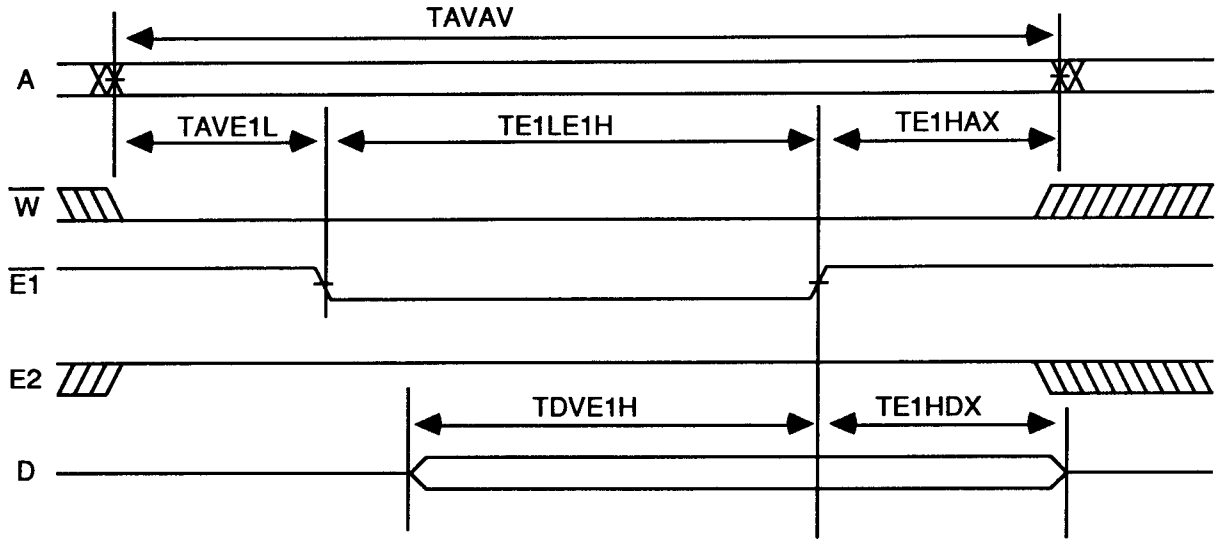
Parameter	Sym		150ns		200 ns		Units
			Min	Max	Min	Max	
Write Cycle Time	TAVAV		150		200		ns
Chip Enable to End of Write	TE1LWH	$\overline{E1}$	85		120		ns
	TE2HWH	E2	85		120		ns
Address Setup Time	TAVWL	$\overline{W}$	Ø		Ø		ns
	TAVE1L	$\overline{E1}$	Ø		Ø		ns
	TAVE2H	E2	Ø		Ø		ns
Write Pulse Width	TWLWH	$\overline{W}$	70		110		ns
	TE1LE1	$\overline{E1}$	70		110		ns
	TE2HE2L	E2	70		110		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		ns
	TE1HAX	$\overline{E1}$	5		5		ns
	TE2LAX	E2	5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		ns
	TE1HDX	$\overline{E1}$	5		5		ns
	TE2LDX	E2	5		5		ns
Write to Output in High Z (1)	TWLQZ			50		70	ns
Data to Write Time	TDVWH	$\overline{W}$	60		80		ns
	TDVE1H	$\overline{E1}$	60		80		ns
	TDVE2L	E2	60		80		ns
Output Active from End of Write(1)	TWHQX		5		10		ns
Address Valid to End of Write	TAVWH		100		200		ns

Note 1: Parameter is guaranteed, but not tested.

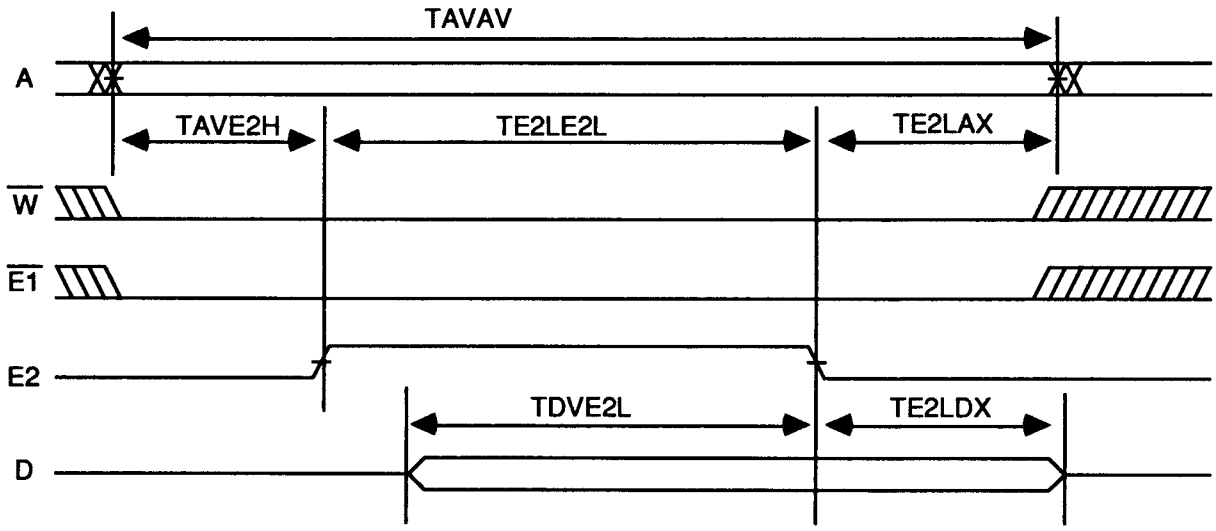
Write Cycle 1
Late Write
$\overline{W}$ Controlled



Write Cycle 2
Early Write
$\overline{E1}$ Controlled



Write Cycle 3
Early Write
E2 Controlled



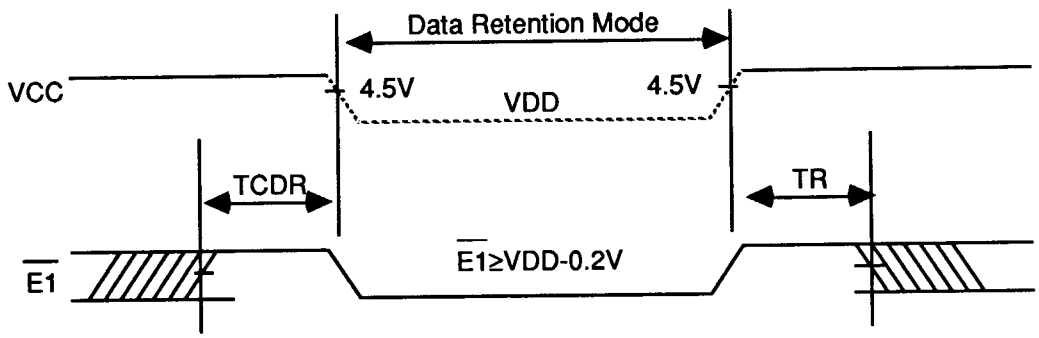
Data Retention Characteristics

(TA = -55°C to +125°C)

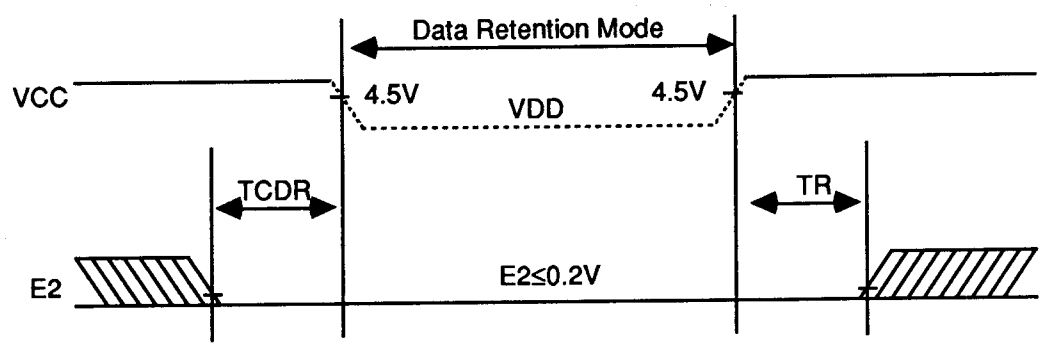
Characteristics	Sym	Test Conditions	Min	Typ	Max	Units
Data Retention Voltage	VDD	$\overline{VDD}$ = 2.0V $\overline{E1}$≥ VDD -0.2V E2 ≤0.2V VIN ≥VDD-0.2V or VIN ≤0.2V	2.0			V
Data Retention Quiescent Current	ICCDR			5	50	µA
Chip Disable to Data Retention Time	TCDR		0			ns
Operation Recovery Time	TR		TAVAV*			ns

*TAVAV = READ CYCLE TIME

Data Retention $\overline{E}$ Controlled

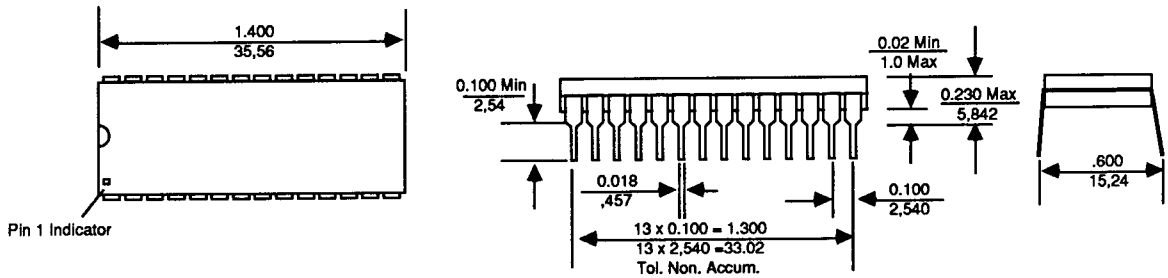


Data Retention E2 Controlled

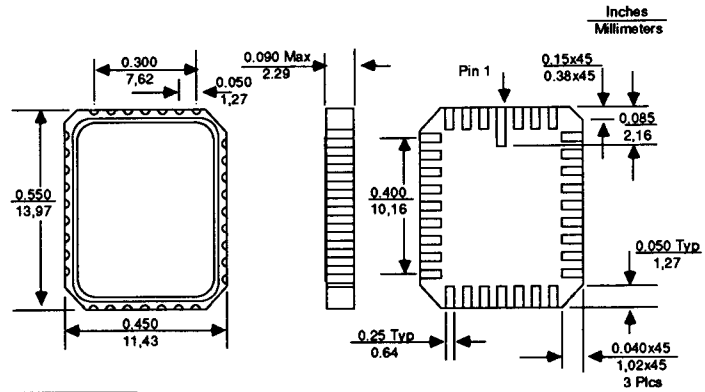


Package Descriptions

D Package
28 Pin CERDIP



J Package
32 Pin
Leadless Chip Carrier
Ceramic



Ordering Information

Part Number	Spd (ns)	Pkg.	Temp Range
EDH8808ACL-85DMHR	85	D	Military
EDH8808ACL-10DMHR	100	D	Military
EDH8808ACL-12DMHR	120	D	Military
EDH8808ACL-15DMHR	150	D	Military
EDH8808ACL-20DMHR	200	D	Military
EDH8808ACL-85JMHR	85	J	Military
EDH8808ACL-10JMHR	100	J	Military
EDH8808ACL-12JMHR	120	J	Military
EDH8808ACL-15JMHR	150	J	Military
EDH8808ACL-20JMHR	200	J	Military

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