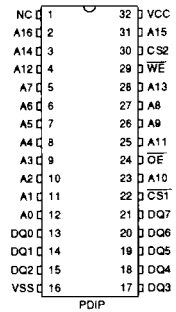
DESCRIPTION

The HY628100 is a high speed, low power and 131,072 x 8-bit CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns. The HY628100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628100 series.

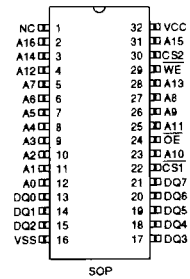
FEATURES

- **High speed -70/85/100/120ns**
- **Low power consumption**
  - **250mW typical operating**
  - **10μW typical standby**
- **Battery back up (L/LL-part)**
  - **2.0V data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **TTL Compatible Inputs and outputs**
- **Tri-state output**
- **Standard Pin Configuration**
  HY628100P : 600mil 32pin PDIP
  HY628100G : 525mil 32pin SOP
  HY628100T1 : 8x20mm TSOP-I
  HY628100R1 : 8x20mm TSOP-I(R)

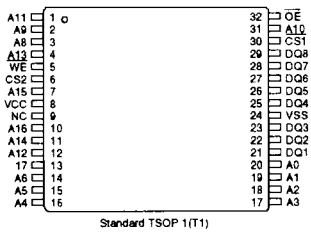
PIN CONNECTION



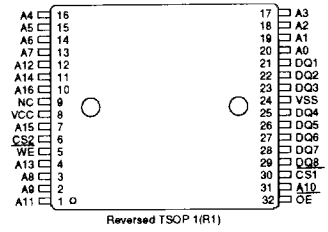
PDIP



SOP



Standard TSOP 1(T1)

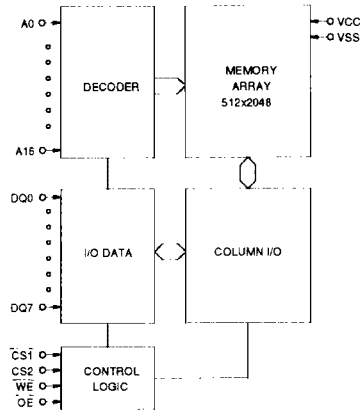


Reversed TSOP 1(R1)

PIN DESCRIPTION

$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A16	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power(+ 5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS NOTE 1

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	- 0.5 to 7.0	V
T_{BIAS}	Temperature under Bias	- 10 to 125	°C
T_{STG}	Storage Temperature	- 65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	°C•sec

NOTE :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating range of this specification is not implied. Exposure to absolute maximum ratings conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

NOTE :

1. V_{IL}= –3.5V for pulse width less than 20ns.

TRUTH TABLE

MODE	DQ OPERATION	$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X	X
	High-Z	X	L	X	X
Output Disabled	High-Z	L	H	H	H
Read	Data Out	L	H	H	L
Write	Data In	L	H	L	X

NOTE : H= V_{IH}, L= V_{IL}, X= Don't Care.

DC CHARACTERISTICS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER/	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-1	-	1	μA
I_{LO}	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2= V_{IL} or $\overline{OE}$= V_{IH} or $\overline{WE}$= V_{IL}, $V_{SS} \le V_{OUT} \le V_{CC}$		-1	-	1	μA
I_{CC}	Static Operating Current	$\overline{CS1}$= V_{IL}, CS2= V_{IH}, V_{IN}= V_{IH} or V_{IL}, $I_{I/O}$= 0mA		-	50	70	mA
I_{CC1}	Dynamic Operating Current	Cycle Time= 1ms, Duty= 100%, $\overline{CS1} \le$ 0.2V, CS2≥ V_{CC}-0.2V $V_{IN} \le$ 0.2V or ≥ V_{CC}-0.2V, $I_{I/O}$= 0mA		-	-	40	mA
I_{SB}	TTL Standby Current (TTL Inputs)	CS1= V_{IH} or CS2= V_{IL}		-	-	3	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	$\overline{CS1} \ge V_{CC}$-0.2V, CS2≤ 0.2V, $V_{IN} \le$ -0.2V or ≥ V_{CC}-0.2V	-	-	-	2	mA
			L-part	-	2	100	μA
			LL-part	-	2	50	μA
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -1.0mA		2.4	-	-	V

NOTE :
1. Typical values are at V_{CC}= 5.0V, T_A= 25°C and specified loading.

AC CHARACTERISTICS

(TA= 0°C to 70°C)

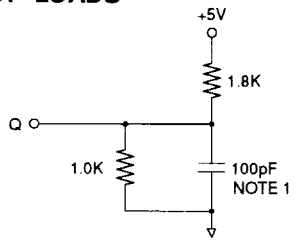
#	SYMBOL	PARAMETER	HY628100								UNIT
			-70		-85		-10		-12		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	70	-	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	35	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Low-Z Output	10	-	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to High-Z Output	-	25	-	30	-	35	-	40	ns
8	tOHZ	Output Disable to High-Z Output	-	25	-	30	-	35	-	40	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	10	-	ns
	WRITE CYCLE										
10	tWC	Write Cycle Time	70	-	85	-	100	-	120	-	ns
11	tCW	Chip Select to Write End	60	-	75	-	90	-	100	-	ns
12	tAW	Address Valid to Write End	60	-	75	-	90	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	60	-	70	-	80	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	-	25	-	30	-	30	-	30	ns
17	tDW	Data to Write Time Overlap	30	-	35	-	40	-	50	-	ns
18	tDH	Data Hold from Write End	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from Write End	5	-	5	-	5	-	5	-	ns

AC TEST CONDITIONS

(TA= 0°C to 70°C)

Parameter	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS



NOTE :
1. Including jig and scope capacitance.

CAPACITANCE

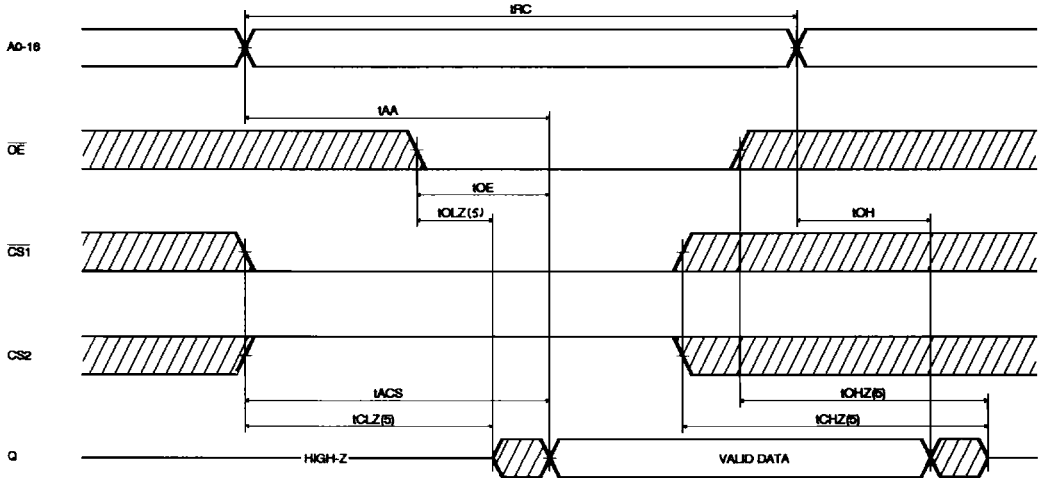
(TA= 25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}= 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$= 0V	10	pF

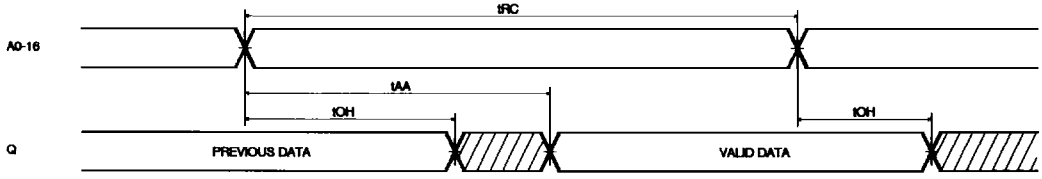
NOTE : This parameter is determined by device characterization but is not production tested.

TIMING DIAGRAM

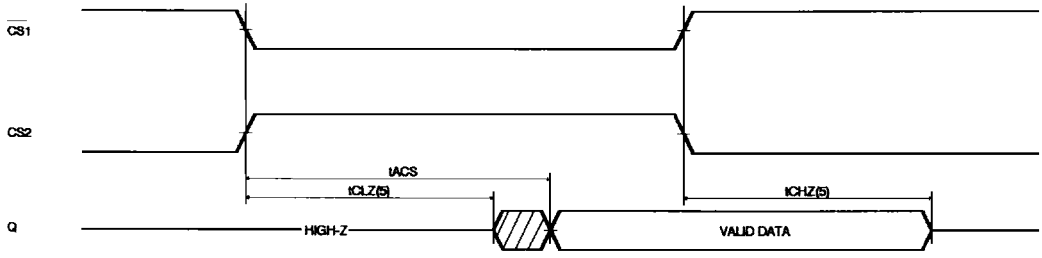
READ CYCLE 1 NOTE 1



READ CYCLE 2 NOTE 1, 2, 4

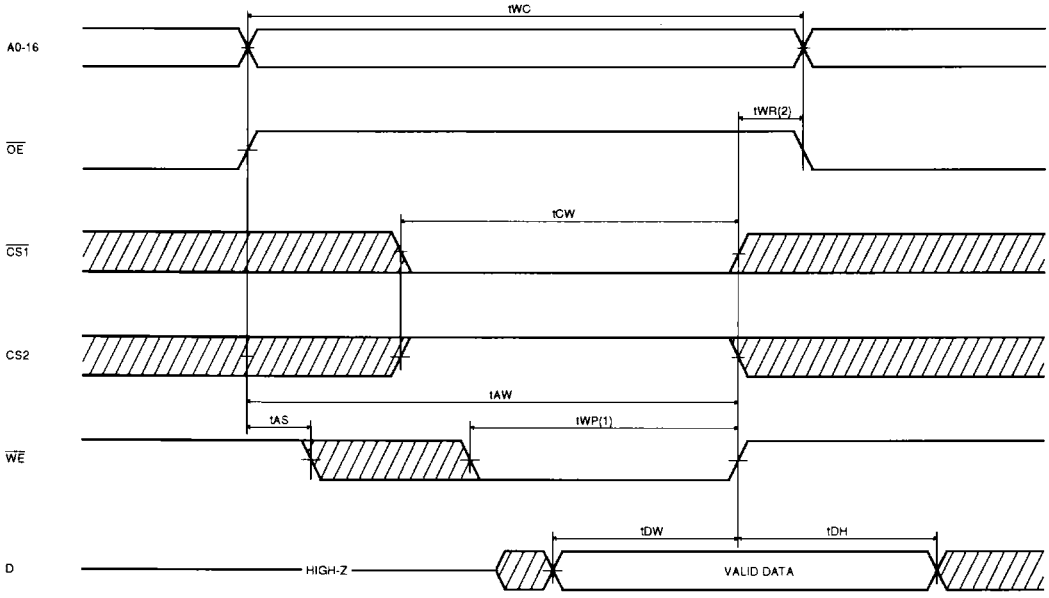


READ CYCLE 3 NOTE 1, 3, 4

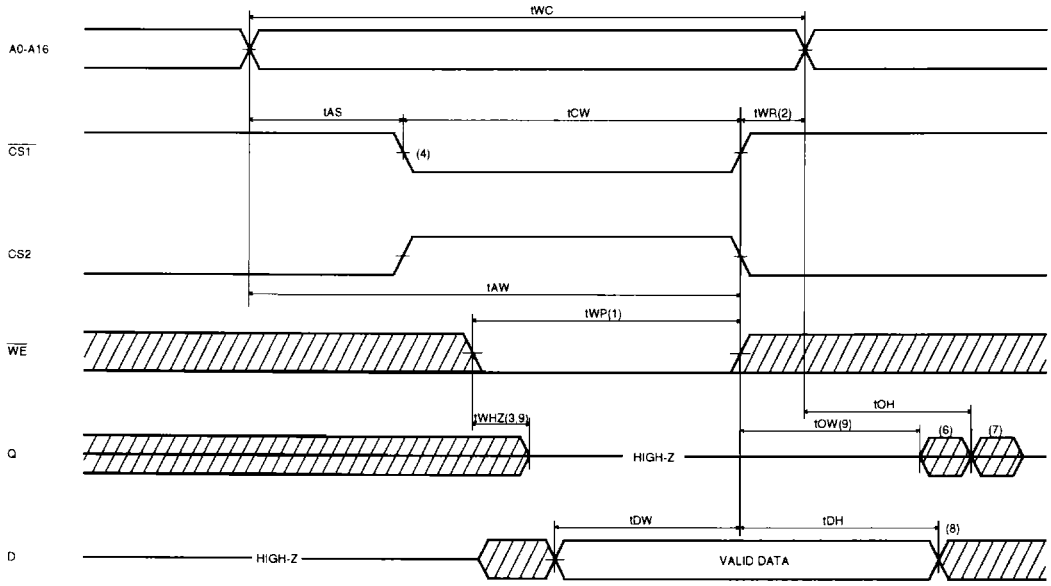


NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS1}$ = VIL, CS2 = VIH.
3. Addresses are valid prior to or coincident with $\overline{CS1}$ transition low, and CS2 transition high.
4. $\overline{OE}$ = VIL.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 NOTE 5



NOTES :

1. A write occurs during the overlap (tWP) of low $\overline{CS1}$, high CS2 and low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going low or CS2 going high to the end of write cycle.
3. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS1}$ low transition and CS2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$= VIL), for write cycle 2.
6. Q is the same phase of write data of this write cycle.
7. Q is the read data of next address.
8. If $\overline{CS1}$ is low and CS2 is high during this period, DQ pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

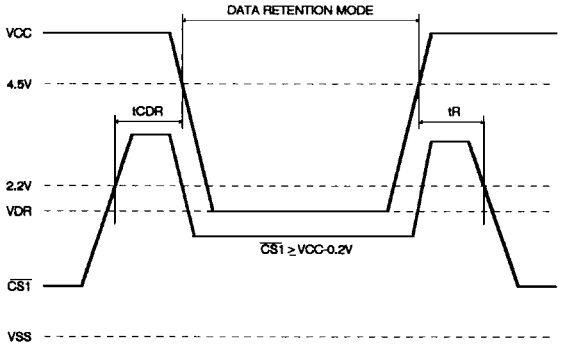
DATA RETENTIOSN CHARACTERISTICS NOTE 1

(T_A = 0°C to 70°C)

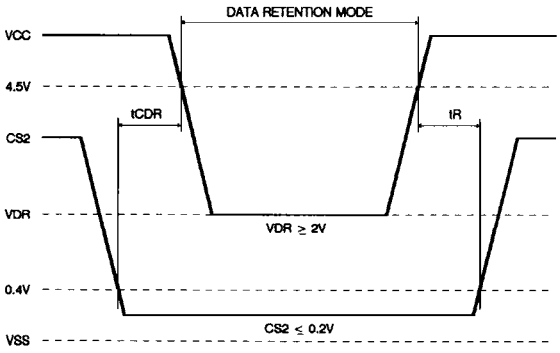
SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.[2]	MAX.	UNIT
V_{DR}	V_{CC} for retention of data	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
I_{CCDR}	Data Retention Current	$V_{CC}=3.0V$, $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	2	50	μA
			LL	-	2	30	μA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
t_R	Operating Recovery Time			t_{RC}[3]	-	-	ns

NOTES :
1. These characteristics are only applied to L-part.
2. Typical values are at the condition of T_A = 25°C.
3. t_{RC} is Read Cycle Time.

DATA RETENTION TIMING DIAGRAM 1

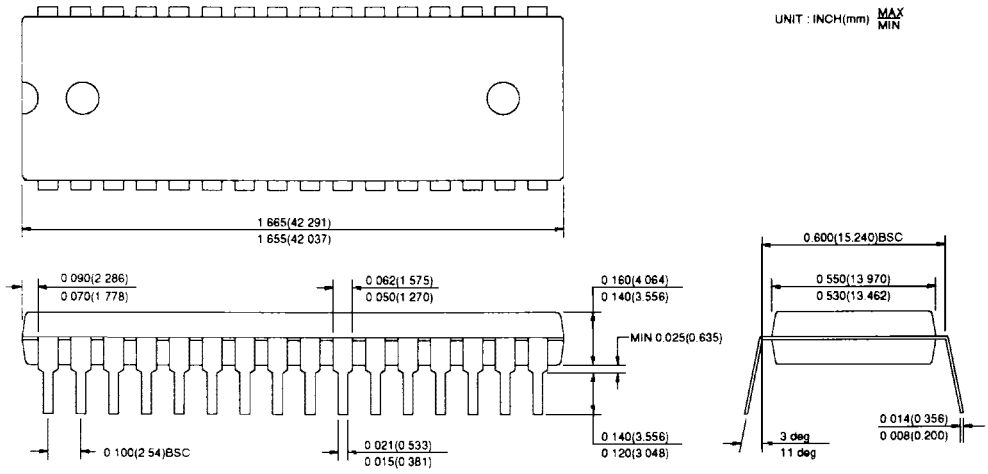


DATA RETENTION TIMING DIAGRAM 2

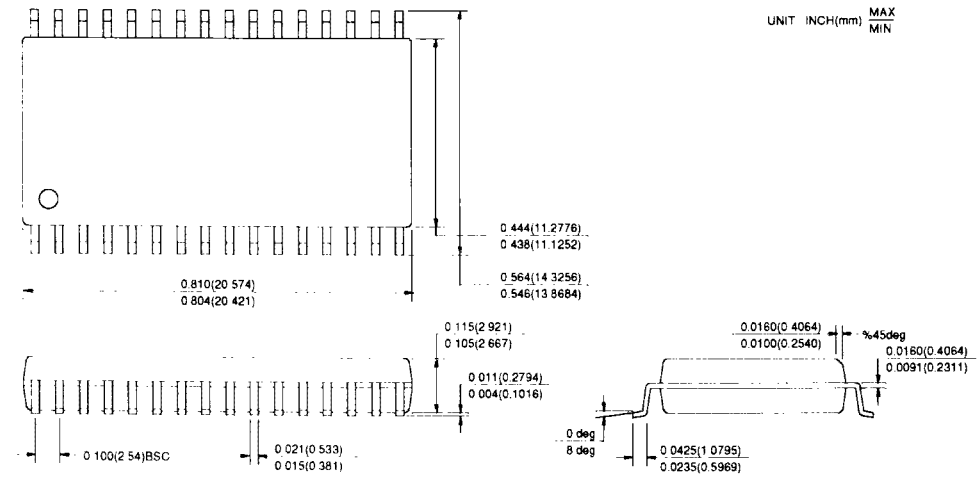


PACKAGE INFORMATION

600 mil 32 pin Plastic Dual In Line Package (P)

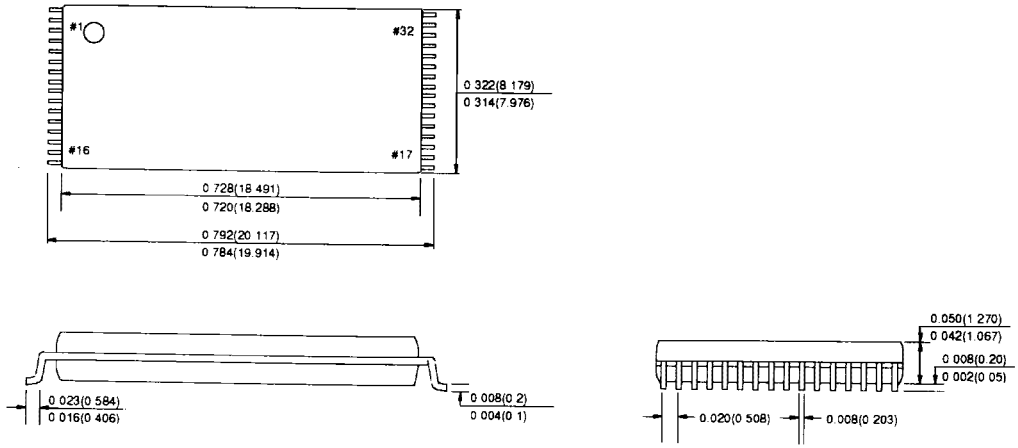


525 mil 32 pin Small Outline Package (G)



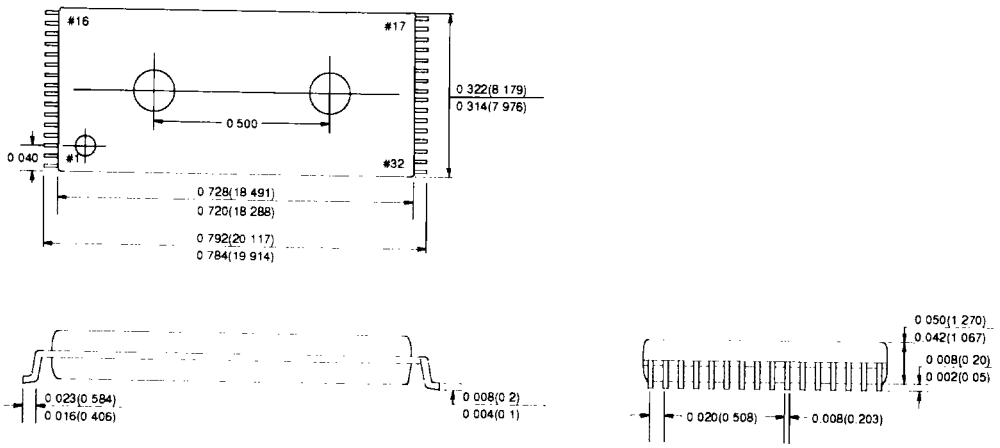
32 pin Thin Small Outline Package 8 x 20 mm Standard (T1)

UNIT : INCH(mm)



32 pin Thin Small Outline Package 8 x 20 mm Reversed (R1)

UNIT INCH(mm)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE	PART NO	SPEED	POWER	PACKAGE
HY628100P	70/85/100/120		PDIP	HY628100T1	70/85/100/120		TSOP-I
HY628100LP	70/85/100/120	L-part	PDIP	HY628100LT1	70/85/100/120	L-part	TSOP-I
HY628100LLP	70/85/100/120	LL-part	PDIP	HY628100LLT1	70/85/100/120	LLpart	TSOP-I
HY628100G	70/85/100/120		SOP	HY628100R1	70/85/100/120		TSOP-I(R)
HY628100LG	70/85/100/120	L-part	SOP	HY628100LR1	70/85/100/120	L-part	TSOP-I(R)
HY628100LLG	70/85/100/120	LL-part	SOP	HY628100LLR1	70/85/100/120	LL-part	TSOP-I(R)