MOTOROLA

# MC74AC845
# MC74ACT845
# MC74AC846
# MC74ACT846

*Product Preview*

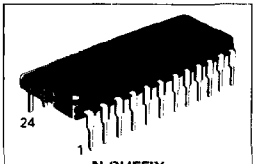
## 8-Bit Transparent Latch

**8-BIT TRANSPARENT LATCH**

The MC74AC845/74ACT845 and MC74AC846/74ACT846 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

The MC74AC845/74ACT845 is functionally and pin compatible with AMD's AM29845.

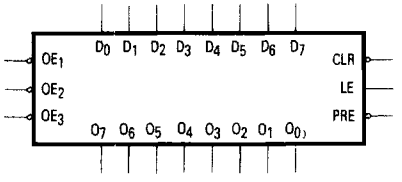
- 'ACT845 and 'ACT846 Have TTL Compatible Inputs



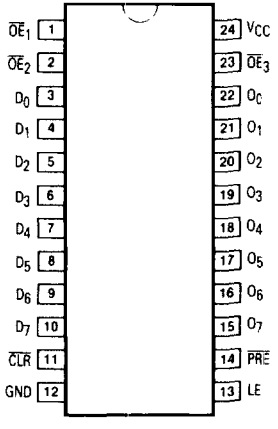

N SUFFIX
CASE 649-03
PLASTIC


DW SUFFIX
CASE 751E-02
PLASTIC

**LOGIC SYMBOL (MC74AC845/74ACT845)***




*The MC74AC846/74ACT846 has inverting outputs.




**PIN NAMES**

| | |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $O_0$–$O_7$ | Data Outputs (MC74AC845/74ACT845) |
| $\overline{O}_0$–$\overline{O}_7$ | Data Outputs (MC74AC846/74ACT846) |
| $\overline{OE}_1$–$\overline{OE}_3$ | Output Enables |
| LE | Latch Enable |
| $\overline{CLR}$ | Clear |
| $\overline{PRE}$ | Preset |

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

### FUNCTIONAL DESCRIPTION

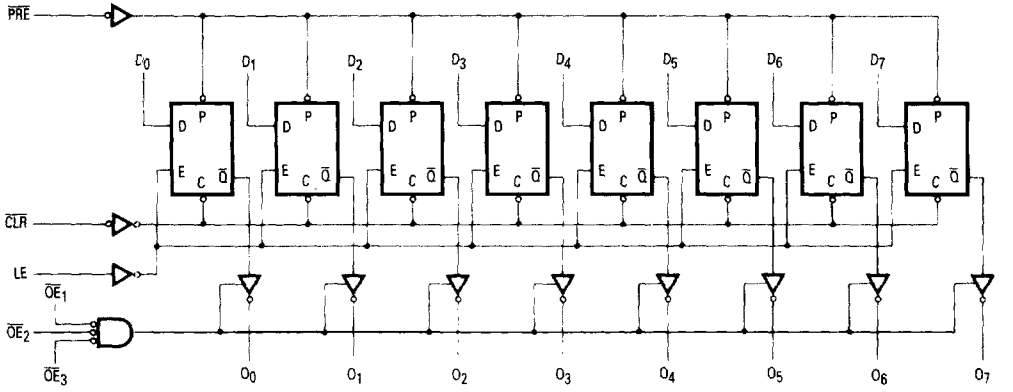
The MC74AC845/74ACT845 and MC74AC846/74ACT846 consist of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

### FUNCTION TABLE

| Inputs | | | | | Internal | Outputs | | Function |
|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{PRE}$ | $\overline{OE}_1$–$\overline{OE}_3$ | LE | D | Q | O ('845) | $\overline{O}$ ('846) | |
| H | H | H | H | L | L | Z | Z | High Z |
| H | H | H | H | H | H | Z | Z | High Z |
| H | H | H | L | X | NC | Z | Z | Latched |
| H | H | L | H | L | L | L | H | Transparent |
| H | H | L | H | H | H | H | L | Transparent |
| H | H | L | L | X | NC | NC | NC | Latched |
| H | L | L | X | X | H | H | L | Preset |
| L | H | L | X | X | L | L | H | Clear |
| L | L | L | X | X | H | H | L | Preset |
| L | H | H | L | X | L | Z | Z | Clear/High Z |
| H | L | H | L | X | H | Z | Z | Preset/High Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

### LOGIC DIAGRAM (MC74AC845/74ACT845)




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The MC74AC846/74ACT846 also has the same logic diagram with inverting outputs.

**DC CHARACTERISTICS** (unless otherwise specified)

| Symbol | Parameter | Value | Units | Test Conditions |
|---|---|---|---|---|
| $I_{CC}$ | Maximum Quiescent Supply Current | 80 | $\mu$A | $V_{IN}$ = $V_{CC}$ or Ground, $V_{CC}$ = 5.5 V, $T_A$ = Worst Case |
| $I_{CC}$ | Maximum Quiescent Supply Current | 8.0 | $\mu$A | $V_{IN}$ = $V_{CC}$ or Ground, $V_{CC}$ = 5.5 V, $T_A$ = 25°C |
| $I_{CCT}$ | Maximum Additional $I_{CC}$/Input ('ACT845/846) | 1.5 | mA | $V_{IN}$ = $V_{CC}$ − 2.1 V, $V_{CC}$ = 5.5 V, $T_A$ = Worst Case |

**AC CHARACTERISTICS** (For Figures and Waveforms — See Section 3)

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C, $C_L$ = 50 pF | | | 74AC $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay $D_n$ to $O_n$ | 3.3<br>5.0 | | 17<br>12 | | | | ns | 3-5 |
| $t_{PHL}$ | Propagation Delay $D_n$ to $O_n$ | 3.3<br>5.0 | | 16.5<br>11 | | | | ns | 3-5 |
| $t_{PLH}$ | Propagation Delay LE to $O_n$ | 3.3<br>5.0 | | 18.5<br>13 | | | | ns | 3-6 |
| $t_{PHL}$ | Propagation Delay LE to $O_n$ | 3.3<br>5.0 | | 17<br>12 | | | | ns | 3-6 |
| $t_{PLH}$ | Propagation Delay $\overline{PRE}$ to $O_n$ | 3.3<br>5.0 | | 17<br>12 | | | | ns | 3-6 |
| $t_{PHL}$ | Propagation Delay $\overline{CLR}$ to $O_n$ | 3.3<br>5.0 | | 17<br>12 | | | | ns | 3-6 |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 14.5<br>10 | | | | ns | 3-7 |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 11.5<br>8.0 | | | | ns | 3-8 |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 13<br>9.0 | | | | ns | 3-7 |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 3.3<br>5.0 | | 13<br>9.0 | | | | ns | 3-8 |

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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**AC OPERATING REQUIREMENTS**

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C, $C_L$ = 50 pF | | 74AC $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | Units | Fig. No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | |
| $t_s$ | Setup Time, HIGH or LOW $D_n$ to LE | 3.3<br>5.0 | 4.0<br>2.5 | | | ns | 3-9 |
| $t_h$ | Hold Time, HIGH or LOW $D_n$ to LE | 3.3<br>5.0 | 0<br>0 | | | ns | 3-9 |
| $t_w$ | LE Pulse Width, HIGH | 3.3<br>5.0 | 4.0<br>2.5 | | | ns | 3-6 |
| $t_w$ | $\overline{PRE}$ Pulse Width, LOW | 3.3<br>5.0 | 4.0<br>2.5 | | | ns | 3-6 |
| $t_w$ | $\overline{CLR}$ Pulse Width, LOW | 3.3<br>5.0 | 4.0<br>2.5 | | | ns | 3-6 |
| $t_{rec}$ | $\overline{PRE}$ Recovery Time | 3.3<br>5.0 | 5.0<br>4.0 | | | ns | 3-9 |
| $t_{rec}$ | $\overline{CLR}$ Recovery Time | 3.3<br>5.0 | 5.0<br>4.0 | | | ns | 3-9 |

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

**AC CHARACTERISTICS** (For Figures and Waveforms — See Section 3)

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C, $C_L$ = 50 pF | | | 74ACT $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | | 12 | | | | ns | 3-5 |
| $t_{PHL}$ | Propagation Delay $D_n$ to $O_n$ | 5.0 | | 11 | | | | ns | 3-5 |
| $t_{PLH}$ | Propagation Delay LE to $O_n$ | 5.0 | | 13.5 | | | | ns | 3-6 |
| $t_{PHL}$ | Propagation Delay LE to $O_n$ | 5.0 | | 12 | | | | ns | 3-6 |
| $t_{PLH}$ | Propagation Delay $\overline{PRE}$ to $O_n$ | 5.0 | | 12 | | | | ns | 3-6 |
| $t_{PHL}$ | Propagation Delay $\overline{CLR}$ to $O_n$ | 5.0 | | 12 | | | | ns | 3-6 |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | | 10 | | | | ns | 3-7 |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | | 18 | | | | ns | 3-8 |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | | 9.0 | | | | ns | 3-7 |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | | 9.0 | | | | ns | 3-8 |

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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**AC OPERATING REQUIREMENTS**

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C, $C_L$ = 50 pF | | 74ACT $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | Units | Fig. No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | |
| $t_s$ | Setup Time, HIGH or LOW $D_n$ to LE | 5.0 | 2.5 | | | ns | 3-9 |
| $t_h$ | Hold Time, HIGH or LOW $D_n$ to LE | 5.0 | 0 | | | ns | 3-9 |
| $t_w$ | LE Pulse Width, HIGH | 5.0 | 2.5 | | | ns | 3-6 |
| $t_w$ | $\overline{PRE}$ Pulse Width, LOW | 5.0 | 2.5 | | | ns | 3-6 |
| $t_w$ | $\overline{CLR}$ Pulse Width, LOW | 5.0 | 2.5 | | | ns | 3-6 |
| $t_{rec}$ | $\overline{PRE}$ Recovery Time | 5.0 | 5.0 | | | ns | 3-9 |
| $t_{rec}$ | $\overline{CLR}$ Recovery Time | 5.0 | 5.0 | | | ns | 3-9 |

*Voltage Range 5.0 is 5.0 V ± 0.5 V

**CAPACITANCE**

| Symbol | Parameter | Value Typ | Units | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | | pF | $V_{CC}$ = 5.0 V |

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