

DATA SHEET

74ABT126

Quad buffer (3-State)

Product data
Supersedes data of 1998 Jan 16

2002 Dec 13

Quad buffer (3-State)

74ABT126

FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64 mA / -32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT126 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	2.9	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V or } V_{CC}$	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{ V or } V_{CC}$	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	65	μA

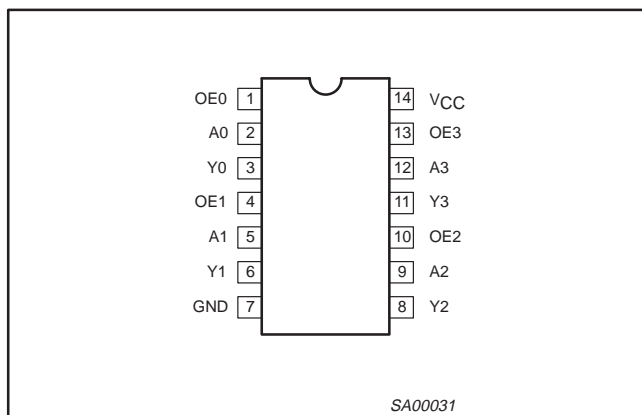
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
14-Pin plastic SO	-40 °C to +85 °C	74ABT126D	SOT108-1
14-Pin Plastic SSOP Type II	-40 °C to +85 °C	74ABT126DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40 °C to +85 °C	74ABT126PW	SOT402-1

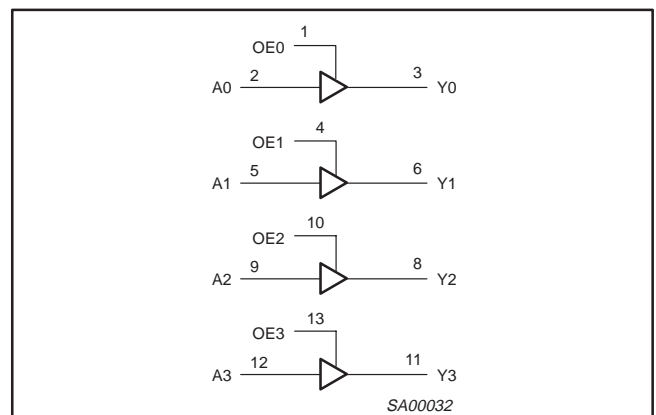
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	OE0 – OE3	Output enable inputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

PIN CONFIGURATION



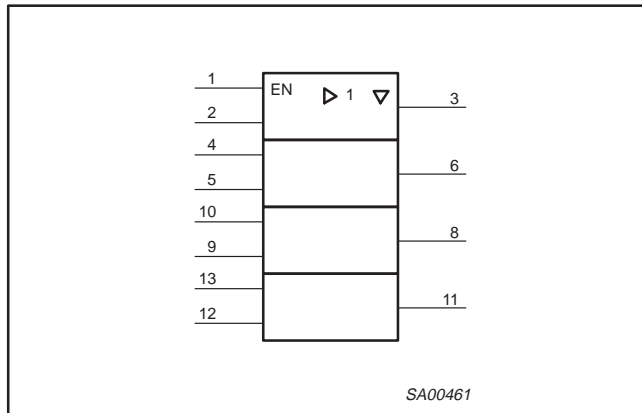
LOGIC SYMBOL



Quad buffer (3-State)

74ABT126

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
OEn	An	Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0 V	-50	mA
V _{OUT}	DC output voltage ³	output in Off or HIGH state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in LOW state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0		V
V _{IL}	LOW-level Input voltage		0.8	V
I _{OH}	HIGH-level output current		-32	mA
I _{OL}	LOW-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

Quad buffer (3-State)

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = -40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA		-0.9	-1.2		-1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}		0.35	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V		±5.0	±100		±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current ³	V _{CC} = 2.1 V; V _O = 0.5 V; V _I GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	µA
I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}		1.0	50		50	µA
I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}		-1.0	-50		-50	µA
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs High, V _I = GND or V _{CC}		65	250		250	µA
I _{CCL}		V _{CC} = 5.5 V; Outputs Low, V _I = GND or V _{CC}		12	15		15	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}		65	250		250	µA
ΔI _{CC}	Additional supply current per input pin ²	Outputs enabled, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V		50	250		250	µA
		Outputs 3-State, one enable input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10%, a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V; t_R = t_F = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

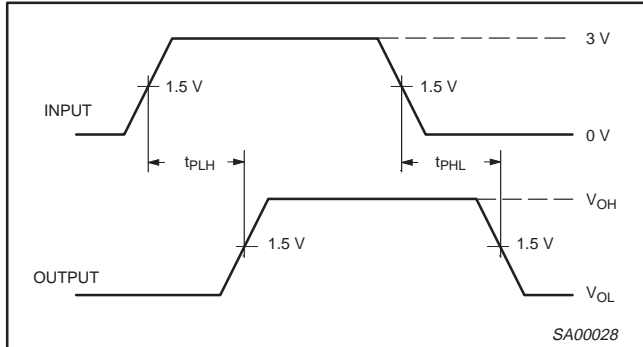
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = -40 °C to +85 °C V _{CC} = +5.0 V ± 0.5 V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.9 3.0	4.2 4.3	1.0 1.0	4.4 4.6	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	2	1.9 1.9	3.2 4.4	5.8 5.9	1.9 1.9	6.5 6.5	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	2	1.0 1.0	4.2 2.9	5.2 4.9	1.0 1.0	5.8 5.5	ns

Quad buffer (3-State)

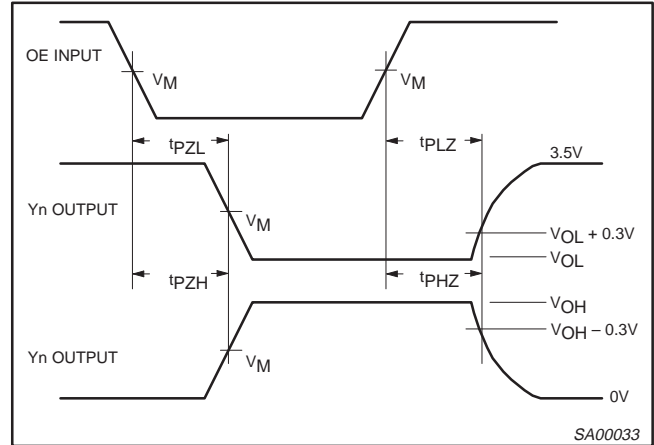
74ABT126

AC WAVEFORMS

$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$



Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

$V_M = 1.5\text{ V}$

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

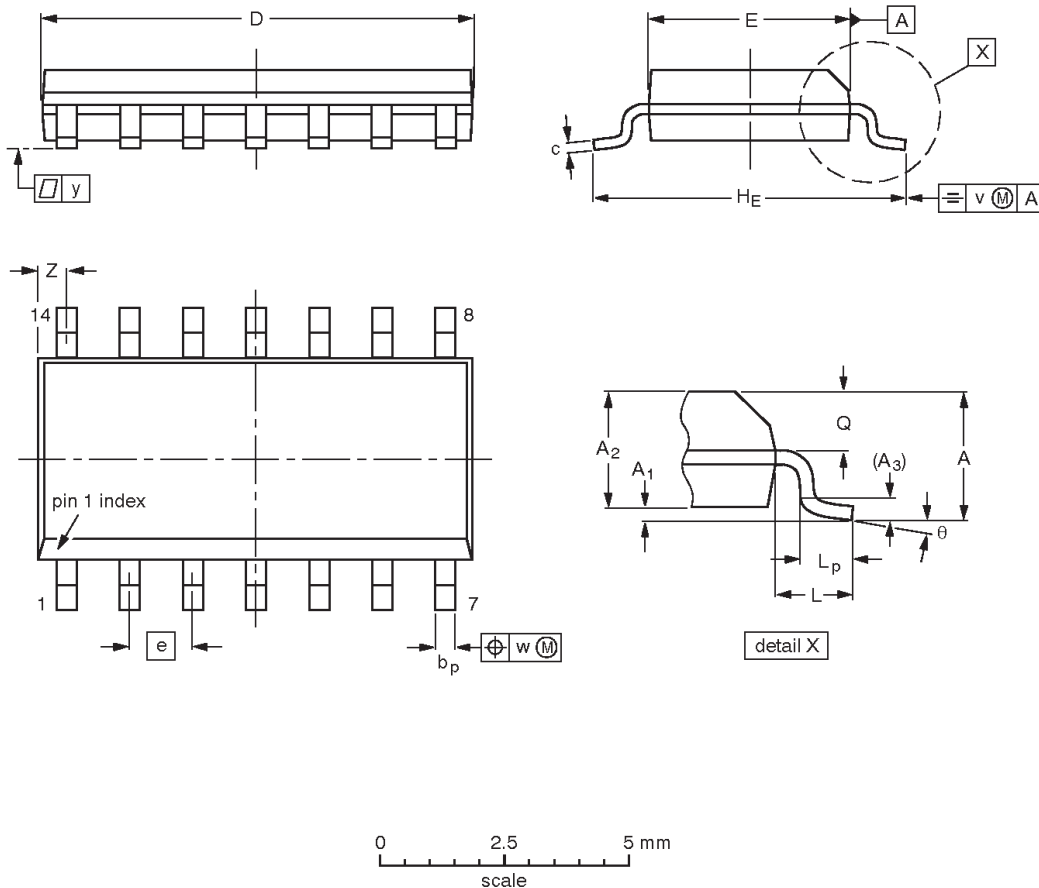
SA00012

Quad buffer (3-State)

74ABT126

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

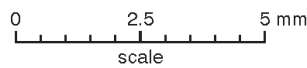
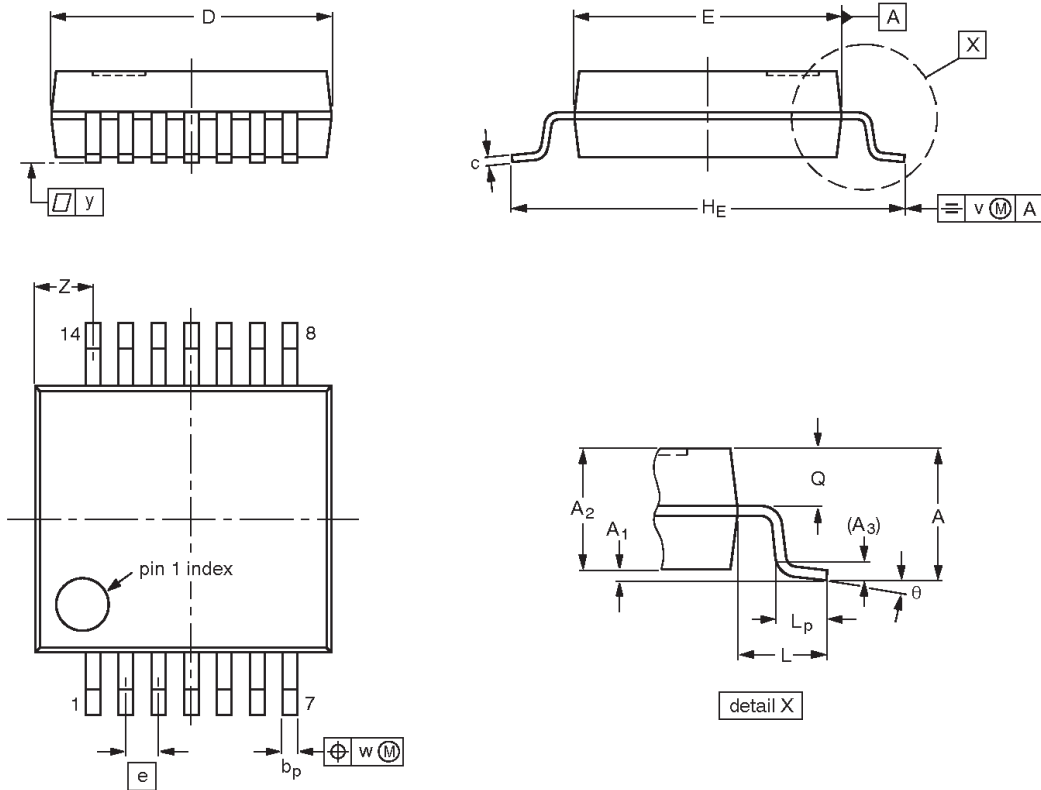
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

Quad buffer (3-State)

74ABT126

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

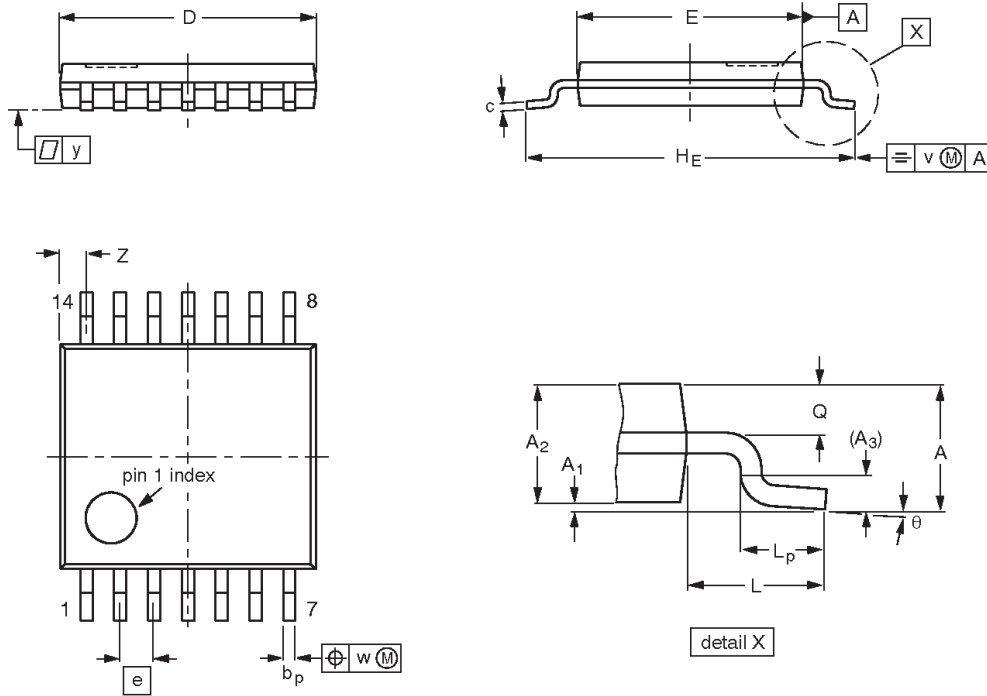
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				96-01-18 99-12-27

Quad buffer (3-State)

74ABT126

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-95-04-04 99-12-27

Quad buffer (3-State)

74ABT126

REVISION HISTORY

Rev	Date	Description
_3	20021213	Product data (9397 750 10856); ECN 853-1607 29291 of 12 December 2002. Supersedes data of 16 January 1998 (9397 750 03462). Modifications: <ul style="list-style-type: none">● Ordering information table: remove "North America" column; remove 74ABT126N package offering.
_2	19980116	Product specification (9397 750 03462). ECN 853-1607 18867 of 16 January 1998. Supersedes data of 26 February 1996.

Quad buffer (3-State)

74ABT126

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 10856

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74ABT126; Quad buffer (3-State)

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General description

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The 74ABT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

Features

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64 mA / -32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

Applications

- [AN203_2: Test Fixtures for High Speed Logic](#) (date 02-Apr-98)
- [AN2301: Simulation Support for Philips' Advanced BiCMOS Products](#)

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74ABT126	Quad buffer (3-State)	12/13/2002	Product specification	10	94	Download

□ Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74ABT126D	SOT108-1 (SO14)	Quad Buffer/Line Driver with Active HIGH Output Enable (3-State)	4~6	5 Volts +	14	None	TTL	High
74ABT126DB	SOT337-1 (SSOP14)	Quad Buffer/Line Driver with Active HIGH Output Enable (3-State)	4~6	5 Volts +	14	None	TTL	High
74ABT126PW	SOT402-1 (TSSOP14)	Quad Buffer/Line Driver with Active HIGH Output Enable (3-State)	4~6	5 Volts +	14	None	TTL	High

□ Products, packages, availability and ordering

<u>Type number</u>	<u>North American type number</u>	<u>Ordering code (12NC)</u>	<u>Marking/Packing</u>  IC packing info	<u>Package</u>	<u>Device status</u>	<u>Buy online</u>
74ABT126D	74ABT126D	9350 530 90602	Standard Marking * Tube (Signetics)	SOT108-1 (SO14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>
	74ABT126D-T	9350 530 90623	Standard Marking * Reel Pack, SMD, 13" (Signetics)	SOT108-1 (SO14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>
74ABT126DB	74ABT126DB	9351 812 90112	Standard Marking * Tube	SOT337-1 (SSOP14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>
	74ABT126DB-T	9351 812 90118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>
74ABT126PW	74ABT126PW	9352 010 70112	Standard Marking * Tube	SOT402-1 (TSSOP14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>
	74ABT126PW-T	9352 010 70118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	<input type="text" value="order this"/> <input type="text" value="-"/>

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

▣ Similar products

[74ABT126](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

▣ Support & tools

[ABT family characteristics, Family specifications](#)(date 01-Mar-98)

[Introduction to Advanced BiCMOS Logic Products](#)(date 01-Mar-98)

[Advanced BiCMOS features](#)(date 01-Jan-98)

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