# QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS 12-BIT 2:1 MUX/ DEMUX SWITCH WITH RESISTOR TERMINATION ON THE DEMUX SIDE

**IDTQS316292**

## FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot clamp diodes on all switch and control pins
- Available in 56-pin SSOP and TSSOP Packages

## APPLICATIONS

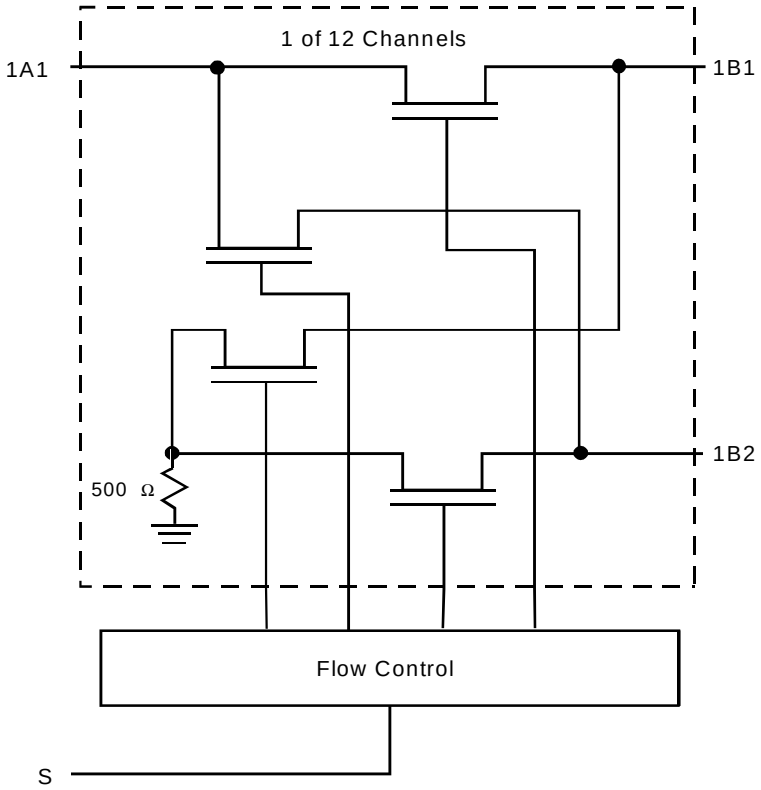
- Resource sharing
- Hot-docking
- Voltage translation (5V to 3.3V)

## DESCRIPTION:

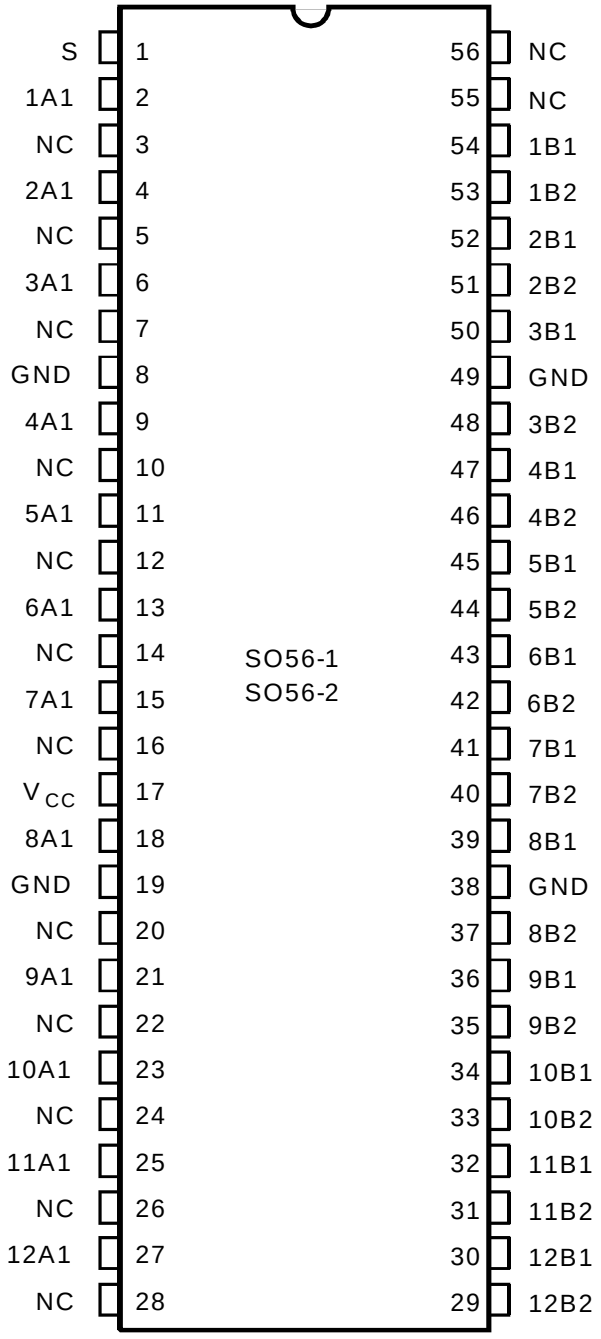
The QS316292 is a high-speed CMOS12-bit 2:1 multiplexer/demultiplexer switch with a 500Ω resistor termination to GND on the demultiplexer side to eliminate floating nodes. The low ON resistance of the QS316292 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise.

The QS316292 is characterized for operation at -40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SSOP/ TSSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | | Max. | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Supply Voltage to Ground | | – 0.5 to +7 | V |
| $V_{TERM}$(3) | DC Switch Voltage $V_S$ | | – 0.5 to +7 | V |
| $V_{TERM}$(3) | DC Input Voltage $V_{IN}$ | | – 0.5 to +7 | V |
| $V_{AC}$ | AC Input Voltage (pulse width ≤20ns) | | -3 | V |
| $I_{OUT}$ | DC Output Current | | 120 | mA |
| $P_{MAX}$ | Maximum Power | SSOP | .93 | W |
| | Dissipation ($T_A$ = 85°C) | TSSOP | .77 | |
| $T_{STG}$ | Storage Temperature | | – 65 to +150 | °C |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

## CAPACITANCE

**($T_A$ = +25°C, f = 1.0MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V)**

| Pins | Typ. | Max. (1) | Unit |
|---|---|---|---|
| Control Inputs | 4 | 5 | pF |
| Quickswitch Channels (Switch OFF) | 7.5 | 9 | pF |

**NOTE:**
1. This parameter is guaranteed but not production tested.

## PIN DESCRIPTION

| Pin Names | I/O | Description |
|---|---|---|
| $_1A_1$ - $_{12}A_1$ | I/O | Bus A |
| $_1Bn$ - $_{12}Bn$ | I/O | Bus B |
| S | I | Data Select |

## FUNCTION TABLE(1)

| S | $xA_1$ | Function |
|---|---|---|
| L | $xB_1$ | $xA_1$ to $xB_1$, $xB_2$ to GND through 500Ω |
| H | $xB_2$ | $xA_1$ to $xB_2$, $xB_1$ to GND through 500Ω |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level

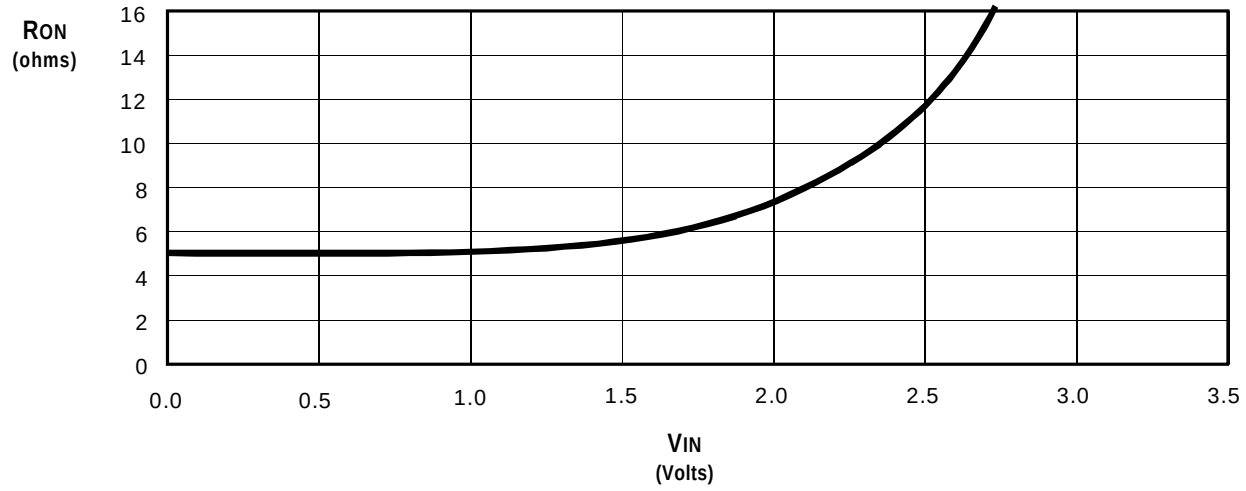
# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Industrial: $T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%**

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for Control Pins | 2 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for Control Pins | — | — | 0.8 | V |
| $I_{IN}$ | Input Leakage Current (Control Inputs) | $0V \le V_{IN} \le Vcc$ | — | — | ±1 | µA |
| $I_{OZ}$ | Off-State Current (Hi-Z) | $0V \le V_{OUT} \le Vcc$, Switches OFF | — | — | ±1 | µA |
| $I_{OS}$ | Short Circuit Current | A(B) = 0V B(A) = Vcc | -100 | — | — | mA |
| $V_{IK}$ | Clamp Diode Voltage | Vcc = Min., $I_{IN}$ = -18mA | — | -0.7 | -1.2 | V |
| $V_H$ | Input Hysterisis at Control Pins | — | — | 150 | — | mV |
| $R_{ON}$ | Switch ON Resistance (2) | Vcc = Min., $V_{IN}$ = 0V, $I_{ON}$ = 30mA | — | 5 | 7 | Ω |
| $R_{ON}$ | Switch ON Resistance (2) | Vcc = Min., $V_{IN}$ = 2.4V, $I_{ON}$ = 15mA | — | 10 | 14 | Ω |
| $V_P$ | Pass Voltage (3) | $V_{IN}$ = Vcc = 5V, $I_{OUT}$ = -5µA | 3.7 | 4 | 4.2 | V |

**NOTES:**
1. Typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C.
2. Max value of $R_{ON}$ is guaranteed but not production tested.
3. Pass voltage is guaranteed but not production tested.

# TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC}$ = 5V



# POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | Tyo. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or Vcc, f = 0 | 0.1 | 3 | µA |
| $\Delta I_{CC}$ | Power Supply Current per Control Input HIGH [2] | $V_{CC}$ = Max., $V_{IN}$ = 3.4V, f = 0 | — | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current per MHz[3] | $V_{CC}$ = Max., A and B pins open<br>Control Input Toggling at 50% Duty Cycle | — | 0.25 | mA/MHz |

**NOTES:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input ($V_{IN}$ = 3.4V). A and B pins do not contribute to ΔIcc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

# SWITCHING CHARACTERISTICS OVER OPERATING RANGE

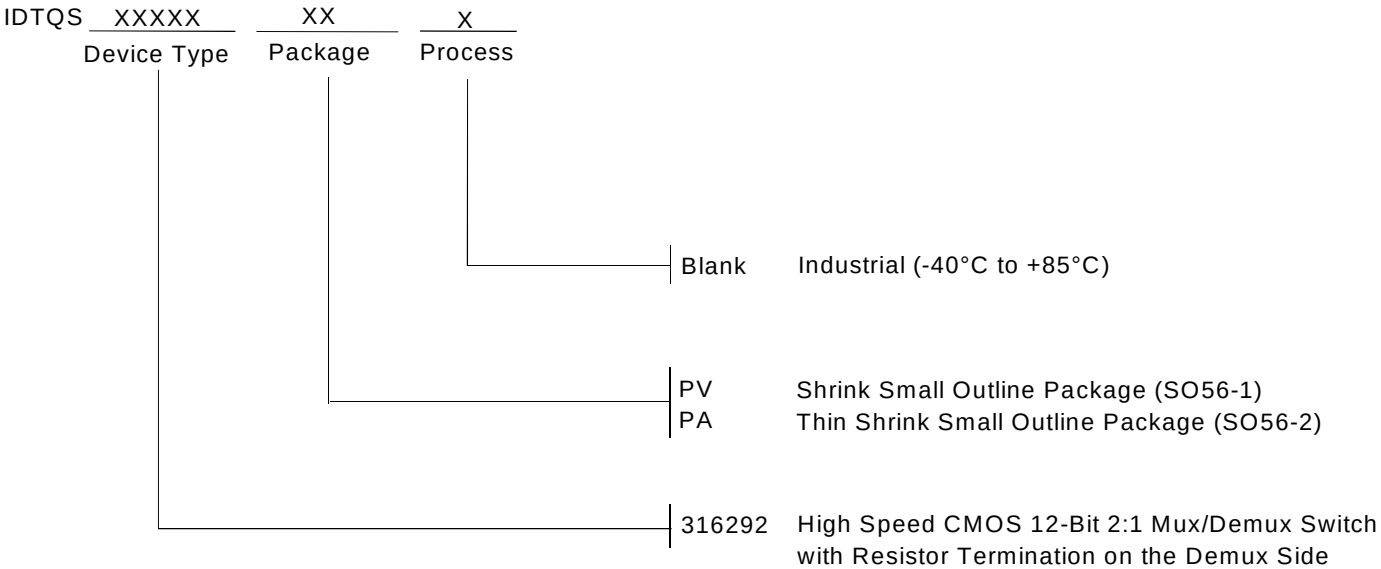
**$T_A$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%**

**$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.**

| Symbol | Parameter | Min. [1] | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Data Propagation Delay [2,3]<br>$xA_1$ to xBn, xBn to $xA_1$ | — | — | 0.25 [3] | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Switch Turn-on Delay [4]<br>S to $xA_1$ or xBn | 1.5 | — | 6.5 | ns |
| $t_{PLZ}$<br>$t_{PHZ}$ | Switch Turn-off Delay [2]<br>S to $xA_1$, xBn | 1.5 | — | 6.2 | ns |

**NOTES:**
1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The time constant for the switch alone is of the order of 0.25ns for $C_L$ = 50pF. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Switch turn-on delay from S to xBn is guaranteed but not production tested.

## ORDERING INFORMATION

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