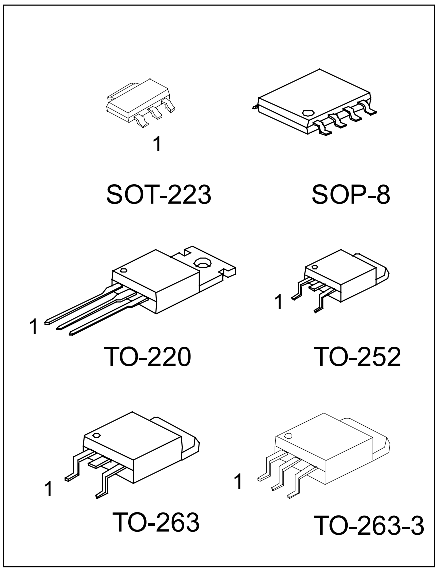
LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATORS



SOP-8 1: GND; 2,3,6,7: Vout;
4: Vin; 5,8: NC

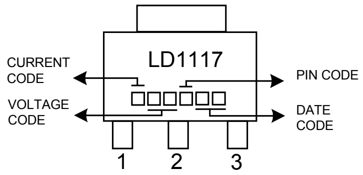
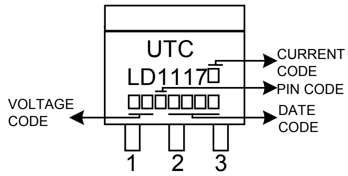
DESCRIPTION

The UTC LD1117/A is a LOW DROP Voltage Regulator able to provide up to 0.8/1.0A of Output Current, available even in adjustable version (Vref=1.25V). Concerning fixed versions, are offered the following Output Voltages: 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 3.6V and 5.0V. The 2.85V type is ideal for SCSI-2 lines active termination. The device is supplied in: SOT-223, TO-252, TO-263, TO-263-3, SOP-8 and TO-220. The SOT-223, TO-263, TO-263-3 and TO-252 surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in the case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common 10µF minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within ±1% at 25°C. The ADJUSTABLE LD1117/A is pin to pin compatible with the other standard Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.

FEATURES

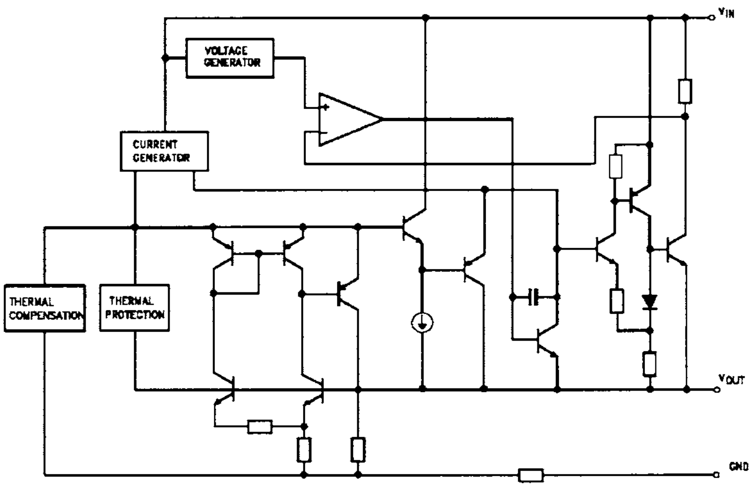
*Low dropout voltage (1V Typ.)
*2.85V device performances are suitable for SCSI-2 active termination
*Output current up to 0.8/1.0A
*Fixed output voltage of: 1.5V, 1.8V, 2.5V, 2,85V, 3.0V, 3.3V, 3.6V, 5.0V
*Adjustable version availability (Vref=1.25V)
*Internal current and thermal limit
*Available in ±1%(at 25°C) and 2% in all temperature range
*Supply voltage rejection: 75dB (TYP)
*Temperature range: 0°C to 125°C

MARKING INFORMATION

PACKAGE	VOLTAGE CODE	PIN CODE	PIN 1	PIN 2	PIN 3	MARKING
SOT-223	15:1.5V 18:1.8V	A	GND	OUT	IN	
	25:2.5V	B	OUT	GND	IN	
	28:2.85V	C	GND	IN	OUT	
	30:3.0V 33:3.3V	D	IN	GND	OUT	
TO-220 TO-252 TO-263 TO-263-3	36:3.6V	A	GND	OUT	IN	
	50:5.0V	B	OUT	GND	IN	
	AD:ADJ	C	GND	IN	OUT	
		D	IN	GND	OUT	

Note: The current code “A” means output current up to 1.0A, while without “A” means output current up to 0.8A.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

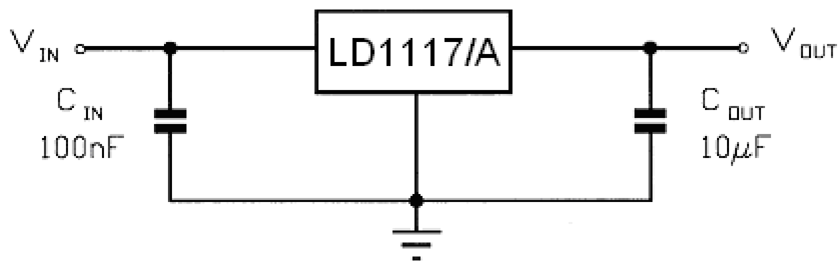
PARAMETER	SYMBOL	VALUE	UNIT
DC Input Voltage	V_{IN}	15	V
Power Dissipation	Ptot	12	W
Storage temperature	Tstg	-65 ~ +150	°C
Operating Junction Temperature	Top	0 ~ +125	°C

Note: Absolute Maximum Ratings are those value beyond which damage to the device may occur. Functional operation under there condition is not implied. Over the above suggested Max Power Dissipation a Short Circuit could definitively damage the device.

THERMAL DATA

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance Junction-case	Rth-case		
SOT-223		15	°C/W
SOP-8		20	°C/W
TO-252		8	°C/W
TO-220		3	°C/W
TO-263		3	°C/W
Thermal Resistance Junction-ambient	Rthj-amb		
TO-220		50	°C/W

APPLICATION CIRCUIT



UTC LD1117/A-1.5 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=3.5V, Io=10mA, Tj=25°C	1.485	1.500	1.515	VV
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=3 to 8V	1.470	1.500	1.530	V
Line Regulation	ΔVo	Vin=3 to 8V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=3V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤10V		5	10	mA
Output Current	Io	Vin=6.5V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=4.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000 mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-1.8 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=3.8V, Io=10mA, Tj=25°C	1.780	1.800	1.820	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=3.3 to 8V	1.760		1.840	V
Line Regulation	∆Vo	Vin=3.3 to 8V, Io=0mA		1	6	mV
Load Regulation	∆Vo	Vin=3.3V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	∆Vo			0.5		%
Long Term Stability	∆Vo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			10	V
Quiescent Current	Id	Vin≤8V		5	10	mA
Output Current	Io	Vin=6.8V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.5 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=4.5V, Io=10mA, Tj=25°C ±1% ±2%	2.475 2.450	2.500 2.500	2.525 2.550	V V
Output Voltage	Vo	Io=0 to 800/1000mA, ±2% Vin=3.9 to 10V ±4%	2.450 2.400		2.550 2.600	V V
Line Regulation	∆Vo	Vin=3.9 to 10V, Io=0mA		1	6	mV
Load Regulation	∆Vo	Vin=3.9V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	∆Vo			0.5		%
Long Term Stability	∆Vo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤10V		5	10	mA
Output Current	Io	Vin=7.5V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.85 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=4.85V, Io=10mA, Tj=25°C	2.82	2.85	2.88	V
Output Voltage	Vo	Io=0 to 800/1000mA,Vin=4.25 to 10V	2.79		2.91	V
Line Regulation	∆Vo	Vin=4.25 to 10V, Io=0mA		1	6	mV
Load Regulation	∆Vo	Vin=4.25V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	∆Vo			0.5		%
Long Term Stability	∆Vo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤10V		5	10	mA
Output Current	Io	Vin=7.85V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.85V, Vripple=1Vpp	60	75		DB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=5V, Io=10mA, Tj=25°C ±1% ±2%	2.97 2.94	3.00 3.00	3.03 3.06	V V
Output Voltage	Vo	Io=0 to 800/1000mA, ±2% Vin=4.5 to 10V ±4%	2.94 2.88		3.06 3.12	V V
Line Regulation	∆Vo	Vin=4.5 to 12V, Io=0mA		1	6	mV
Load Regulation	∆Vo	Vin=4.5V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	∆Vo			0.5		%
Long Term Stability	∆Vo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤12V		5	10	mA
Output Current	Io	Vin=8V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.3 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=5.3V, Io=10mA, Tj=25°C ±1% ±2%	3.267 3.235	3.300 3.300	3.333 3.365	V V
Output Voltage	Vo	Io=0 to 800/1000mA, ±2% Vin=4.75 to 10V ±4%	3.235 3.160		3.365 3.440	V V
Line Regulation	ΔVo	Vin=4.75 to 15V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=4.75V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤15V		5	10	mA
Output Current	Io	Vin=8.3V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6.3V, Vripple=1Vpp	60	75		DB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.6 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10µF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=5.6V, Io=10mA, Tj=25°C	3.564	3.600	3.636	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=5 to 10V	3.528	3.600	3.672	V
Line Regulation	ΔVo	Vin=5 to 15V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=5V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤15V		5	10	mA
Output Current	Io	Vin=8.6V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		µV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6.6V, Vripple=1Vpp	60	75		DB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-5.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=7V, Io=10mA, Tj=25°C ±1% ±2%	4.95 4.90	5.00 5.00	5.05 5.10	V V
Output Voltage	Vo	Io=0 to 800/1000mA, ±2% Vin=6.5 to 15V ±4%	4.90 4.80		5.10 5.20	V V
Line Regulation	ΔVo	Vin=6.5 to 15V, Io=0mA		1	10	mV
Load Regulation	ΔVo	Vin=6.5V, Io=0 to 800/1000mA		1	15	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤15V		5	10	mA
Output Current	Io	Vin=10V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=8V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-ADJUSTABLE ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	Vref	Vin-VO=2V, Io=10mA, Tj=25°C	1.238	1.25	1.262	V
Reference Voltage	Vref	Io=10 to 800/1000mA, Vin-Vo=1.4 to 10V	1.225		1.275	V
Line Regulation	ΔVo	Vin-Vo=1.5 to 13.75V, Io=10mA		0.035	0.200	%
Load Regulation	ΔVo	Vin-Vo=3V, Io=10 to 800/1000mA		0.10	0.400	%
Temperature stability	ΔVo			0.50		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin				15	V
Adjustment Pin Current	Iadj	Vin≤15V		60	120	μA
Adjustment Pin Current Change	ΔIadj	Vin-Vo=1.4 to 10V, Io=10 to 800/1000mA		1	5	μA
Minimum Load Current	Io(min)	Vin=15V		2	5	mA
Output Current	Io	Vin-Vo=5V, Tj=25°C	800	950	1200	mA
Output Noise (%Vo)	eN	B=10Hz to 10KHz, Tj=25°C		0.003		%
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin-Vo=3V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA Io=500mA Io=800mA Io=1000mA		1.00 1.15 1.20 1.20	1.10 1.25 1.30 1.30	V V V V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

TYPICAL APPLICATIONS

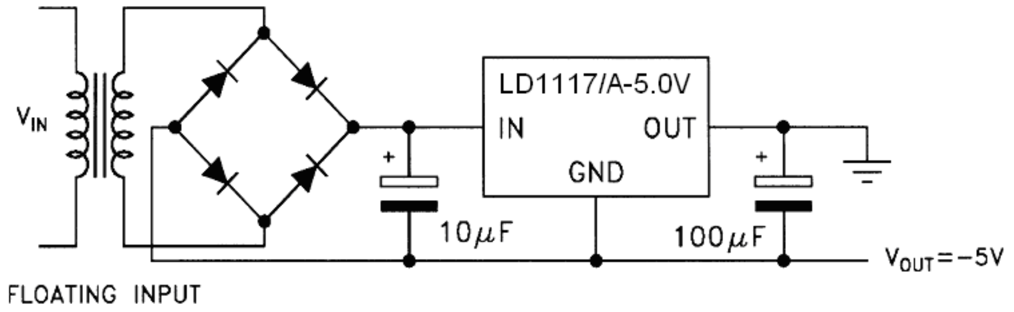


FIG.1 Negative Supply

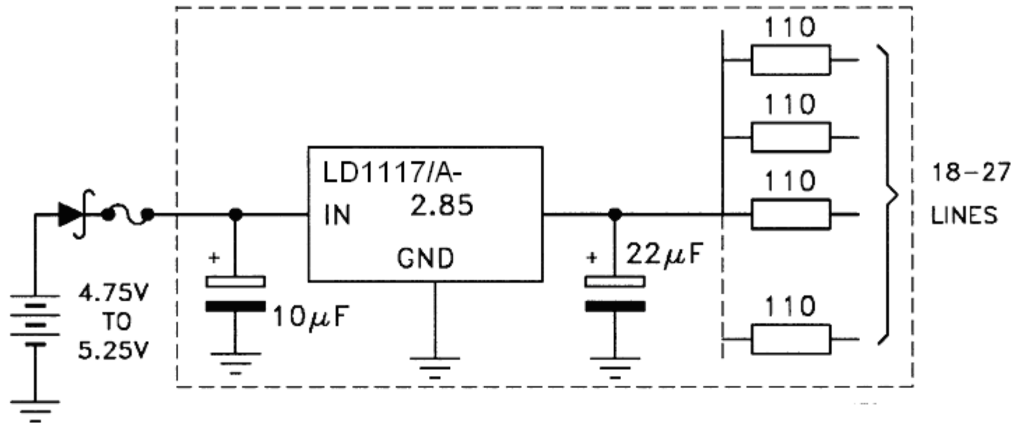


FIG.2 Active Terminator for SCSI-2 BUS

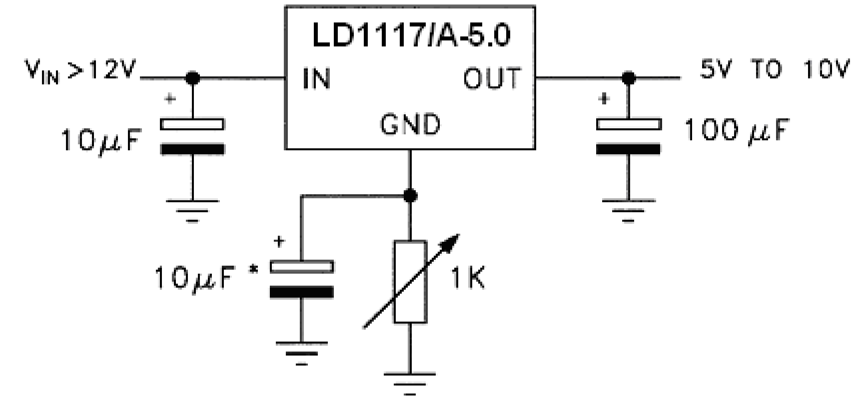


FIG.3 Circuit for Increasing Output Voltage

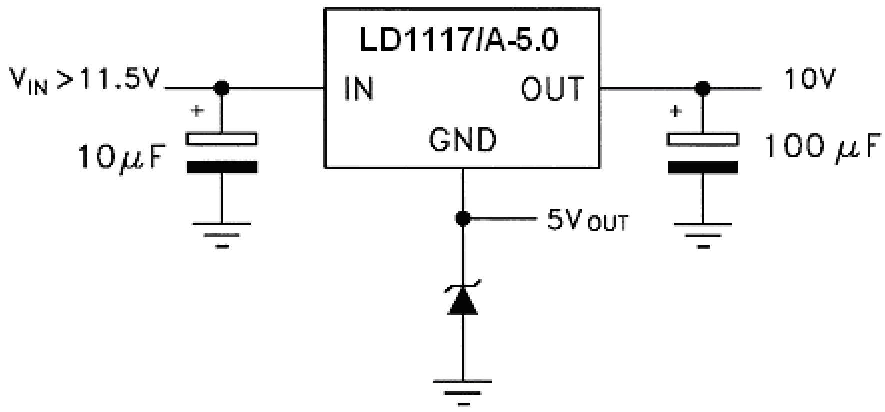


FIG.4 Voltage Regulator With Reference

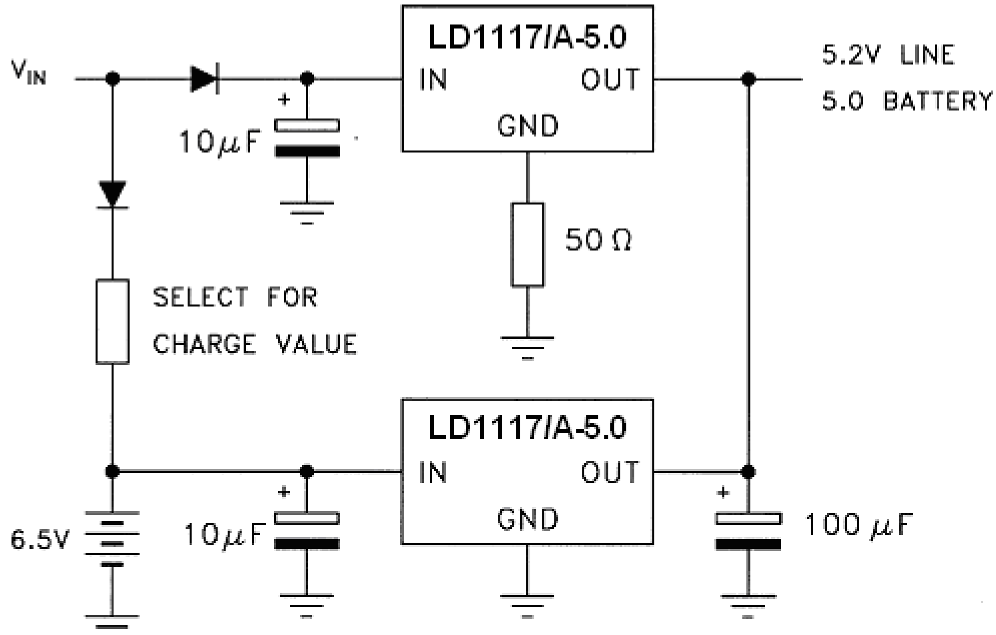


FIG.5 Battery Backed-up Regulated Supply

FEEDBACK PATH

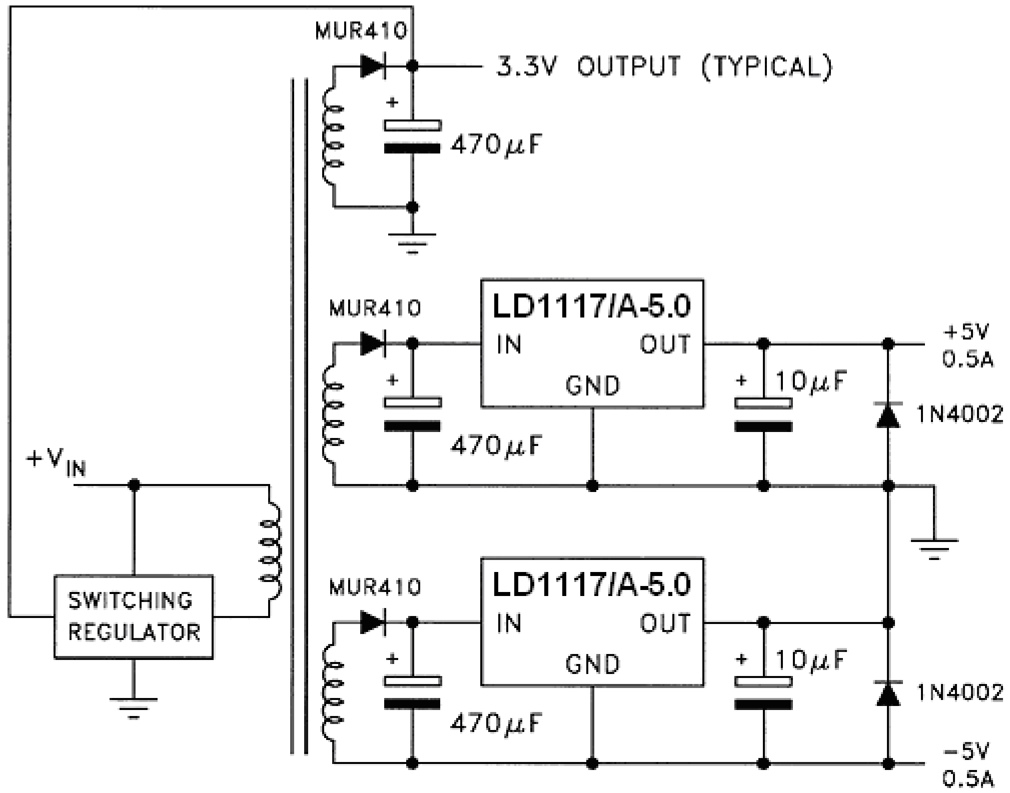


FIG.6 Post-Regulated Dual Supply

LD1117/A ADJUSTABLE APPLICATION NOTE

The LD1117/A ADJUSTABLE has a thermal stabilized 1.25±0.012V reference voltage between the OUT and ADJ pins. I_{ADJ} is 60µA typ. (120µA max.) and ΔI_{ADJ} is 1µA typ. (5µA max.).
R1 is normally fixed to 120Ω. From figure 7 we obtain:
$V_{OUT}=V_{REF}+R2(I_{ADJ}+I_{R1})=V_{REF}+R2(I_{ADJ}+V_{REF}/R1)=V_{REF}(1+R2/R1)+R2 \times I_{ADJ}$.
In normal application R2 value is in the range of few Kohm,, so the R2 X I_{ADJ} product could not be considered in the V_{OUT} calculation; then the above expression becomes: $V_{OUT}=V_{REF}(1+R2/R1)$
In order to have the better load regulation it is important to realize a good Kelvin connection of R1 and R2 resistors. In particular R1 connection must be realized very close to OUT and ADJ pin, while R2 ground connection must be placed as near as possible to the negative Load pin. Ripple rejection can be improved by introducing a 10µF electrolytic capacitor placed in parallel to the R2 resistor (See Fig. 8)

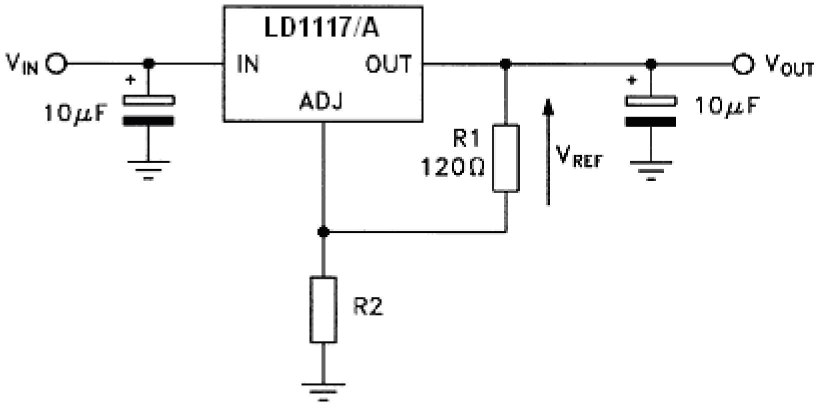


FIG.7 Adjustable Output Voltage Application Circuit

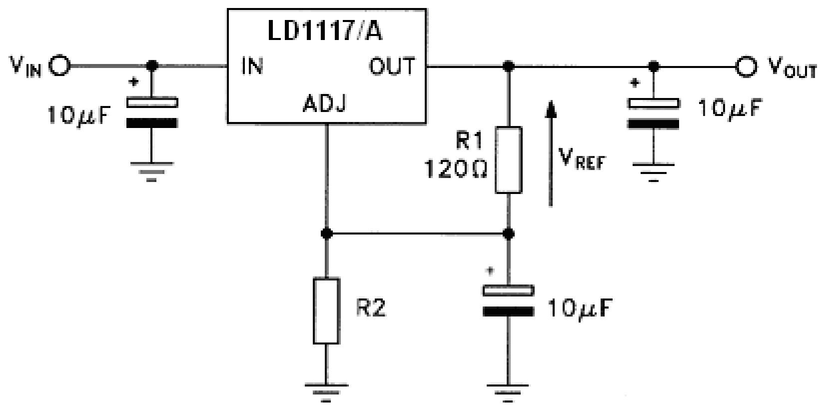


FIG.8 Adjustable Output Voltage Application with improved Ripple Rejection.

TYPICAL CHARACTERISTICS

Fig.1 Reference Voltge vs. Temperature

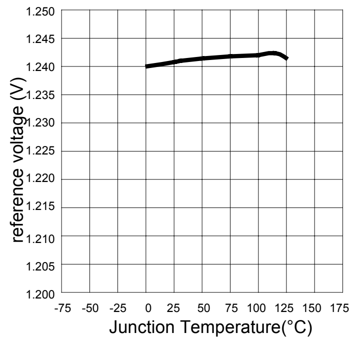


Fig.2 Output Voltage vs. Temperautre

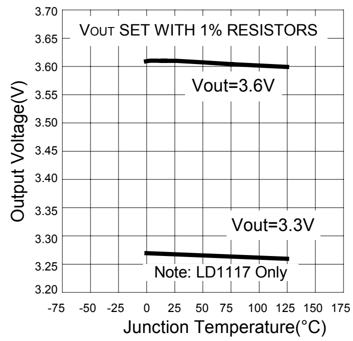


Fig.3 Maximum Power Dissipation