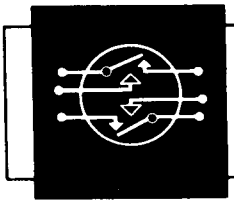

LOW R_{on} DUAL FET ANALOG GATES
SPST AND DPST

CAG13, 13A, 13C, 13D, 24, 27, 27-10, 42

- WILL CONNECT AS SPDT AND DPDT
- BREAK BEFORE MAKE ACTION
- ± 10V SIGNAL LEVELS
- WORK FROM DTL, TTL, HNIL AND MOS LOGIC
- 20 V_{PP} SIGNAL LEVELS AC OR DC WITH CAG42

ELECTRICAL SPECIFICATIONS: T_A = +25°C V_{CC} = +15V, V_{EE} = -18V (unless otherwise specified)

PARAMETER	TYPE SYMBOL	TEST CONDITIONS	ALL EXCEPT CAG24			CAG24			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
* Power Drain	Pt/Ckt.	V_{IN} = + 3V	–	65	90	–	5	6	mW
* Logic "1" Current	$I_{IN}(1)$	V_{IN} = + 2.4V	–	320	400	–	32	40	µA
* Logic "0" Current	$I_{IN}(0)$	V_{IN} = + 0V	–	–	50	–	–	50	µA

PARAMETER	TYPE SYMBOL	TEST CONDITIONS	ALL EXCEPT CAG27,CAG27-10			CAG27 CAG27-10			UNITS
			MIN	TYP.	MAX.	MIN.	TYP.	MAX.	
* Drain to Gate Capacitance	C_{dgo}	V_{DG}=10V, I_S=0, f=140KHz	–	6	8	–	18	25	pfd
* Source to Gate Capacitance	C_{sgo}	V_{SG}=10V, I_D=0, f=140KHz	–	6	8	–	18	25	pfd
* Signal Current Limit	$I_{SIG-LIM}$	V_{DS}=2V, V_{GS}=0	10	–	–	100	–	–	mA
Off Leakage Current	$I_{D\ (off)}$	$V_{SIG}=V_{SIG\ (MIN)}$	–	0.5	1.0	–	0.5	3.0	nA
* Off Leakage Current	$I_{D\ (off)}$ (125°C)	$V_{SIG}=V_{SIG\ (MIN)}$	–	1	2	–	1	2	µA

SYMBOL (Units) PARAMETER			V_{SIG} (V) SIGNAL VOLTAGE RANGE			$R_{ds}(\Omega)$ DRAIN SOURCE ON-RESISTANCE			R_{ds}(125° C) (Ω) DRAIN SOURCE ON-RESISTANCE			**t_{on} (µsec) TURN-ON TIME			**t_{off} (µsec) TURN-OFF TIME		
TYPE	PKG.	DIA.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
CAG13	TO-100	L1	–10	–	+10	20	35	50	–	–	100	–	0.4	0.5	–	0.2	0.5
CAG13A	TO-100	L1	–10	–	+10	20	35	50	–	–	100	–	0.4	0.5	–	0.2	0.5
CAG13C	TO-87	L2	–10	–	+10	20	35	50	–	–	100	–	0.4	0.5	–	0.2	0.5
CAG13D	TO-8	L3	–10	–	+10	20	35	50	–	–	100	–	0.4	0.5	–	0.2	0.5
CAG24	TO-8	L3	–6	–	+10	15	25	30	–	–	60	–	3.0	10	–	1.0	10
CAG27	TO-8	L3	–6	–	+10	3	5	6	–	–	12	–	2.0	3.0	–	1.0	3.0
CAG27-10	TO-8	L3	–6	–	+10	4	7	10	–	–	20	–	2.0	3.0	–	1.0	3.0
CAG42	TO-100	L1	–10	–	+10	20	35	50	–	–	100	–	0.7	1.0	–	0.4	1.0

* These parameters guaranteed but may not be tested.
** Includes Propagation Delay

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MAXIMUM RATINGS

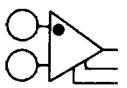
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Operating Temperature	T_{op}	-55	-	+125	°C
Storage Temperature	T_{stg}	-65	-	+150	°C
Pos. Supply Voltage	V_{CC}	0	15	18	V
Neg. Supply Voltage	V_{EE}	-6	-15	-18	V

The series consists of 2 completely separate FET Analog Switch Circuits capable of switching up to ±10V signals and being controlled directly from most logic circuits. Besides its inherent zero offset voltage and low R_{on} the circuit is unique in that it turns off faster than on allowing multiplexing without cross talk. When in the off or open state the FET gate is AC grounded lowering high frequency signal feedthrough by at least 10 dB over otherwise equivalent circuits. Separate Logic grounds allow over ±10V noise immunity with respect to signal or supply grounds.

Logic 1 ($\geq$2.4V) opens contacts

Logic 0 ($\leq$0.6V) closes contacts

See Page 12 for other logic connections:



NOTES:

1) The CAG42 will switch AC as well as DC signals. The other circuits may present difficulties when attempting to pass high level AC signals. See application note "Fet Analog Gate fails to switch AC."

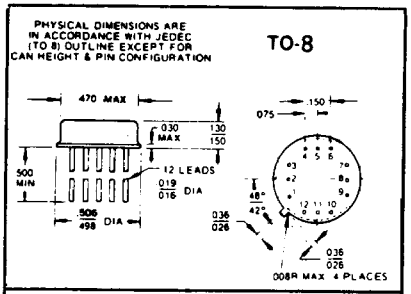
2) The CAG13C, CAG13D, CAG24 and CAG27 will have access to the FET gate leads for compensation.

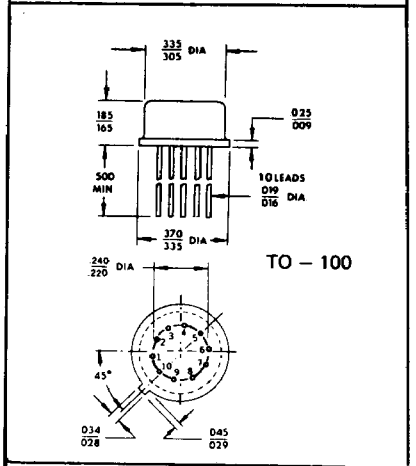
3) The CAG24 is specifically for low power drain applications and is compatible with Low Level Logic.

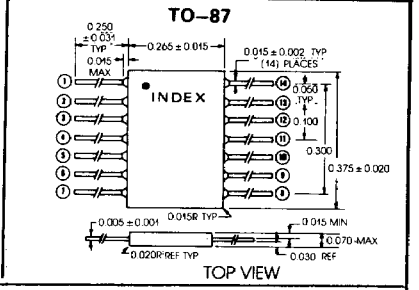
4) The CAG13A is Direct Coupled for AC switching without compensation. It draws approximately 1.0 mA from the signal source.

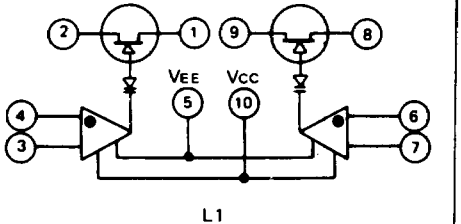
5) SWITCHING TIMES are measured with a 300 Ohm load. When used as a SPDT switch, the turn-off time may appear longer than specified if switching into a high impedance load. The apparent toff is then actually the settling time of the FET capacitance and load impedance.

CAG13 thru CAG27-10

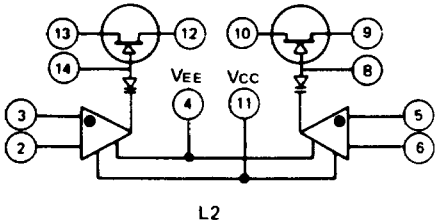




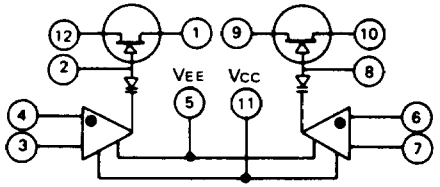




L1

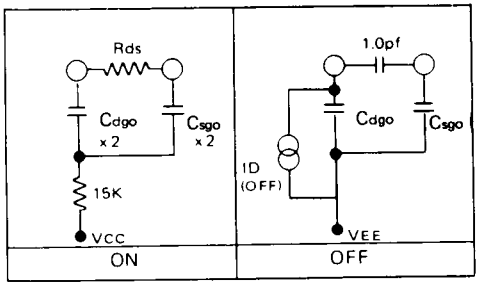


L2



L3

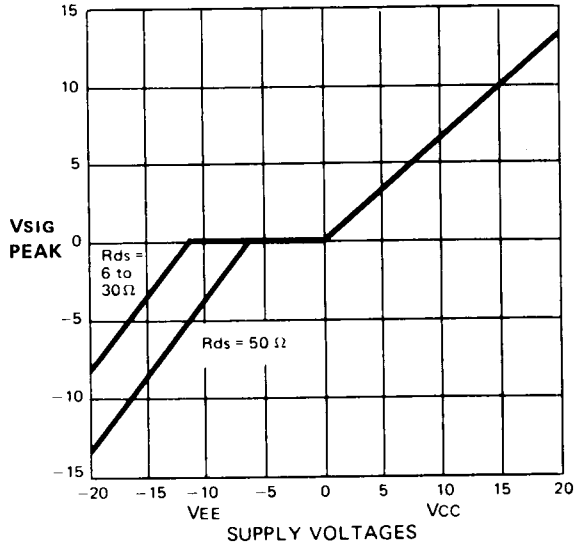
EQUIVALENT CIRCUITS



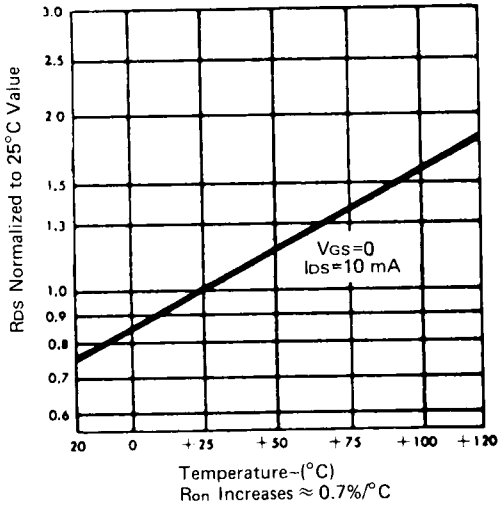
LOGIC CONNECTIONS

ON (CLOSED)	OFF (OPEN)	LOGIC
(0V) Logic 0	(+3V) Logic 1	DTL/TTL NORMAL
+3V Logic 1 (+3V)	+3V Logic 0 (0V)	DTL/TTL INVERTED
Logic 0 (0V)	Logic 1 (-10V)	MOS
LOGIC — +3V		DTL/TTL DOUBLE THROW

VSIG RANGE VS. VCC AND VEE



ON RESISTANCE VS. TEMPERATURE



OFF LEAKAGE CURRENT VS. TEMPERATURE