512Kx32 SRAM MODULE *ADVANCED**

FEATURES

- Access Times of 17, 20, 25, 35ns
- Packaging
  - Module is manufactured with four 512Kx8 SRAM memory devices on laminate substrate
  - 72 pin SIMM, JEDEC Standard Pinout
  - 72 pin ZIP
- Organized as 512Kx32
- Commercial Temperature Range
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WPS512K32-XXC

TOP VIEW

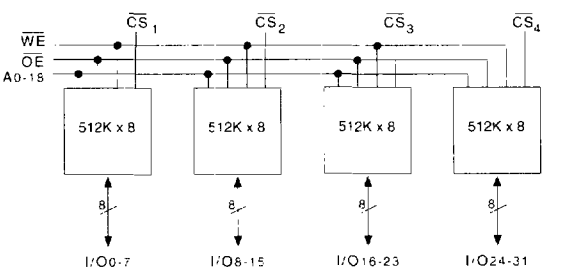
NC	1	$\overline{CS4}$	37
NC	2	CS3	38
PD2	3	A17	39
PD3	4	A16	40
GND	5	$\overline{OE}$	41
PD0	6	GND	42
PD1	7	I/O24	43
I/O0	8	I/O16	44
I/O8	9	I/O25	45
I/O1	10	I/O17	46
I/O9	11	I/O26	47
I/O2	12	I/O18	48
I/O10	13	I/O27	49
I/O3	14	I/O19	50
I/O11	15	A3	51
Vcc	16	A10	52
A0	17	A4	53
A7	18	A11	54
A1	19	A5	55
A8	20	A12	56
A2	21	Vcc	57
A9	22	A13	58
I/O12	23	A6	59
I/O4	24	I/O20	60
I/O13	25	I/O28	61
I/O5	26	I/O21	62
I/O14	27	I/O29	63
I/O6	28	I/O22	64
I/O15	29	I/O30	65
I/O7	30	I/O23	66
GND	31	I/O31	67
$\overline{WE}$	32	GND	68
A15	33	A18	69
A14	34	NC	70
$\overline{CS2}$	35	NC	71
CS1	36	NC	72

PD0	—	open
PD1	—	open
PD2	—	GND
PD3	—	open

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
PD_{0-3}	Presence Detect
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_{STG}	-55	+125	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	0	+70	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	60	pF
$\overline{WE}$	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	60	pF
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	18	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	60	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		520	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = 0°C to +70°C)

Parameter Read Cycle	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	17		20		25		35		ns
Address Access Time	tAA		17		20		25		35	ns
Output Hold from Address Change	tOH	0		0		0		0		ns
Chip Select Access Time	tACS		17		20		25		35	ns
Output Enable to Output Valid	tOE		9		10		12		25	ns
Chip Select to Output in Low Z	tCLZ[1]	2		2		2		2		ns
Output Enable to Output in Low Z	tOLZ[1]	0		0		0		0		ns
Chip Disable to Output in High Z	tCHZ[1]		8		9		10		10	ns
Output Disable to Output in High Z	tOHZ		8		9		10		10	ns

1. This parameter is guaranteed by design but not tested.

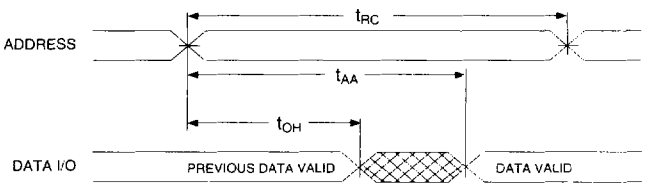
AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = 0°C to +70°C)

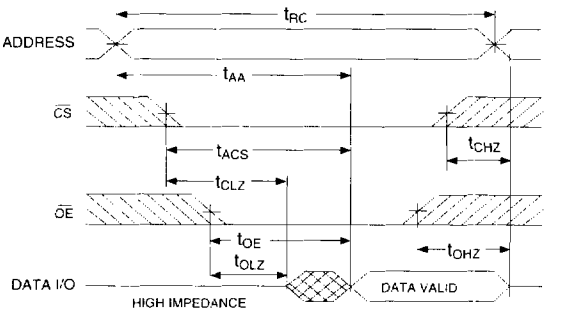
Parameter Write Cycle	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17		20		25		35		ns
Chip Select to End of Write	tCW	13		13		15		25		ns
Address Valid to End of Write	tAW	13		13		15		25		ns
Data Valid to End of Write	tDW	9		10		11		20		ns
Write Pulse Width	tWP	13		13		15		25		ns
Address Setup Time	tAS	0		0		0		0		ns
Address Hold Time	tAH	0		0		0		0		ns
Output Active from End of Write	tOW[1]	3		3		3		3		ns
Write Enable to Output in High Z	tWHZ[1]		9		11		13		15	ns
Data Hold Time	tDH	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
TIMING WAVEFORM - READ CYCLE

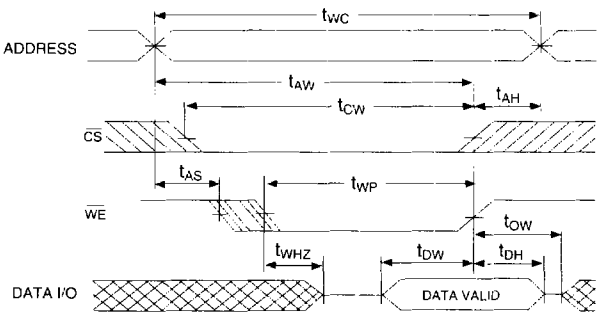


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



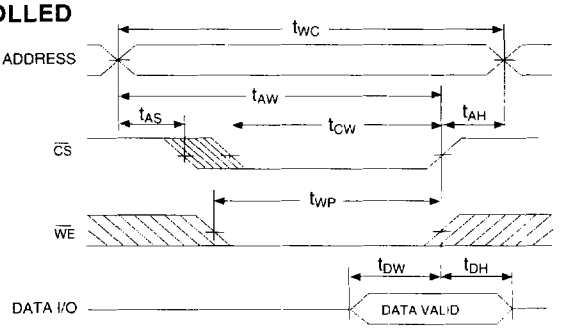
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED



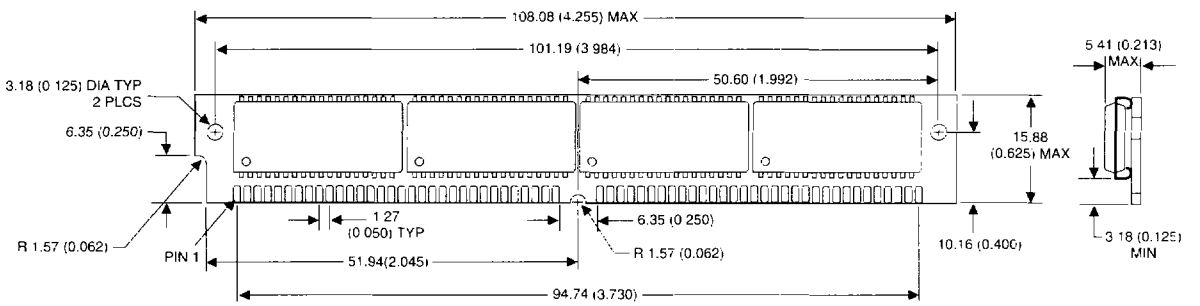
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED



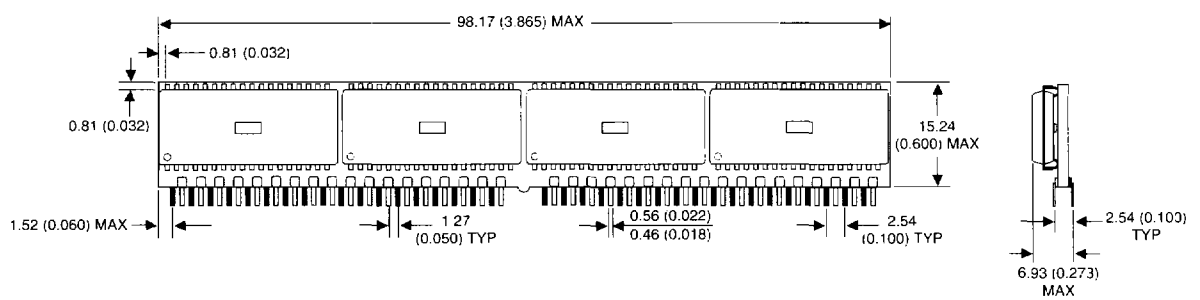
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

FIG. 5
PACKAGE DRAWING 72-PIN SIMM



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 6
PACKAGE DRAWING 72-PIN ZIP



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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