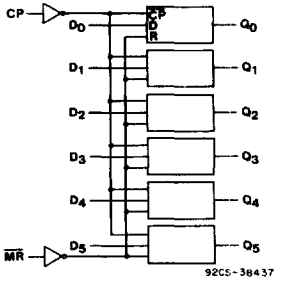
CD54/74HC174
CD54/74HCT174

File Number **1608**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Hex D-Type Flip-Flop with Reset
Positive-Edge Triggered

Type Features:

- *Buffered Positive-Edge-Triggered Clock*
- *Asynchronous Common Reset*

The RCA-CD54/74HC174 and CD54/74HCT174 are edge triggered flip-flops which utilize silicon gate CMOS circuitry to implement D-type flip-flops. They possess low power and speeds comparable to low power Schottky TTL circuits. The devices contain 6 master-slave flip-flops with a common clock and common reset. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The $\overline{MR}$ input, when low, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The CD54/74HCT174 is functionally as well as pin compatible to the 54LS174/74LS174.

The CD54HC174 and CD54HCT174 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC174 and CD74HCT174 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC};
  @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

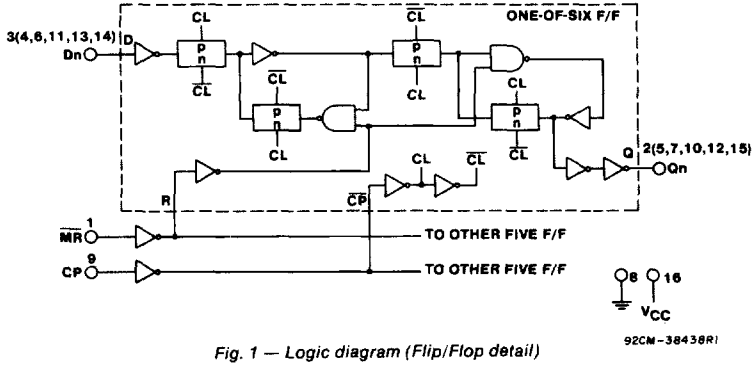


Fig. 1 — Logic diagram (Flip/Flop detail)

CD54/74HC174
CD54/74HCT174

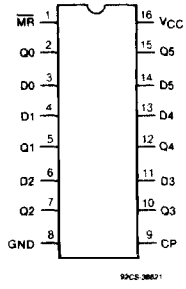
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC} +0.5$ V) ..... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to -125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300°C

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	**CLOCK CP**	**DATA Dn**	**Qn**
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q_O

H = High Level (Steady State)
L = Low Level (Steady State)
X = *Irrelevant*
↗ = Transition from Low to High Level
Q_O = Level Before the Indicated Steady-State Input Conditions were established



TOP VIEW

TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC174
CD54/74HCT174

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC174/CD54HC174										CD74HCT174/CD54HCT174									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage CMOS Loads V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage TTL Loads V_{OH}	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage CMOS Loads V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage TTL Loads V_{OL}	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{CP}$	0.80
$\overline{MR}$	0.55
D	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Pulse	2	80	—	—	—	100	—	—	—	120	—	—	—	
Width t_w	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 3	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{MR}$ Pulse Width t_w	4.5	16	—	25	—	20	—	31	—	24	—	38	—	ns
Fig. 4	6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time Data	2	60	—	—	—	75	—	—	—	90	—	—	—	
to Clock t_{SU}	4.5	12	—	16	—	15	—	20	—	18	—	24	—	ns
Fig. 5	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data	2	5	—	—	—	5	—	—	—	5	—	—	—	
to Clock t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 5	6	5	—	—	—	5	—	—	—	5	—	—	—	
Removal Time	2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{MR}$ to Clock t_{rem}	4.5	5	—	12	—	5	—	15	—	5	—	18	—	ns
Fig. 4	6	5	—	—	—	5	—	—	—	5	—	—	—	
	2	6	—	—	—	5	—	—	—	4	—	—	—	
Clock Frequency f_{max}	4.5	30	—	25	—	24	—	20	—	20	—	17	—	MHz
	6	35	—	—	—	28	—	—	—	24	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
Clock to Q t_{PHL}	4.5	—	33	—	40	—	41	—	50	—	50	—	60	ns
Fig. 3	6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{MR}$ to Q t_{PHL}	4.5	—	30	—	44	—	38	—	55	—	45	—	66	ns
Fig. 4	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Fig. 6	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

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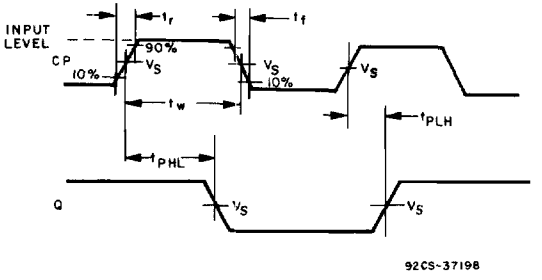
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

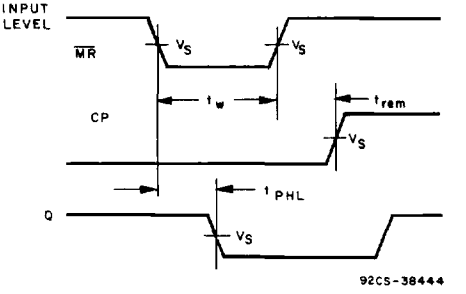
CHARACTERISTIC		C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay — Clock to Q Fig.3	t_{PLH} / t_{PHL}	15	13	17	ns
Propagation Delay — MR to Q Fig. 4	t_{PLH} / t_{PHL}	15	12	18	ns
Power Dissipation Capacitance*	C_{PD}	—	38	44	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage



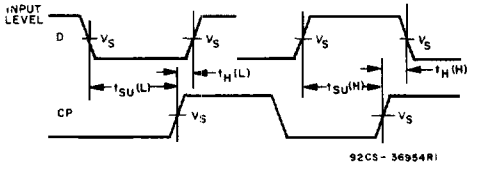
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 — Propagation delay times and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 — Prerequisite and propagation delay times for master reset.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 — Pre

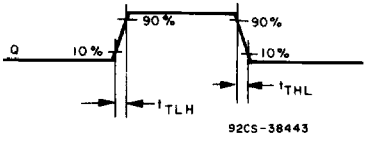


Fig. 6 — Transition times.