Aerospace Electronics

Advance Information

512K x 8 STATIC RAM—SOI

HX6408

FEATURES

RADIATION

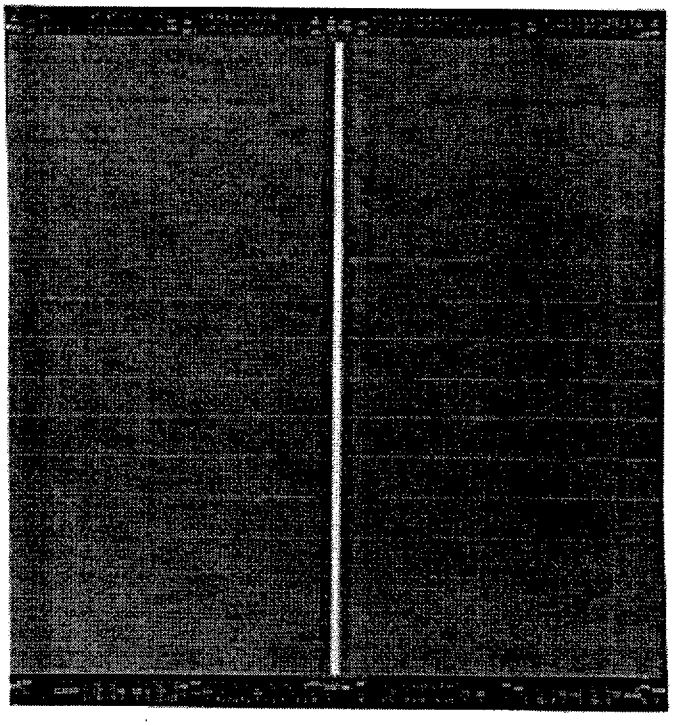
- Fabricated with RICMOS™ V Silicon On Insulator (SOI) 0.35 µm Process (L_{eff} = 0.28 µm)
- Total Dose Hardness ≥$5x10^5$ rad(SiO_2)
- Neutron Hardness ≥$1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness ≥$1x10^{10}$ rad(Si)/s (3.3 V)
- Dose Rate Survivability ≥$1x10^{12}$ rad(Si)/s
- Soft Error Rate Upsets/bit-day ≤$1x10^{-10}$ (3.3 V)
- No Latchup

OTHER

- Read/Write Cycle Times
  ≤ 20 ns, (3.3 V), 0 to 80°C
  ≤ 25 ns, (3.3 V), -55 to 125°C
- Typical Operating Power
  ≤9.5 mW/MHz (3.3 V)
- Asynchronous/Synchronous Operation (Bond Programmable)
- CMOS Compatible I/O
- Single Power Supply, 3.3 V ± 0.3 V
- Operating Range is -55°C to +125°C
- Package Options:
  – 36-Lead Flat Pack

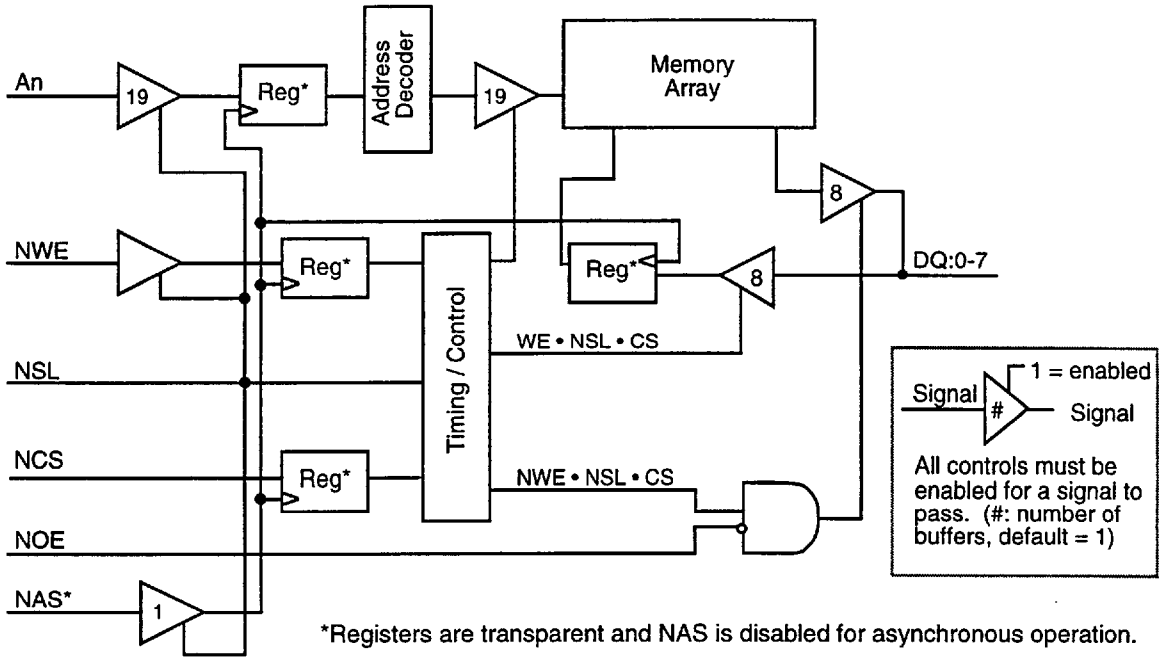
GENERAL DESCRIPTION

The 512K x 8 Radiation Tolerant Static RAM is a high performance 524,288 word x 8-bit static random access memory with optional industry-standard functionality. It is fabricated with Honeywell's radiation hardened technology, and is designed for use in low voltage systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 3.3 V ± 0.3V power supply. Power consumption is typically less than 9.5 mW/MHz in operation, and less than 6 mW when de-selected.



Honeywell's enhanced SOI RICMOS™ V (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. The RICMOS™ V low power process is a SIMOX CMOS technology with a 100 Å gate oxide and a minimum drawn feature size of 0.35 µm. Additional features include tungsten via and contact plugs, Honeywell's proprietary SHARP planarization process and a lightly doped drain (LDD) structure for improved short channel reliability. A seven transistor (7T) memory cell is used for superior single event upset hardening, while three layer metal power bussing and the low collection volume SIMOX substrate provide improved dose rate hardening.

FUNCTIONAL DIAGRAM



*Registers are transparent and NAS is disabled for asynchronous operation.

SIGNAL DEFINITIONS

A: 0-18 Address input pins which select a particular eight-bit word within the memory array.

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS Negative chip select, when at a low level allows normal read or write operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state. If this signal is not used it must be connected to VSS. This signal is clocked with NRS in synchronous operation.

NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level NWE allows normal read operation.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and NSL. If this signal is not used it must be connected to VSS. This signal is asynchronous, even in synchronous operation.

NSL Not sleep, when at a high level allows normal operation. When at a low level NSL forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS and NOE input buffers. If this signal is not used it must be connected to VDD. This signal is asynchronous, even in synchronous operation.

NAS Not address strobe, (synchronous option only) the falling edge of this signal strobes in new addresses and data.

TRUTH TABLE

NCS	NSL	NWE	NOE	NAS	Mode	DQ
L	H	H	L	X	Read	Data Out
L	H	L	X	X	Write	Data In
H	X	X	X	X	Deselected	High Z
X	L	X	X	X	Sleep	High Z

X: VI=VIH or VIL,
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 3.6 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 KeV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that stiffening capacitance be placed near the package VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through or valid stored data requirements, typical circuit board mounted de-coupling capacitors are recommended.

The SRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The SRAM is capable of meeting the specified Soft Error Rate (SER), under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	≥$5x10^5$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset	≥$1x10^{10}$	rad(Si)/s	Pulse width ≤50 ns VDD>3.6V, T_A=25°C
Transient Dose Rate Survivability	≥$1x10^{12}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=3.6 V, T_A=25°C
Soft Error Rate	<$1x10^{-10}$	upsets/bit-day	T_A=85°C, Adams 90% worst case environment
Neutron Fluence	≥$1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=3.0 V to 3.6 V, TA=-55°C to 125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Supply Voltage Range (2)		-0.5	4.6	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature (5 Seconds)			270	°C
PD	Maximum Power Dissipation (3)			2	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage		2000		V
ΘJC	Thermal Resistance (Jct-to-Case)	36 Pin FP		2	°C/W
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	3.0	3.3	3.6	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical (1)	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance			7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance			9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

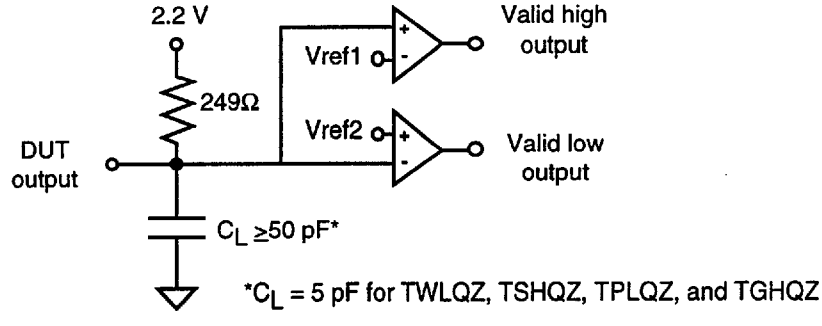
Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
VDR	Data Retention Voltage		2.25		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current			1	mA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.
(2) Worst case operating conditions: TA= -55°C to +125°C, post total dose at 25°C.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Worst Case (1)		Units	Test Conditions
		Min	Max		
IDDSB	Static Supply Current		5	mA	VDD=max, Iout=0mA, Inputs Stable
IDDSL	Static Supply Current with NSL Low		5	mA	VDD=max, Iout=0mA, f=fmax
IDDOPW	Dynamic Supply Current, Selected (Write)		3	mA/MHz	VDD=max, Iout-0mA, f=1MHz NSL=VIH, NCS=VIL (1)
IDDOPR	Dynamic Supply Current, Selected (Read)		3	mA/MHz	VDD=max, Iout-0mA, f=1MHz) NSL=VIH, NCS=VIL (1)
IDDOP	Dynamic Supply Current, Deselected		1	mA	VDD=max, Iout-0mA, f=1MHz NSL=NCS=VIH (2)
II	Input Leakage Current	-5	5	µA	Vss≤VI≤VDD
IOZ	Output Leakage Current	-10	10	µA	Vss≤VIO≤VDD Output = high Z
VIL	Low-Level Input Voltage		0.3xVDD	V	VDD=3.0 V
VIH	High-Level Input Voltage	0.7xVDD		V	VDD=3.6 V
VOL	Low-Level Output Voltage		0.4	V	VDD=3.0 V, IOL = 8mA
VOH	High-Level Output Voltage	2.4		V	VDD=3.0V, IOH = 4mA

(1) Worst case operating conditions: VDD=3.0 V to 3.6 V, -55°C to +125°C, post total dose at 25°C.
(2) All inputs switching. DC average current.

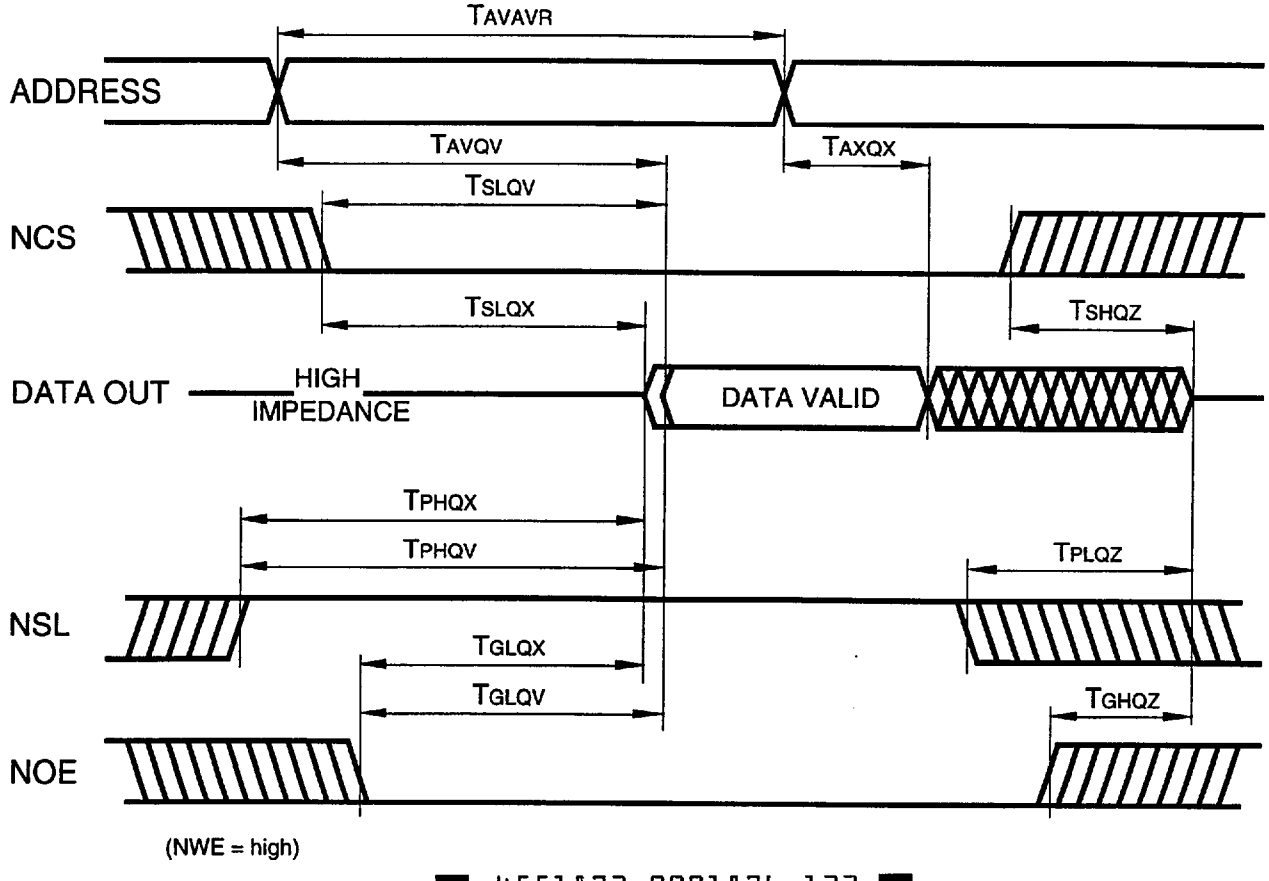


Tester Equivalent Load Circuit

ASYNCHRONOUS READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVR	Address Read Cycle Time		25		ns
TAVQV	Address Access Time			25	ns
TAXQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			25	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			10	ns
TPHQV	Sleep Enable Access Time			25	ns
TPHQX	Sleep Enable Output Enable Time		5		ns
TPLQZ	Sleep Enable Output Disable Time			10	ns
TGLQV	Output Enable Access Time			9	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			9	ns

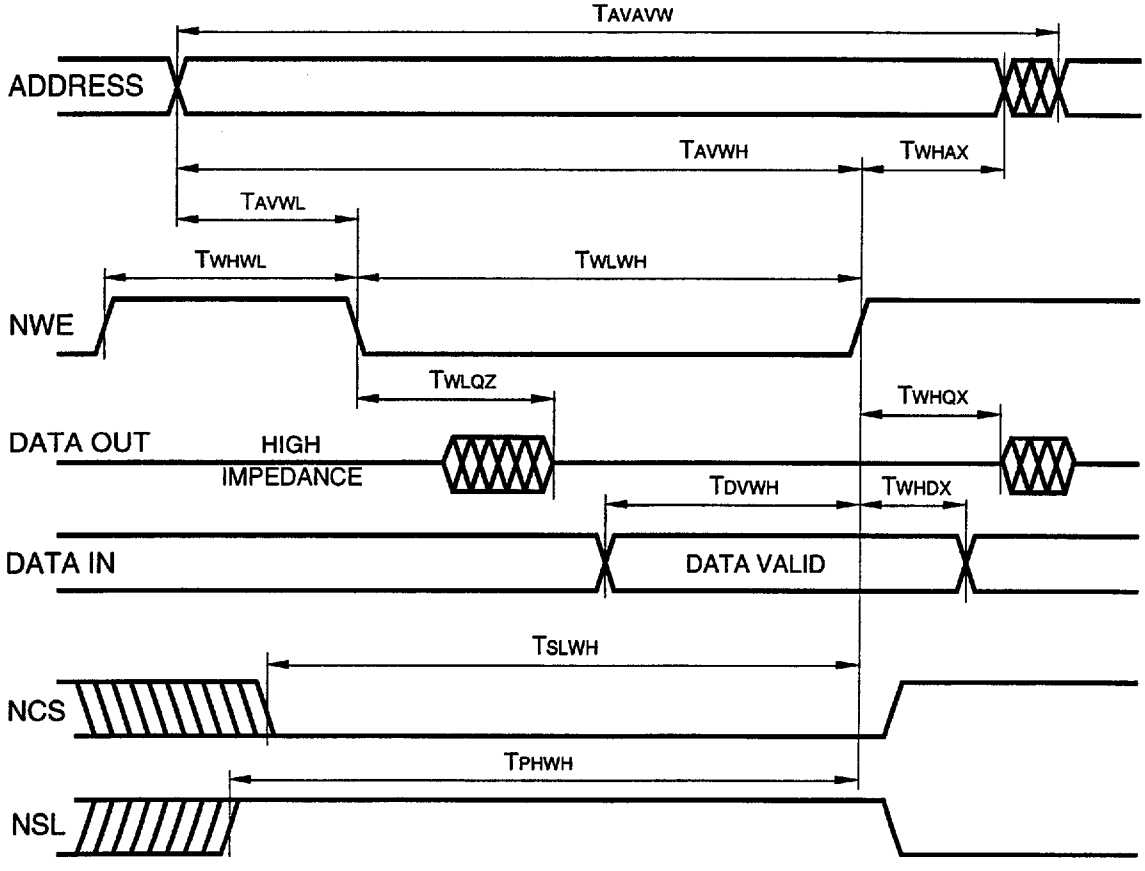
(1) Test conditions: input switching levels,VIL/VIH=0V/3V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading C_L=5 pF for TSHQZ, TPLQZ TGHQZ. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=3.3 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=3.0 V to 3.6 V, TA= -55°C to 125°C, post total dose at 25°C.



ASYNCHRONOUS WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Max	Units
TAVAVW	Write Cycle Time (4)		25		ns
TWLWH	Write Enable Write Pulse Width		20		ns
TSLWH	Chip Select to End of Write Time		20		ns
TDVWH	Data Valid to End of Write Time		15		ns
TAVWH	Address Valid to End of Write Time		20		ns
TWHDX	Data Hold Time after End of Write Time		0		ns
TAVWL	Address Valid Setup to Start of Write Time		0		ns
TWHAX	Address Valid Hold after End of Write Time		0		ns
TWLQZ	Write Enable to Output Disable Time		0	9	ns
TWHQX	Write Disable to Output Enable Time		5		ns
TWHWL	Write Disable to Write Enable Pulse Width (5)		5		ns
TPHWH	Sleep Enable to End of Write Time		20		ns

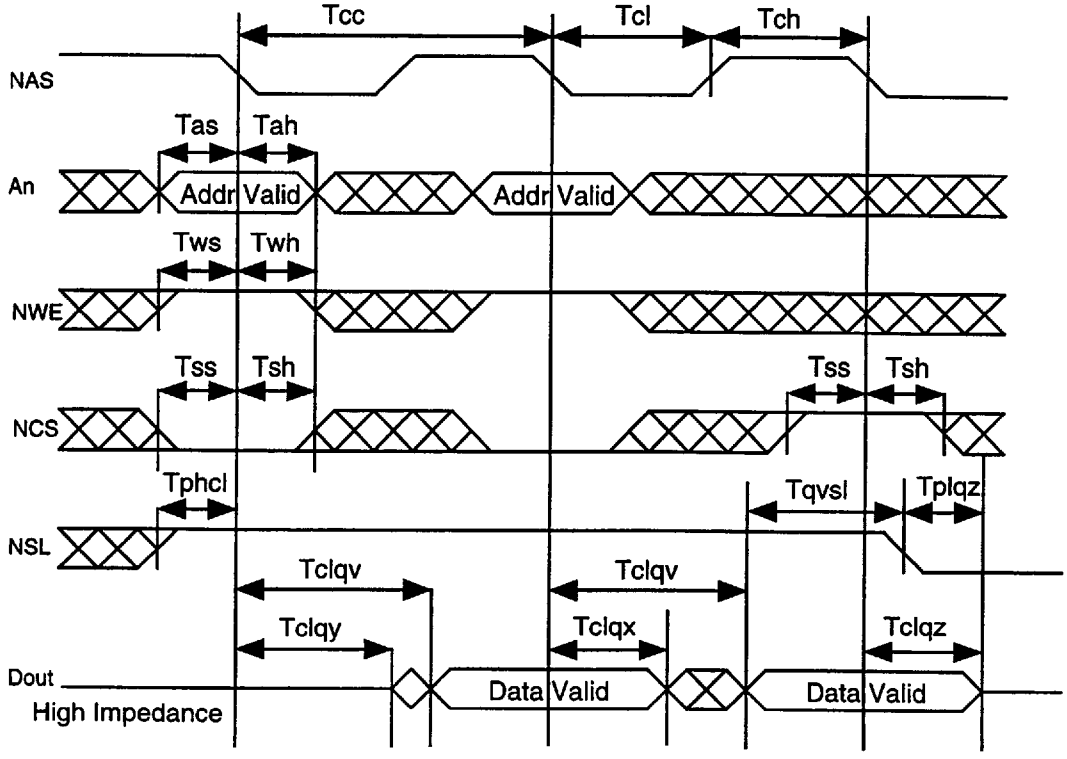
(1) Test conditions: input switching levels, VIL/VIH=0V/3V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading ≥50 pF, or equivalent capacitive load of 5 pF for TWLQZ.
(2) Typical operating conditions: VDD=3.3 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=3.0 V to 3.6 V, -55 to 125°C, post total dose at 25°C.
(4) TAVAVW = TWLWH + TWHWL
(5) Guaranteed but not tested.



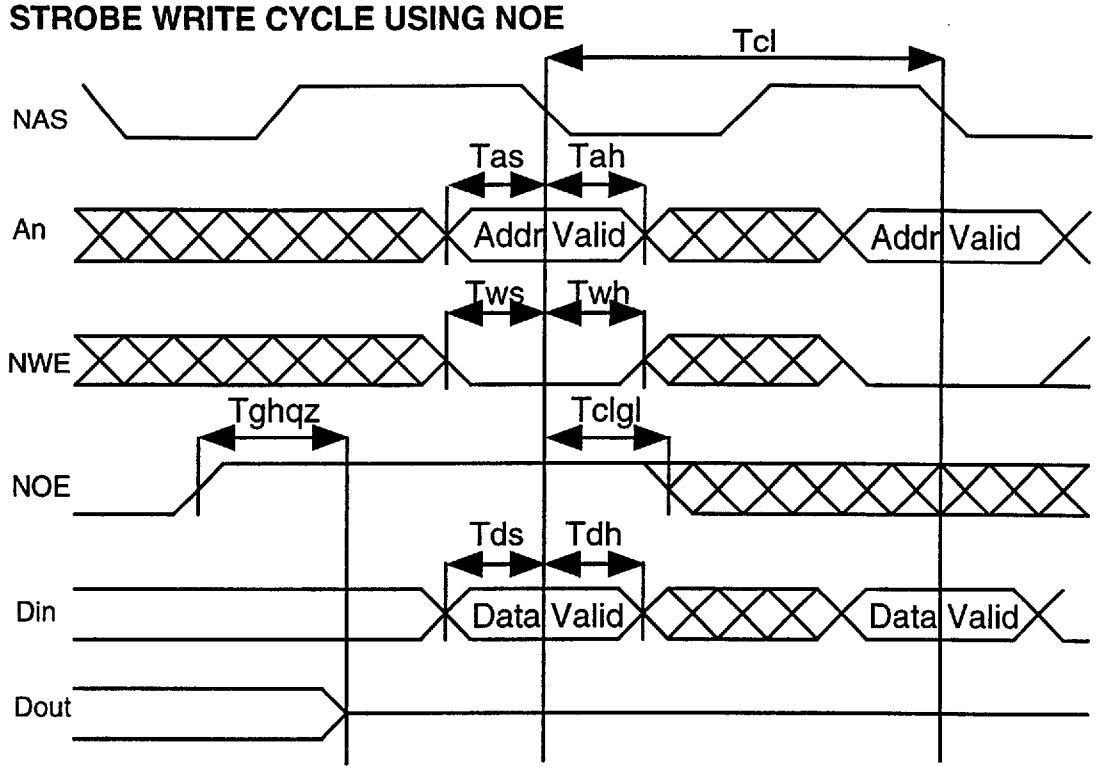
SYNCHRONOUS AC TIMIMG CHARACTERISTICS

Symbol	Parameter	Worst Case		Units
Tcc	Clock Cycle Time	25		ns
Tcl	Clock Low	10		ns
Tch	Clock High	10		ns
Tas	Address Setup Time	3		ns
Tah	Address Hold Time	5		ns
Tds	Data Setup Time	3		ns
Tdh	Data Hold Time	7		ns
Tws	Write Setup Time	3		ns
Twh	Write Hold Time	5		ns
Tss	Not Chip Select Setup Time	3		ns
Tsh	Not Chip Select Hold Time	5		ns
Tphcl	Sleep Enable Setup Time	5		ns
Tqvsl	Data Valid To Sleep Enable Time	0		ns
Tplqz	Sleep Enable Output Disable Time	2	10	ns
Tclqv	Address Strobe Access Time		25	ns
Tclqx	Address Strobe to Output Invalid Time	2		ns
Tclqy	Address Strobe to Output Enable Time	5		ns
Tclqz	Address Strobe to Output Disable Time		10	ns
Tghqz	Output Enable Output Disable Time		9	ns
Tclgl	Output Disable Hold Time	5		ns

ADDRESS STROBE READ CYCLE



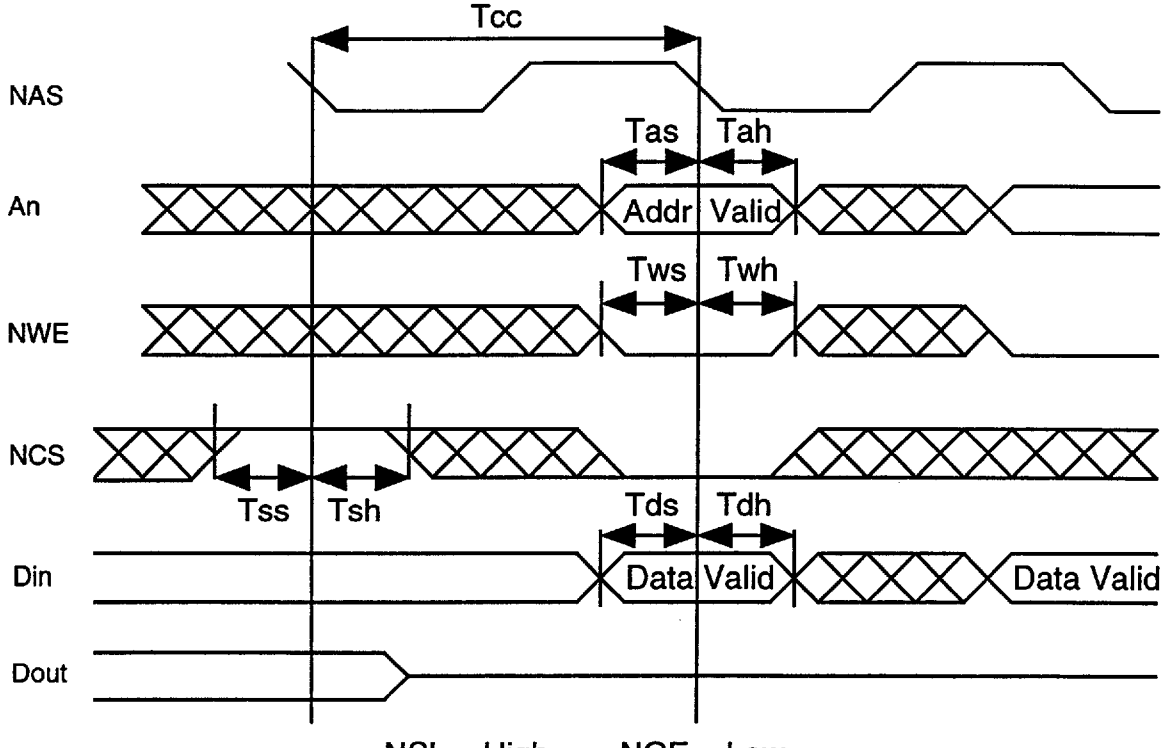
ADDRESS STROBE WRITE CYCLE USING NOE



NSL = High NCS = Low

NSL timing shown in address strobe read cycle diagram

ADDRESS STROBE WRITE CYCLE USING NCS



NSL = High NOE = Low

NSL timing shown in address strobe read cycle diagram

DYNAMIC ELECTRICAL CHARACTERISTICS

Asynchronous Operation

The RAM in asynchronous in operation, allows the read cycle to be controlled by address, chip select (NCS), or not sleep (NSL) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and not sleep (NSL) and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with NSL held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and NSL must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and NSL must be valid prior to or coincident with the enabling NCS edge transition. Address or NSL edge transitions can occur later than the specified setup times to NCS; however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with NSL, all addresses and NCS must be valid prior to or coincident with the enabling NSL edge transition. Address or NCS edge transitions can occur later than the specified setup times to NSL; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when NSL is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TPLQZ time following a disabling NSL edge transition.

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or not sleep (NSL) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and NSL must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or NSL held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and NSL. All three modes of control are similar, except the NCS and NSL controlled modes actually disable the RAM during the write recovery pulse. NSL fully disables the RAM decode logic and input buffers for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity; however, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and NSL must be held high for at least TWLWH/TSLSH/TPHPH time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TPLPL time. Address inputs must be valid at least TAVWL/TAVSL/TAVPH time before the enabling NWE/NCS/NSL edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVPL, and an address valid to end of write time of TAVWH/TAVSH/TAVPL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/NSL edge transition must be a minimum of TWHAX/TSHAX/TPLPX time and TWHDX/TSHDX/TPLDX time, respectively. The minimum write cycle time is TAVAV.

Snchronous Operation

Synchronous read cycle operation is initiated by the falling edge of NAS when NSLP and NWE are high, and NCS and NOE are low. If NOE is high, an internal read will occur, but the RAM outputs will be tristated. Addresses must be set up Tas time before and held for Tah time after the falling edge of NAS to guarantee a valid read address. Valid data will appear at the outputs TCLQV time after the falling edge of NAS.

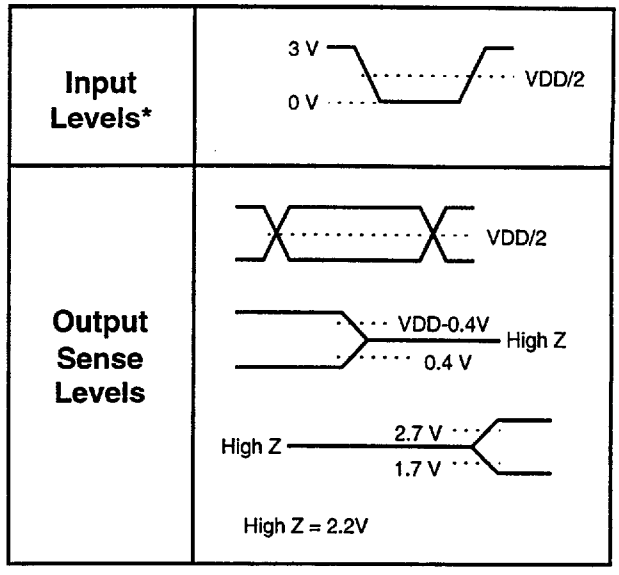
The NOE and NSLP pins are asynchronous in operation, where NOE can be switched at any time to disable the outputs or to prepare for a write cycle. NSLP will disable all input latches and the NAS signal, reducing power to standby levels. The NSLP pin should only be switched low in read mode (NWE high) to avoid an unwanted write. If a write cycle is required when exiting sleep mode, NSLP should be switched high before or coincident with NWE switching low.

DYNAMIC ELECTRICAL CHARACTERISTICS (Con't)

Two methods are available for enabling write mode after a read: 1.) NOE can be switched high once valid data is retrieved from the read cycle, after which data can be forced onto the data bus TGHQz time after the falling edge of NOE. NWE can then be switched Tws time before the falling edge of NAS. Data must be set up Tds time before the falling edge of NAS to perform a valid write. 2.) NCS can be used to disable the chip, forcing the outputs into a Hi-Z state. Data can then be forced onto the data bus Tclqz time after the falling edge of NAS. NWE should then be switched Tws time before the next falling edge of NAS to perform a valid write.

Sequential write cycles can be performed by holding NWE low and switching NAS. All addresses must be setup Tas time before the falling edge of NAS.

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times <1 ns/V

QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete "Total Quality Assurance System," a computer data base process performance tracking system and a radiation-hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

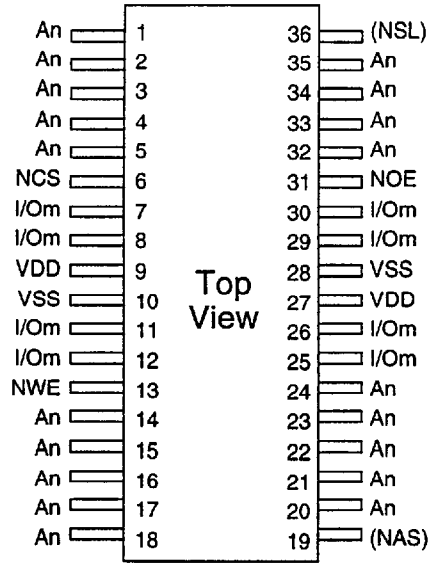
Honeywell offers several levels of device screening to meet your system needs. "Engineering Devices" are available with limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Microcircuit Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements for space and defense systems and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer's requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

36-LEAD FLAT PACK PINOUT



PACKAGING

The 512K x 8 is offered in a commercially compatible 36-lead flat pack. This package is constructed of multilayer ceramic (Al_2O_3) and contains internal power and ground planes. Parentheses denote pin options. These pins are available as NC to conform to commercial standards.

ORDERING INFORMATION (1)

H — **SOURCE**
H=HONEYWELL

X — **PROCESS**
X=Low Power SOI

6408 — **PART NUMBER**

X — **PACKAGE DESIGNATION**
X=36-Lead FP
K=Known Good Die
– =Bare Die (No Package)

S — **SCREEN LEVEL**
V=QML Class V
Q=QML Class Q
S=Class S
B=Class B
E=Engineering Device (2)

H — **TOTAL DOSE HARDNESS**
R=1x10^5 rad(SiO_2)
F=3x10^5 rad(SiO_2)
G=5x10^5 rad(SiO_2)
N=No Level Guaranteed (2)

A — **OPERATION (3)**
A=Asynchronous
S=Synchronous

N — **MODE (4)**
N=Non-Sleep Mode
M=Sleep Mode

(1) Orders may be faxed to 612-954-2051. Please contact our Customer Service Representative at 612-954-2888 for further information.
(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, IDDSB = 10mA, no radiation guaranteed.
(3) With the Asynchronous operation option, pin 19 is a no-connect (NC), and is not wire bonded to the chip. With synchronous operation, pin 19 has the NAS function.
(4) With the Non-Sleep mode option, pin 36 is a no-connect (NC), and is not wire bonded to the chip. With the Sleep Mode option, pin 36 has NSL function.

Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

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