Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74S112

Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flop with Preset, Clear, and Complementary Outputs

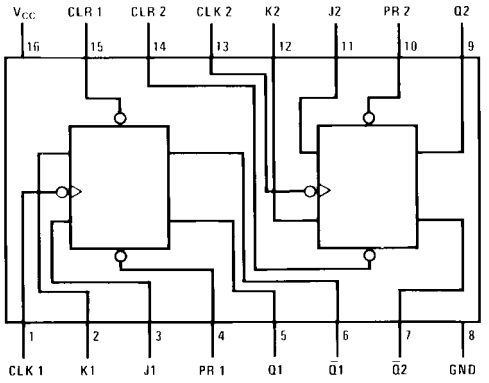
General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is HIGH or LOW without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM74S112	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (HIGH) level.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−1	mA
I_{OL}	LOW Level Output Current				20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock HIGH	6			ns
		Clock LOW	6.5			
		Clear LOW	8			
		Preset LOW	8			
t_W	Pulse Width (Note 3)	Clock HIGH	8			ns
		Clock LOW	8			
		Clear LOW	10			
		Preset LOW	10			
t_{SU}	Setup Time (Note 4)(Note 5)		7↓			ns
t_H	Input Hold Time (Note 4)(Note 5)		0↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Note 5: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = – 18 mA				–1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			50	µA
			Clear			100	
			Preset			100	
			Clock			100	
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.5V (Note 7)	J, K			–1.6	mA
			Clear			–7	
			Preset			–7	
			Clock			–4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 8)		–40		–100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 9)			30	50	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Clear is tested with preset HIGH and preset is tested with clear HIGH.

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second.

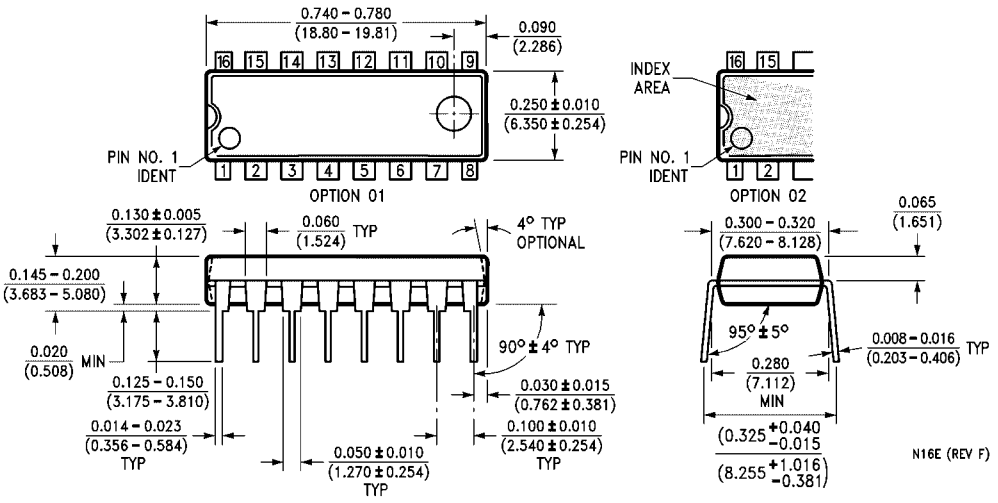
Note 9: With all outputs OPEN, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		7		12	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		7		12	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		7		12	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

[Information as of 1-Aug-2000]

DM74S112

Dual Negative-Edge-Triggered J-K Flip-Flop with Preset Clear and Complementary Ou

Generic P/N 74S112

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Features

Datasheet

Receive datasheet via E-mail or download now ; use Adobe Acrobat to view...

DM74S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs (43 Kbytes; 29-JUL-00)

Availability, Models, Samples & Pricing

Part Number	Grade	Package		Status	Models		Budgetary Pricing		Std Pack Size	Package Marking
		Type	# pins		SPICE	IBIS	Quantity	$US ea		
DM74S112N	Comm	MDIP	16	Full Production	N/A	N/A	1-24 25-99 100-1000	$0.60 $0.45 $0.36	N/A	$Y&Z&4& DM74S11
DM74S112CW	Comm	wafer		Preliminary	N/A	N/A		N/A	N/A	

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