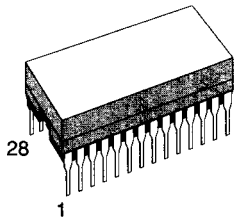
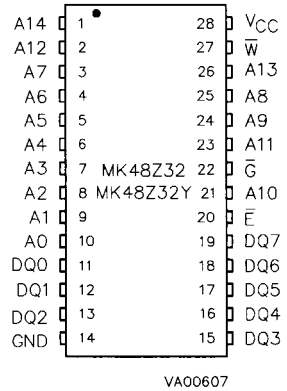
CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- MINIMUM BATTERY BACK-UP OF 10 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE:
  - MK48Z32 - $4.50V \leq V_{PFD} \leq 4.75V$
  - MK48Z32Y - $4.20V \leq V_{PFD} \leq 4.50V$



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



DESCRIPTION

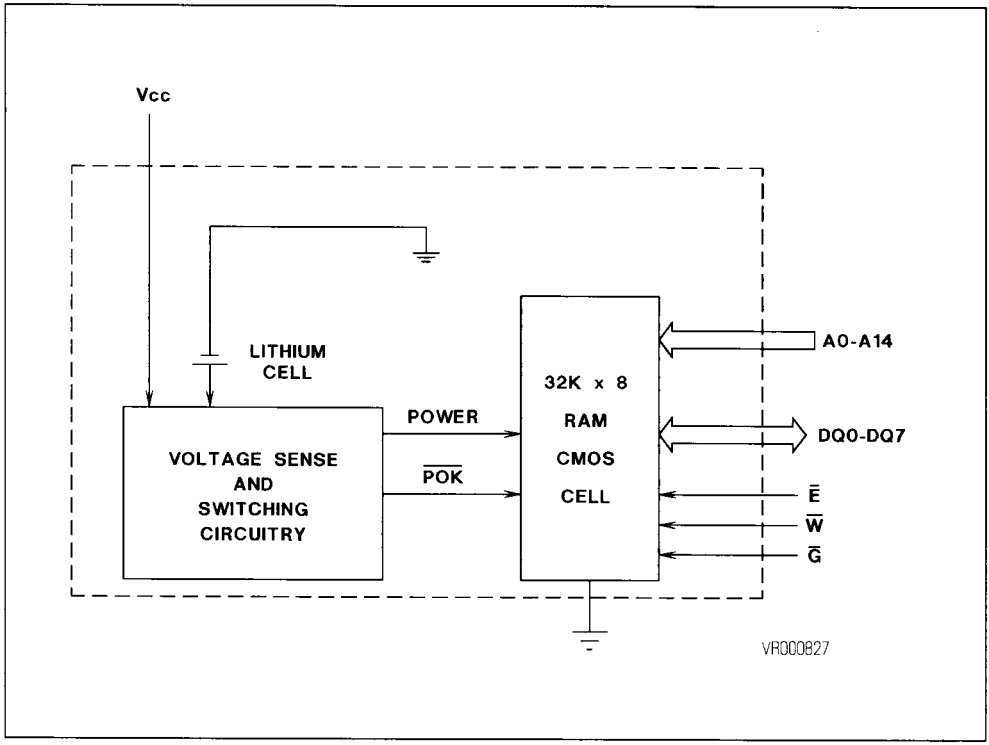
The MK48Z32/32Y ZEROPOWER™ RAM combines an 32K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z32/32Y is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into may EPROM and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z32/32Y has its own Power-fail Detect Circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

PIN NAMES

A0-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
V_{CC} , GND	5 Volts, Ground

Figure 2. Block Diagram



TRUTH TABLE

Vcc	E	G	W	Mode	DQ	Power
< Vcc (max) > Vcc(min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	50	mA
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 70	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z32)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z32Y)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current (70ns)		85	mA	3
I_{CC1}	Average V_{CC} Power Supply Current (120ns)		70	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current (V_{CC} max $\ge \overline{E} \ge$ V_{CC} –0.3V)		2	mA	
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	4
I_{OL}	Output Leakage Current	-2	+2	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0mA)		0.4	V	1

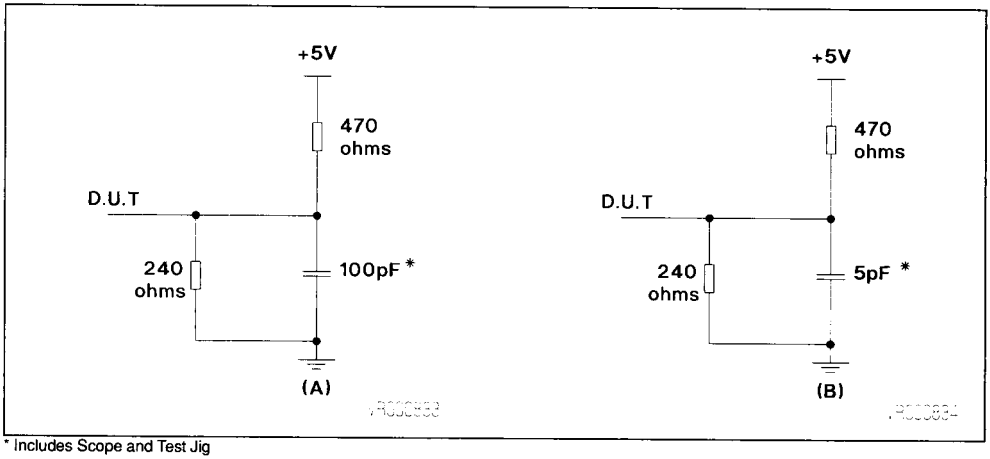
Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $V_{CC} \ge V_I \ge$ GND and outputs deselected.

AC TEST CONDITIONS

Input Levels	0.0V to 3.0V
Transition Times	1.5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS



* Includes Scope and Test Jig

CAPACITANCE

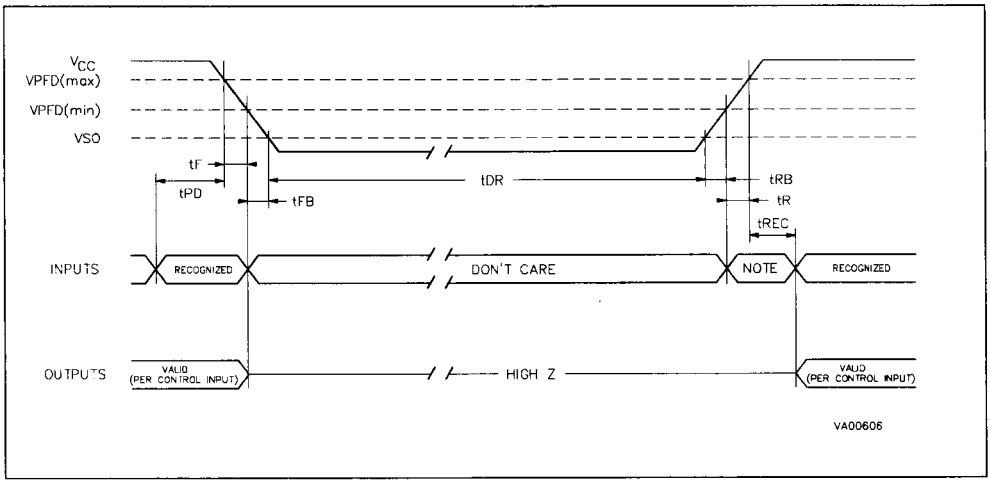
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance On DQ Pins	10.0	pF	1, 2

Notes :

1. Effective capacitance calculated from the equation $C = I \Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0 V.
2. Measured with outputs deselected.

Figure 3. Power Up/Down Waveform



NOTE : Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD}(min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z32)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z32Y)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		2.5		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	

Notes : 1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passesV_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

READ MODE

The MK48Z32/32Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied. If Chip Enable or Output Enable access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

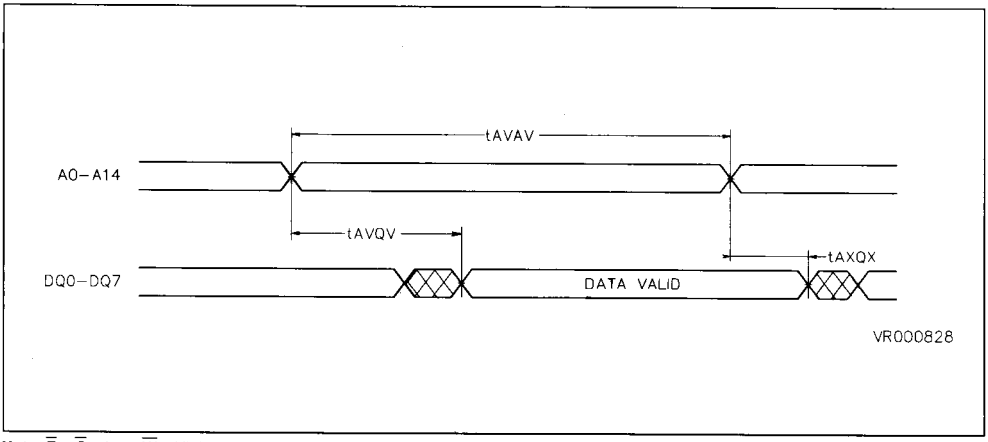
($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq$ V_{CC} max)

Symbol	Parameter	MK48Z32/32Y-70		MK48Z32/32Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AVQV}	Address Access Time		70		120	ns	1
t_{ELQV}	Chip Enable Access Time		70		120	ns	1
t_{GLQV}	Output Enable Access Time		35		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	10		10		ns	2
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	2
t_{EHQZ}	Chip Disable ($\overline{E}$) High to Q High-Z	0	25	0	35	ns	2
t_{GHQZ}	Output Disable ($\overline{G}$) High to Q High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes :

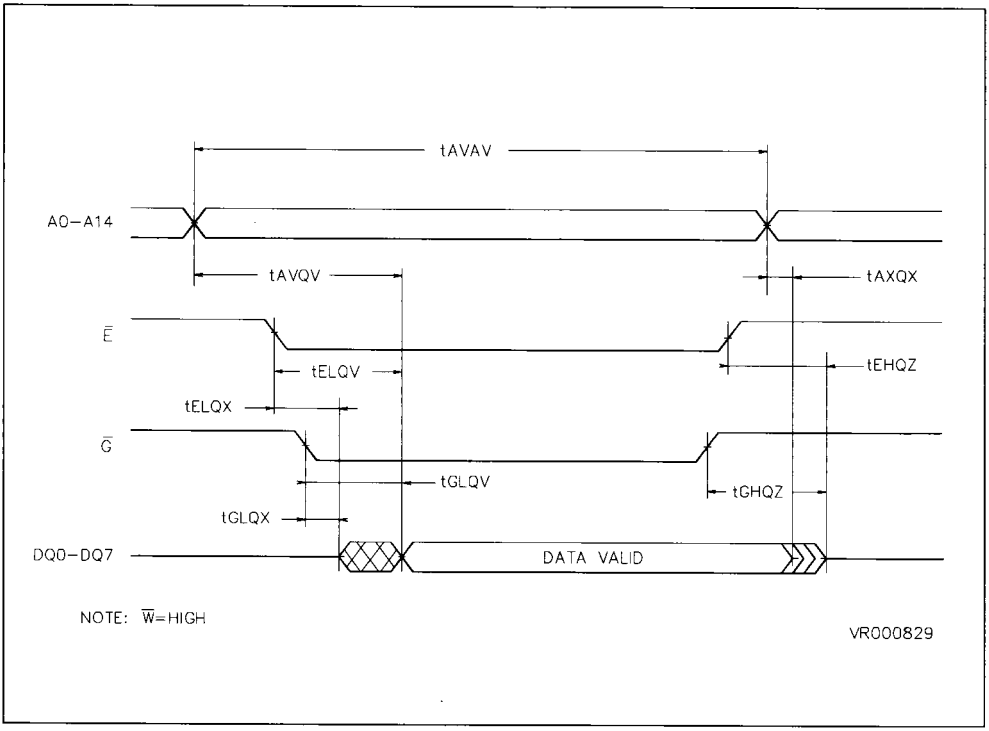
1. Measured with load as shown in Figure A page 4.
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)



Note: $\overline{E}$ = $\overline{G}$ = Low, $\overline{W}$ = High

Figure 5. Read Timing n° 2



WRITE MODE

The MK48Z32/32Y is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of Write Enable or Chip Enable. A write is terminated by the earlier rising edge of Write Enable or Chip Enable. The addresses must be held valid throughout the cycle. Chip Enable or Write Enable must return high or for minimum of t_{WHAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because Output Enable is a Don't Care in the Write Mode and a low on Write Enable will return the outputs to High-Z, Output Enable can be tied low and two-wire RAM control can be implemented. A low on Write Enable will disable the outputs t_{WLQZ} after Write Enable falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq$ V_{CC} max)

Symbol	Parameter	MK48Z32/32Y-70		MK48Z32/32Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-Up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	60		85		ns	
t_{WLWH}	Write Pulse Width	50		65		ns	
t_{WHAX}	Address Hold after End of Write	0		0		ns	
t_{ELEH}	Chip Enable Active to End of Write	55		85		ns	
t_{EHAX}	Address Hold Time from Chip Enable	0		0		ns	
t_{DVWH}	Data Valid to End of Write	30		40		ns	
t_{WHDX}	Data Hold Time	0		0		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	5		5		ns	1
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	25	0	35	ns	1

Notes :

1. Measured with load as shown in Figure B page 4.

Figure 6. Write Control Write Cycle Timing

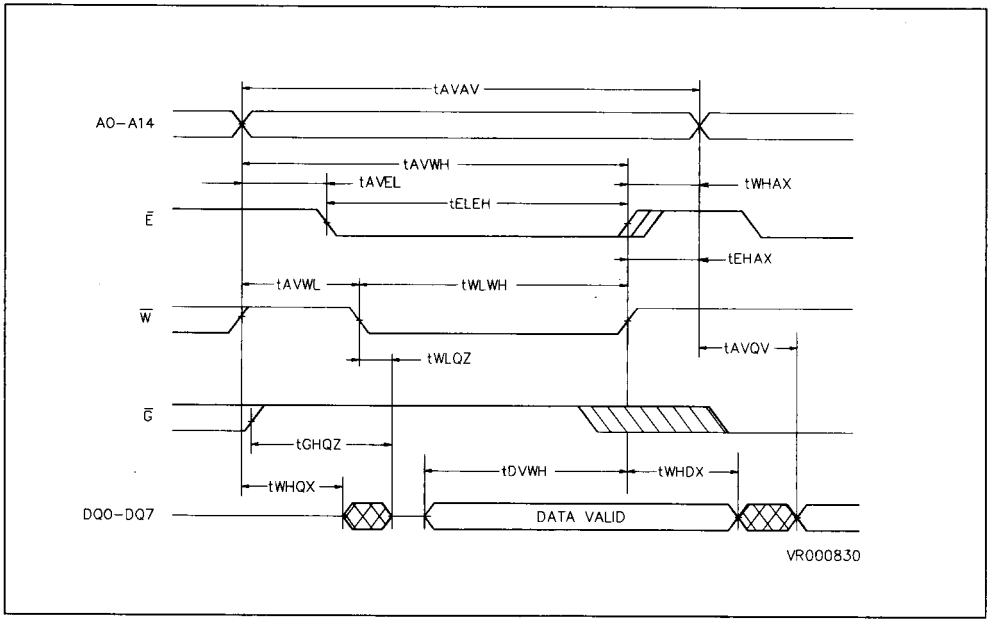
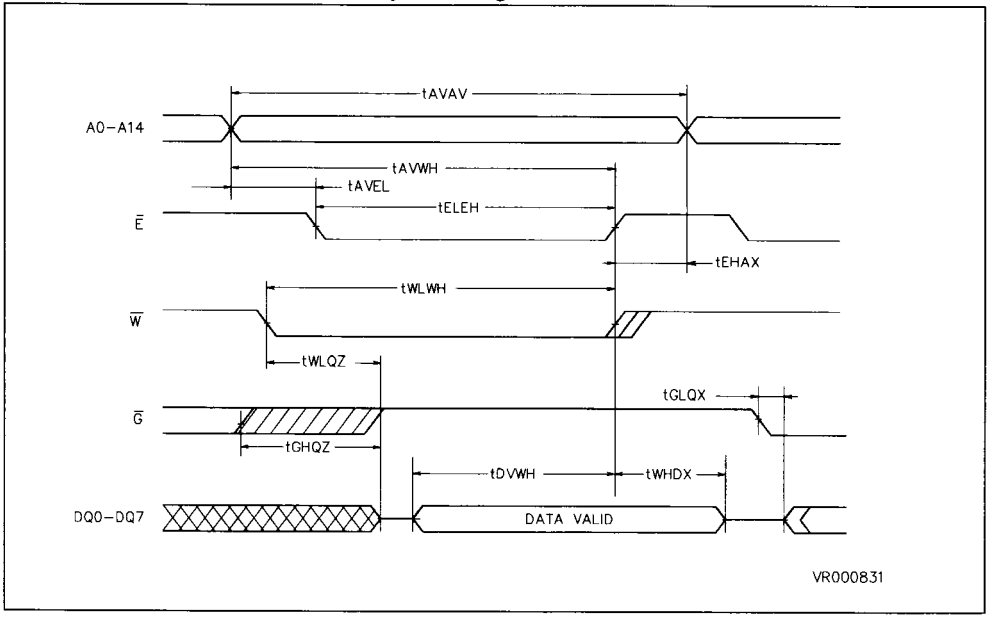


Figure 7. Chip Enable Control Write Cycle Timing



DATA RETENTION MODE

With V_{CC} applied, the MK48Z32/32Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect , write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window.

A mid-cycle power fail may corrupt data at the currently addressed location, but does not jeopar-dize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, providing the V_{CC} fall time is not less than t_F.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z32/32Y is expected to ultimately come to an end for one of two reasons: either because the effects of aging render the cell useless before it can actually be discharged; or because it has been discharged while providing current to an external load.

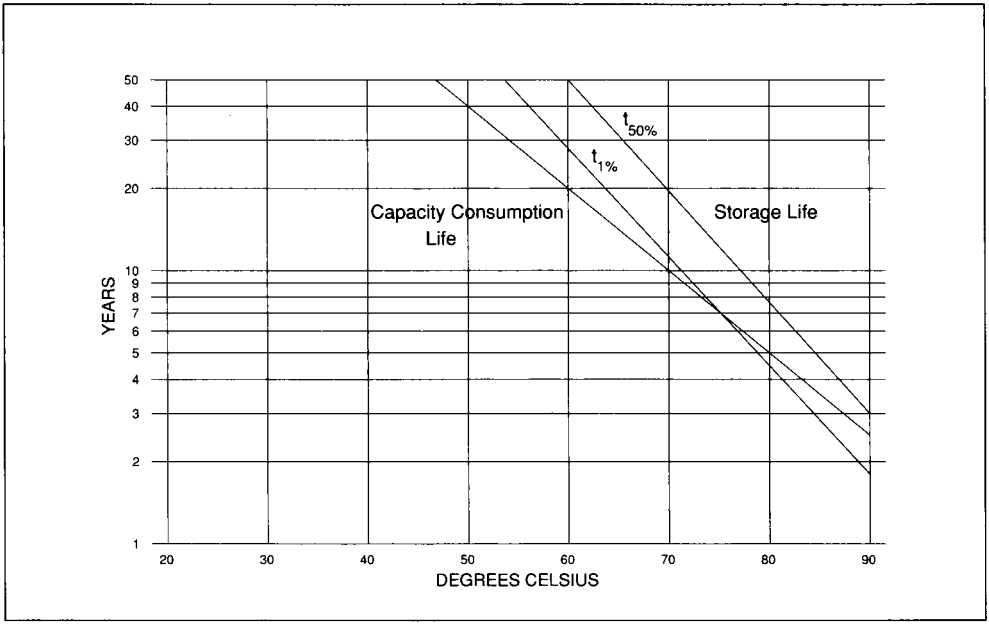
These two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous battery end-of-life mechanisms.

With V_{CC} on, the battery is disconnected from the RAM and Storage Life becomes the determining factor in battery longevity.

With V_{CC} off, the MK48Z32/32Y initiates back-up mode by switching power from the V_{CC} input to the internal battery. In the back-up mode, leakage current drawn by the RAM represents the only load on the battery. The load condition consumes the cell's capacity and is therefore referred to as Capacity Consumption. Capacity Consumption is the primary battery end-of-life mechanism while the MK48Z32/32Y is in the battery back-up mode.

Battery life is defined as beginning on the date of manufacture. Each MK48Z32/32Y is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9 -tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Figure 8. Predicted Battery Storage Life Versus Temperature



Storage Life

Figure 8 illustrates how temperature affects Storage Life of the MK48Z32/32Y battery.

Two End-of- Life curves related to Storage Life are presented in the Figure 8. They are labeled "Average" ($t_{1\%}$), and "Average" ($t_{50\%}$). These terms define the probability that a given number of failures will accumulate by a particular point in time. If, for example, a battery's expected life at 70°C is an issue, Figure 8 indicates that an MK48Z32/32Y has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year time. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years and 50% of them within 20 years.

Capacity Consumption Life

Figure 8 also shows how Capacity Consumption varies with temperature.

The MK48Z32/32Y battery cell has a minimum rated capacity of 39 mAh. The RAM, in battery-backed mode, places a nominal load of 445nA at 70 °C. At this rate, the MK48Z32/32Y will consume the capacity of the battery cell in 87,600 hours or about 10 years.

As long as ambient temperature is held reasonably constant, expected Capacity Consumption Life can be estimated directly from the curve in Figure 8. As Vcc Duty Cycle increases, though, so does Capacity Consumption Life. At 70 °C and 20% power on Duty Cycle, the Capacity Consumption Life is:

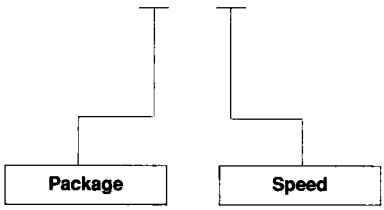
$$10/(1-0.20) = 12.5 \text{ years.}$$

Estimating Back-up System Life

Either Storage or Capacity Consumption can end the System Life of the MK48Z32/32Y. Since these mechanisms are independent, the lower of the two estimated lifetimes defines the Battery Life. At 70°C the System Life of the MK48Z32/32Y would be at least 10 years.

ORDERING INFORMATION

Example: MK48Z32 B 70



Package		Speed	
B	PHDIP28	70	70ns
		12	120ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.