PIPELINE 166/150/133/117 MHz 256K x 18 Synchronous FLOW THROUGH 133/117/100/66 MHz

FEATURES

- 3.3V +5%/-5% Core power supply, 2.5V or 3.3V I/O supply.
- FT mode pin for FLOW THROUGH or PIPELINE operation.
- LBO pin for linear or interleave (Pentium™ and X86) burst mode.
- Byte write (BWE) and global write (GW) operation.
- 3 chip enable signals for easy depth expansion.
- Common data inputs and data outputs.
- Clock Control, registered, address, data, and control.
- Internal Self-Timed WRITE cycle.
- Automatic power-down for portable applications.
- JEDEC standard 100-lead TQFP package and 119-BGA:
  T: TQFP or B: BGA

FLOW THROUGH ONLY

- High frequency operation: 133MHz
- Fast access time: 7.5, 8, 8.5, and 20ns.
- High-performance 2-1-1-1 access rate.
- Fast OE access times: 3.5ns.

PIPELINE ONLY

- High frequency operation: 166 MHz.
- Fast Clock to Output (Q): 3.5ns, 3.8ns and 4ns.
- High performance 3-1-1-1 access rate.
- Fast Cycle Times: 6ns, 6.7ns and 7.5ns.

FUNCTIONAL DESCRIPTION

The GS84018 is a 256K x 18 high performance synchronous SRAM with 2 bit burst counter. It is designed to provide L2 Cache for Pentium™ and other high performance CPU.Addresses, data IOs, chip enables (CE1, CE2, CE3), address control inputs (ADSP, ADSC, ADV), and write control inputs (BW1, BW2, BW3, BW4, BWE, GW) are synchronous and are controlled by a positive edge triggered clock (CLK).

Output enable (OE) and power down control (ZZ) are asynchronous. Burst can be initiated with either ADSP or ADSC inputs. Subsequent burst addresses are generated internally and are controlled by ADV. The burst sequence is either interleave order (Pentium™ or x86) or linear order and is controlled by LBO.

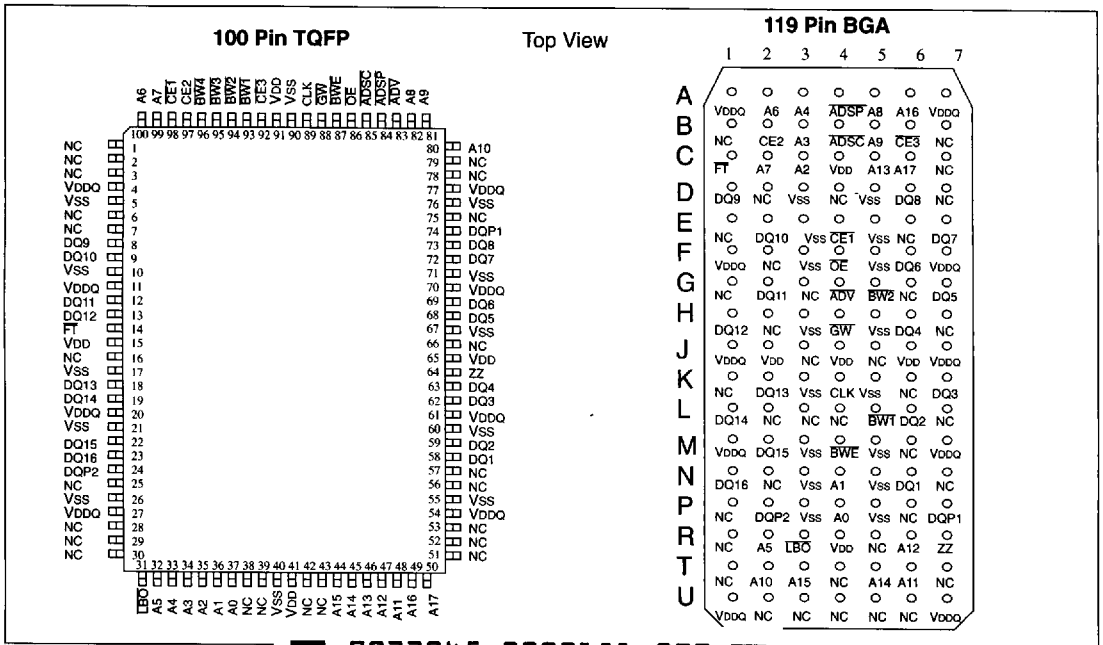
Output registers are provided and controlled by the FT mode pin (#14). Through use of the FT mode pin; Input/Output registers can be programmed to perform PIPELINE or FLOW THROUGH operation. FLOW THROUGH mode reduces latency.

Byte write operation is performed by using byte write enable (BWE) input combined with 4 individual byte write signals BW1-4. In addition, Global Write (GW) is available for writing all bytes at one time.

Low power (standby mode) is attained through the assertion of the ZZ signal, or by stopping the clock (CLK). Memory data is retained during standby mode.

The GS84018 operates on a 3.3V power supply and all inputs/outputs are 3.3V or 2.5V LVTTL compatible. Separate output (VDDQ) and ground (VSSQ) pins are used to de-couple output noise from the internal circuit.

*** Pentium is a trademark of Intel Corp.



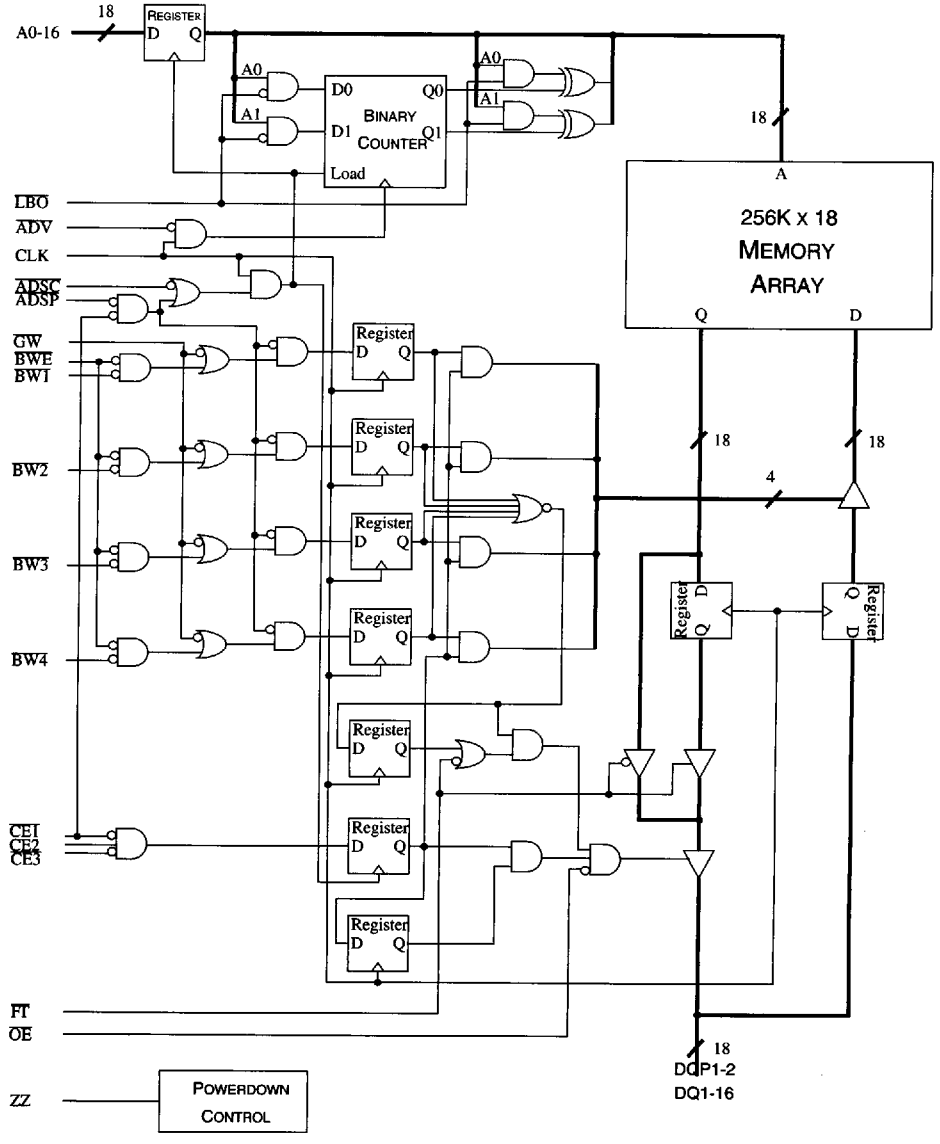
TQFP Pin Description

Pin Location	Symbol	Description
32, 33, 34, 35, 36, 37 ,44, 45, 46,47, 48, 49, 50, 80, 81, 82, 99, 100	A0-17	Address Input Signals. Inputs are registered and must meet setup and hold times as specified on page 11.
89	CLK	Clock Input Signal.
87	$\overline{BWE}$	Byte Write Enable Signal. The byte write enable signal needs to be combined with one of the four byte write signals or global write for a write operation to occur.
93	$\overline{BW1}$	Byte Write signal for data outputs 1thru 8.
94	$\overline{BW2}$	Byte Write signal for data outputs 9thru 16.
88	$\overline{GW}$	Global Write Enable. This signal combined with $\overline{BWE}$ enables
92, 97, 98	$\overline{CE1}$,CE2, $\overline{CE3}$	Chip Enables.
86	$\overline{OE}$	Output Enable.
83	$\overline{ADV}$	Burst address advance.
84, 85	$\overline{ADSP}$, $\overline{ADSC}$	Address status signals.
8, 9, 12, 13, 18, 19, 22, 23, 58, 59, 62 ,63, 68, 69, 72, 73	DQ1-16	Data Input and Output pins.
74, 24	DQP1-2	Parity Input and Output pins.
64	ZZ	Power down control. Application of ZZ will result in a low standby power consumption.
14	$\overline{FT}$	Flow Through or Pipeline mode.
31	$\overline{LBO}$	Linear Order burst mode.
15, 41, 65, 91	V_{DD}	3.3V power supply.
5,10,17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Ground.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	3.3V output power supply for noise reduction.
1, 2, 3, 6, 7, 16, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	No Connect.

PBGA PIN DESCRIPTION

Pin Location	Symbol	Description
2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	A0-17	Address Input Signals. Inputs are registered and must meet setup and hold times as specified on page 11.
4K	CLK	Clock Input Signal.
4M	$\overline{BWE}$	Byte Write Enable Signal. The byte write enable signal needs to be combined with one of the four byte write signals or global write for a write operation to occur.
3G	$\overline{BW1}$	Byte Write signal for data outputs 1thru 8.
3L	$\overline{BW2}$	Byte Write signal for data outputs 9thru 16.
4H	$\overline{GW}$	Global Write Enable. This signal combined with $\overline{BWE}$ enables
4E, 2B, 6B	$\overline{CE1}$,CE2, $\overline{CE3}$	Chip Enables.
4F	$\overline{OE}$	Output Enable.
4G	$\overline{ADV}$	Burst address advance.
4A, 4B	$\overline{ADSP}$, $\overline{ADSC}$	Address status signals.
1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N	DQ1-16	Data Input and Output pins.
2P, 7P	DQP1-2	Parity Input and Output pins.
7R	ZZ	Power down control. Application of ZZ will result in a low standby power consumption.
1C	$\overline{FT}$	Flow Through or Pipeline mode.
3R	$\overline{LBO}$	Linear Order burst mode.
4C, 2J, 4J, 6J, 4R	V_{DD}	3.3V power supply.
3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Ground.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	V_{DDQ}	3.3V output power supply for noise reduction.
1B, 7B, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 1T, 4T, 7T, 2U, 3U, 4U, 5U, 6U	NC	No Connect.

FUNCTIONAL BLOCK DIAGRAM



3

MODE PIN FUNCTION

$\overline{\text{LBO}}$	FUNCTION
L	LINEAR BURST
H OR NC	INTERLEAVED BURST

$\overline{\text{FT}}$	FUNCTION
L	FLOW THROUGH
H OR NC	PIPELINE

POWER DOWN CONTROL

ZZ	FUNCTION
L OR NC	ACTIVE
H	STANDBY, IDD = ISB

NOTE:

THERE ARE PULL UP DEVICES ON $\overline{\text{LBO}}$ AND $\overline{\text{FT}}$ PINS AND PULL DOWN DEVICE ON ZZ PIN, SO THOSE INPUT PINS CAN BE UNCONNECTED AND THE CHIP WILL OPERATE IN THE DEFAULT STATES AS SPECIFIED IN THE ABOVE TABLES.

LINEAR BURST SEQUENCE

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1ST ADDRESS	00	01	10	11
2ND ADDRESS	01	10	11	00
3RD ADDRESS	10	11	00	01
4TH ADDRESS	11	00	01	10

THE BURST WRAP AROUND TO INITIAL STATE UPON COMPLETION.

INTERLEAVED BURST SEQUENCE

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1ST ADDRESS	00	01	10	11
2ND ADDRESS	01	00	11	10
3RD ADDRESS	10	11	00	01
4TH ADDRESS	11	10	01	00

THE BURST WRAP AROUND TO INITIAL STATE UPON COMPLETION.

BYTE WRITE FUNCTION

FUNCTION	$\overline{\text{SGW}}$	$\overline{\text{BWE}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	$\overline{\text{BW4}}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE ALL BYTES	L	X	X	X	X	X
WRITE ALL BYTES	H	L	L	L	L	L
WRITE BYTE 1	H	L	L	H	H	H
WRITE BYTE 2	H	L	H	L	H	H
WRITE BYTE 3	H	L	H	H	L	H
WRITE BYTE 4	H	L	H	H	H	L

NOTE:

H = LOGIC HIGH, L = LOGIC LOW, NC = NO CONNECT

PIPELINE 166/150/133/117 MHz 256K x 18 Synchronous FLOW THROUGH 133/117/100/66 MHz

SYNCHRONOUS TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
DESELECT CYCLE, POWER DOWN	NONE	H	X	X	X	L	X	X	X	L-H	HIGH-Z
DESELECT CYCLE, POWER DOWN	NONE	L	L	X	L	X	X	X	X	L-H	HIGH-Z
DESELECT CYCLE, POWER DOWN	NONE	L	X	H	L	X	X	X	X	L-H	HIGH-Z
DESELECT CYCLE, POWER DOWN	NONE	L	L	X	H	L	X	X	X	L-H	HIGH-Z
DESELECT CYCLE, POWER DOWN	NONE	L	X	H	H	L	X	X	X	L-H	HIGH-Z
READ CYCLE, BEGIN BURST	EXTERNAL	L	H	L	L	X	X	X	L	L-H	Q
READ CYCLE, BEGIN BURST	EXTERNAL	L	H	L	L	X	X	X	H	L-H	HIGH-Z
READ CYCLE, BEGIN BURST	EXTERNAL	L	H	L	H	L	X	H	L	L-H	Q
READ CYCLE, BEGIN BURST	EXTERNAL	L	H	L	H	L	X	H	H	L-H	HIGH-Z
WRITE CYCLE, BEGIN BURST	EXTERNAL	L	H	L	H	L	X	L	X	L-H	D
READ CYCLE, CONTINUE BURST	NEXT	X	X	X	H	H	L	H	L	L-H	Q
READ CYCLE, CONTINUE BURST	NEXT	X	X	X	H	H	L	H	H	L-H	HIGH-Z
READ CYCLE, CONTINUE BURST	NEXT	H	X	X	X	H	L	H	L	L-H	Q
READ CYCLE, CONTINUE BURST	NEXT	H	X	X	X	H	L	H	H	L-H	HIGH-Z
WRITE CYCLE, CONTINUE BURST	NEXT	X	X	X	H	H	L	L	X	L-H	D
WRITE CYCLE, CONTINUE BURST	NEXT	H	X	X	X	H	L	L	X	L-H	D
READ CYCLE, SUSPEND BURST	CURRENT	X	X	X	H	H	H	H	L	L-H	Q
READ CYCLE, SUSPEND BURST	CURRENT	X	X	X	H	H	H	H	H	L-H	HIGH-Z
READ CYCLE, SUSPEND BURST	CURRENT	H	X	X	X	H	H	H	L	L-H	Q
READ CYCLE, SUSPEND BURST	CURRENT	H	X	X	X	H	H	H	H	L-H	HIGH-Z
WRITE CYCLE, SUSPEND BURST	CURRENT	X	X	X	H	H	H	L	X	L-H	D
WRITE CYCLE, SUSPEND BURST	CURRENT	H	X	X	X	H	H	L	X	L-H	D

NOTE:

1. X MEANS "DON'T CARE," H MEANS "LOGIC HIGH," L MEANS "LOGIC LOW."
2. $\overline{BWx}$ IS THE LOGIC FUNCTION OF $\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$. SEE BYTE WRITE FUNCTION TABLE FOR DETAIL. (PAGE 5)
3. ALL INPUTS, EXCEPT $\overline{OE}$, MUST MEET SETUP AND HOLD ON RISING EDGE OF CLK.
4. SUSPENDING BUSRT GENERATES A WAIT CYCLE.
5. $\overline{ADSP}$ LOW ALONG WITH SRAM BEING SELECTED ALWAYS INITIATES A READ CYCLE AT THE L-H EDGE OF THE CLOCK (CLK).
6. A WRITE CYCLE CAN ONLY BE PERFORMED BY SETTING $\overline{WRITE}$ LOW FOR THE CLOCK L-H EDGE OF THE SUBSEQUENT WAIT CYCLE.
   REFER TO PAGE 12 FOR THE WRITE TIMING DIAGRAM.

PARTIAL TRUTH TABLE FOR READ/WRITE OPERATION

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE ONE BYTE	H	L	L	H	H	H
WRITE ALL BYTES	H	L	L	L	L	L
WRITE ALL BYTES	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (Voltage reference to VSS=0V)

SYMBOL	DESCRIPTION	COMMERCIAL	UNIT
V_{DD}	SUPPLY VOLTAGE	-0.5 TO 4.6	V
V_{DDQ}	OUTPUT SUPPLY VOLTAGE	-0.5 TO V_{DD}	V
V_{CLK}	CLK INPUT VOLTAGE	-0.5 TO 6	V
V_{IN}	INPUT VOLTAGE	-0.5 TO V_{DD}+0.5 (≤ 4.6 V MAX.)	V
V_{OUT}	OUTPUT VOLTAGE	-0.5 TO V_{DD}+0.5 (≤ 4.6 V MAX.)	V
I_{OUT}	OUTPUT CURRENT PER I/O	+/- 20	mA
P_D	POWER DISSIPATION	1.5	W
T_{OPR}	OPERATING TEMPERATURE	0 TO 70	°C
T_{STG}	STORAGE TEMPERATURE	-55 TO 125	°C

NOTE:

PERMANENT DAMAGE TO THE DEVICE MAY OCCUR IF THE ABSOLUTE MAXIMUN RATINGS ARE EXCEEDED. FUNCTIONAL OPERATION SHOULD BE RESTRICTED TO THE RECOMMENDED OPERATION CONDITIONS. EXPOSURE TO HIGHER THAN RECOMMENDED VOLTAGES, FOR AN EXTENDED PERIOD OF TIME, COULD EFFECT THE PERFORMANCE AND RELIABILITY OF THIS COMPONENT.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss=0V)

(VDD = 3.135V TO 3.45V, TA = 0°C TO +70°C FOR COMMERCIAL)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE	VDD	3.135	3.3	3.6	V
I/O SUPPLY VOLTAGE	VDDQ	2.375	2.5	VDD	V
INPUT HIGH VOLTAGE	VIH	1.7	---	VDD+0.3	V
INPUT LOW VOLTAGE	VIL	-0.3	---	0.8	V

NOTE:

INPUT OVERSHOOT VOLTAGE SHOULD BE LESS THAN VDD+2V AND NOT EXCEED 5NS.
INPUT UNDERSHOOT VOLTAGE SHOULD BE HIGHER THAN -2V AND NOT EXCEED 5NS.

CAPACITANCE (TA = 25C, F = 1MHZ, VDD = 3.3V)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNIT
CONTROL INPUT CAPACITANCE	CI	VDD=3.3V	3	4	PF
INPUT CAPCITANCE	CIN	VIN=0V	4	5	PF
OUTPUT CAPACITANCE	COUT	VOUT=0V	6	7	PF

NOTE:

THIS PARAMETER IS SAMPLE TESTED.

PACKAGE THERMAL CHARACTERISTICS

RATING	LAYER BOARD	SYMBOL	TQFP MAX	PBGA MAX	UNIT	*Notes*
JUNCTION TO AMBIENT (AT 200 LFM)	SINGLE	$R_{\Theta JA}$	32	28	°C/W	1,2
JUNCTION TO AMBIENT (AT 200 LFM)	FOUR	$R_{\Theta JA}$	20	18	°C/W	1,2
JUNCTION TO CASE (TOP)		$R_{\Theta JC}$	7	4	°C/W	3

NOTES:

1. JUNCTION TEMPERATURE IS A FUNCTION OF SRAM POWER DISSAPATION, PACKAGE THERMAL RESISTANCE, MOUNTING BOARD TEMPERATURE, AMBIENT. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. AVERAGE THERMAL RESISTANCE BETWEEN DIE AND TOP SURFACE, MIL SPEC-883, METHOD 1012.1.

AC TEST CONDITIONS

(V_{DD} = 3.135V TO 3.45V, T_A = 0°C TO 70°C)

PARAMETER	CONDITIONS
INPUT HIGH LEVEL	V_{IH} = 2.3V
INPUT LOW LEVEL	V_{IL} = 0.2V
INPUT SLEW RATE	T_R = 1V/NS
INPUT REFERENCE LEVEL	1.25V
OUTPUT REFERENCE LEVEL	1.25V
OUTPUT LOAD	FIG. 1& 2

NOTES:

1. INCLUDE SCOPE AND JIG CAPACITANCE.
2. TEST CONDITIONS AS SPECIFIED WITH OUTPUT LOADING AS SHOWN IN FIG. 1 UNLESS OTHERWISE NOTED.
3. OUTPUT LOAD 2 FOR T_{LZ}, T_{HZ}, T_{OLZ} AND T_{OHZ}.
4. DEVICE IS DESELECTED AS DEFINED BY THE TRUTH TABLE.

OUTPUT LOAD 1

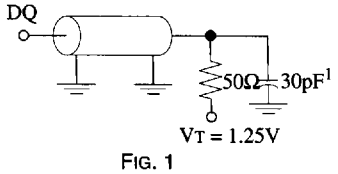


FIG. 1

OUTPUT LOAD 2

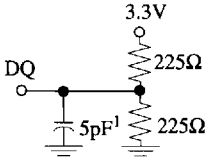


FIG. 2

FLOW THROUGH and PIPELINE Version

DC Characteristics and Supply Currents (Voltage reference to Vss = 0V)

(VDD = 3.135V to 3.45V, TA = 0°C to 70 °C for Commercial Temperature Offering)

Parameter	Symbol	Test Conditions	166MHz		150MHz		133MHz		117MHz		100MHz		66MHz	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Input Leakage Current (except ZZ, FT, LBO pins)	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA
Mode Input Current ($\overline{FT}$ & $\overline{LBO}$ pins)	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0V \leq V_{IN} \leq V_{IL}$	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 4mA, VDDQ = 2.375V	1.7V		1.7V		1.7V		1.7V		1.7V		1.7V	
Output High Voltage	V_{OH}	I_{OH} = - 4mA, VDDQ = 3.135V	2.4V		2.4V		2.4V		2.4V		2.4V		2.4V	
Output Low Voltage	V_{OL}	I_{OL} = + 4mA,		0.8V		0.8V		0.8V		0.8V		0.8V		0.8V

Parameter	Symbol	Test Conditions	166MHz		150MHz		133MHz		117MHz		100MHz		66MHz	
			0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C
Operating Current (V_{DD} = MAN, E = V_{IH})	I_{DD}	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL} Output Open	320mA	3Q98	295mA	3Q98	230mA	3Q98	210mA	3Q98	190mA	3Q98	150mA	3Q98
Standby Current	I_{SB}	ZZ ≥ V_{DD} - 0.2V	20mA	TBD	20mA	TBD	20mA	TBD	20mA	TBD	20mA	TBD	20mA	TBD
Deselect Supply Current	I_{DD}	Device Selected; All other inputs ≥ V_{IH} or ≤ V_{IL}	90mA	TBD	80mA	TBD	80mA	TBD	75mA	TBD	65mA	TBD	40mA	TBD

FLOW THROUGH Version

AC Electrical Characteristics

(VDD = 3.135V to 3.45V, TA = 0°C to 70 °C for Commercial)

Parameter	Symbol	133MHz		117MHz		100MHz		66MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KC}	7.5		8.5		10		15		NS	
Clock HIGH Time	t_{KH}	3	---	3	---	4	---	4.5	---	NS	
Clock LOW Time	t_{KL}	3	---	3	---	4	---	4.5	---	NS	
Clock to Output Vaid	t_{KQ}		7.5		8.5		10		12	NS	1
Clock to Output Invalid	t_{KQX}	2		2		2		2		NS	1
Clock High to Output in Low-Z	t_{KQLZ}	0	---	0	---	0	---	0	---	NS	1,2
Clock to Output in High-Z	t_{KQHZ}	2	3.5	2	3.5	2	3.5	2	3.5	NS	1,2
Output Enable to Output in Low-Z	t_{OELZ}	0		0		0		0		NS	1,2
Output to output in High-Z	t_{OEHZ}		3.5		3.5		3.5		3.5	NS	1,2
Setup time	t_S	1.5	---	1.5	---	2.0	---	2.0	---	NS	1
Hold time	t_H	0.5	---	0.5	---	0.5	---	0.5	---	NS	1
ZZ setup time	t_{ZZS3}	5	---	5	---	5	---	5	---	NS	1,3
ZZ hold time	t_{ZZH3}	1	---	1	---	1	---	1	---	NS	1,3
ZZ recovery	t_{ZZR}	20	---	20	---	20	---	20	---	NS	1,3

Notes:

1. Tested per AC Test Load, Figure 2 (page 9).
2. Measured at +/- 200mV from steady state.
3. ZZ is an asynchronous signal. In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

PIPELINE Version

AC Electrical Characteristics

(VDD = 3.135V to 3.45V, TA = 0°C to 70 °C for Commercial

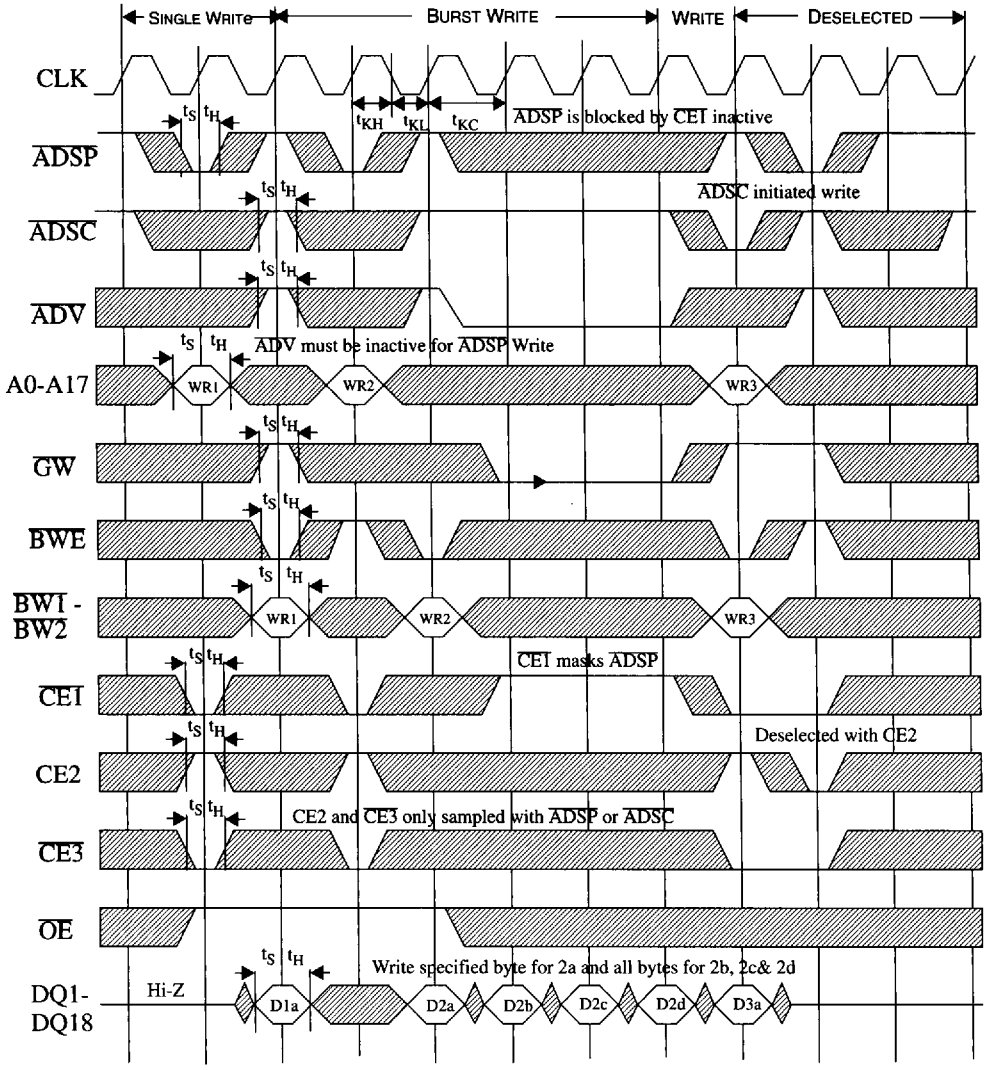
Parameter	Symbol	166MHz		150MHz		133MHz		117MHz		100MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KC}	6.0		6.7		7.5		8.5		10		NS	
Clock High Pulse Width	t_{KHW}	1.3		1.5		1.7		1.7		2.0			
Clock Low Pulse Width	t_{KLW}	1.5		1.7		1.9		1.9		2.5			
Clock Access Time	t_{KQ}		3.5		3.8		4		4		4.5	NS	
Clock to Output Invalid	t_{KQX}	1.5		1.5		1.5		1.5		1.5		NS	
Clock High to Output in Low-Z	t_{LZ}	0	---	0	---	0	---	0	---	0	---	NS	1,2
Clock to Output in High-Z	t_{HZ}		3.5		3.8		4		4		4,5	NS	1,2
Output Enable to Output Valid	t_{OEQ}		3.5		3.5		3.8		4		5	NS	1,2
Output Enable to output in High-Z	t_{OEHZ}		3.5		3.8		4		4		4.5	NS	1,2
Output Enable to output in Low-Z	t_{OLZ}		0		0		0		0		0	NS	1,2
Setup time	t_S	1.5	---	1.5	---	1.5	---	1.5	---	2.0	---	NS	1
Hold time	t_H	0.5	---	0.5	---	0.5	---	0.5	---	0.5	---	NS	1
ZZ setup time	t_{ZZS}	5	---	5	---	5	---	5	---	5	---	NS	1,3
ZZ hold time	t_{ZZH}	1	---	1	---	1	---	1	---	1	---	NS	1,3
ZZ recovery	t_{ZZR}	20	---	20	---	20	---	20	---	20	---	NS	1,3

Notes:

1. Tested per AC Test Load, Figure 2 (page 9).
2. Measured at +/- 200mV from steady state.
3. ZZ is an asynchronous signal. In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

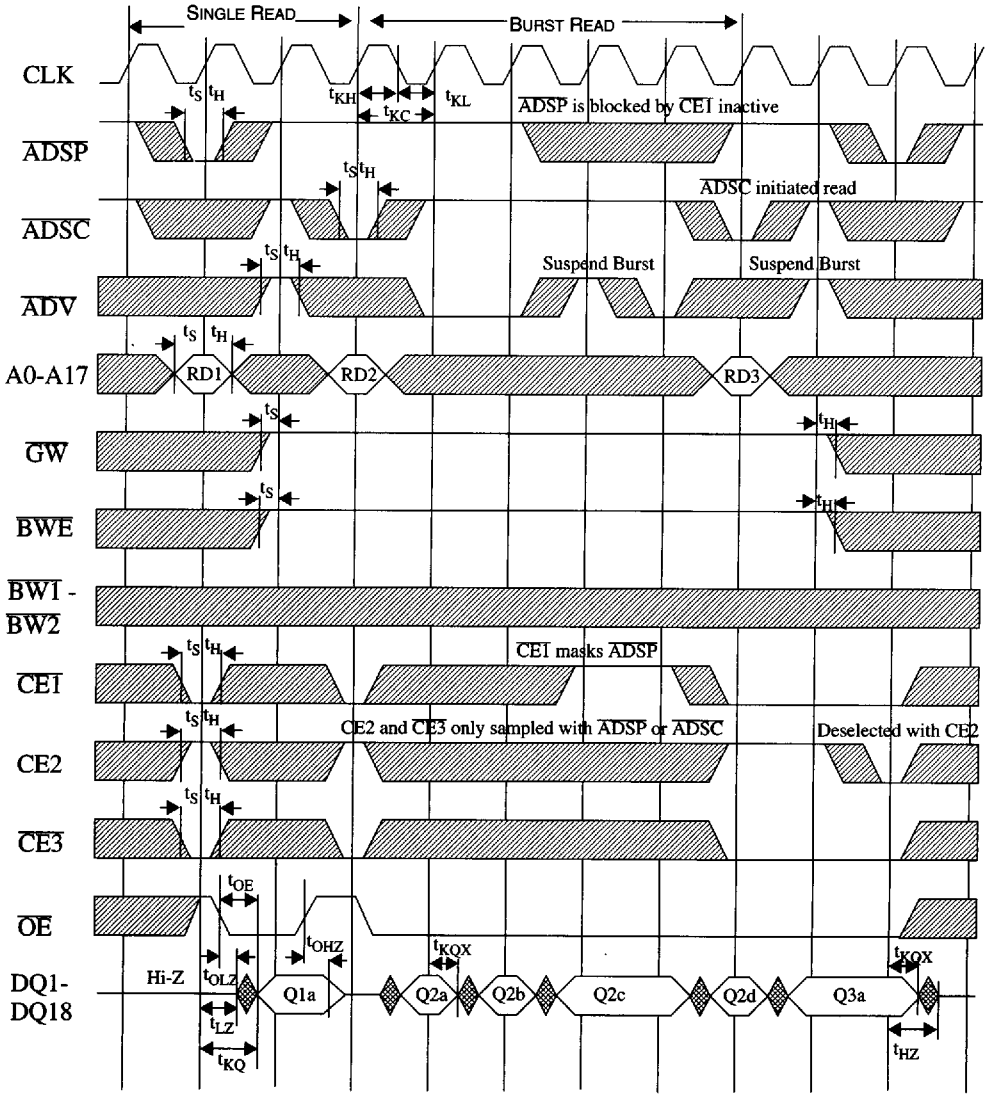
3

WRITE CYCLE TIMING



FLOW THROUGH

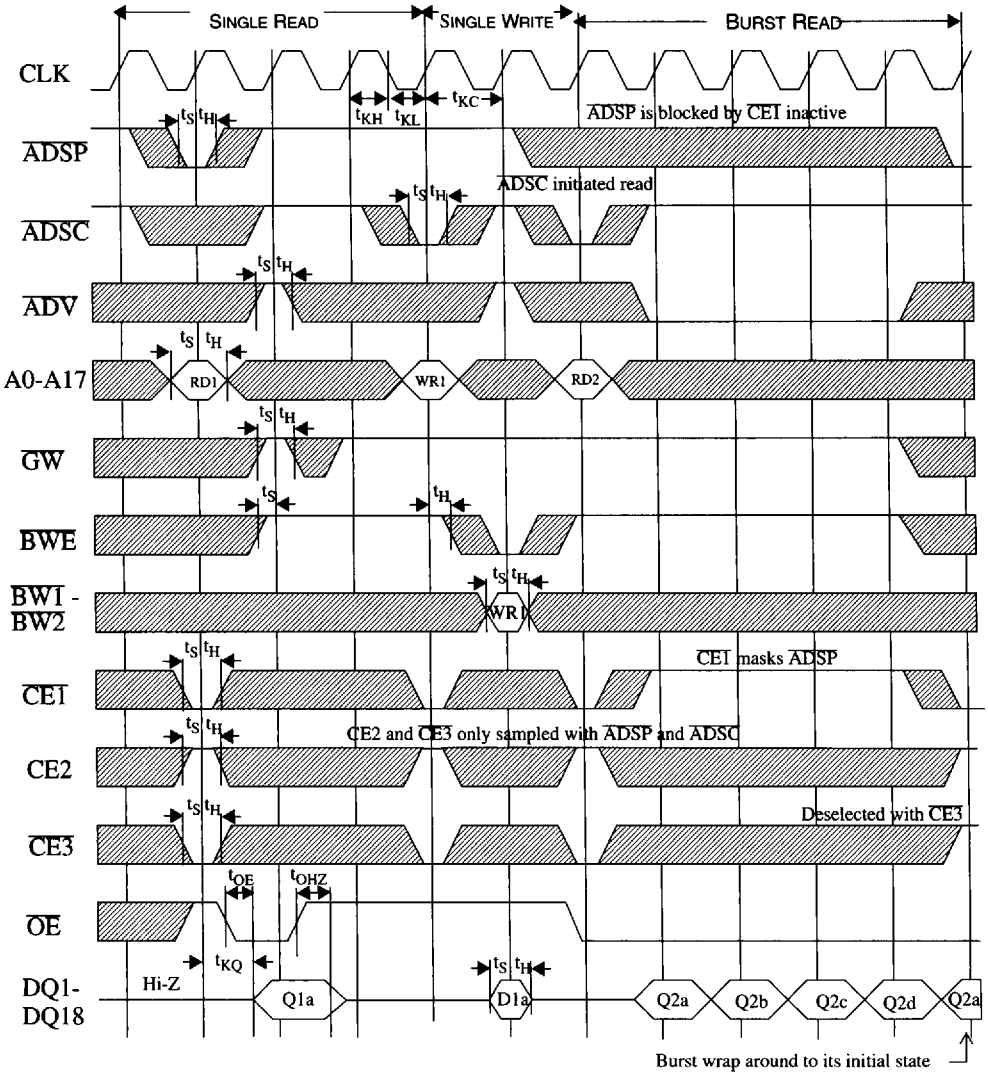
Read Cycle Timing



3

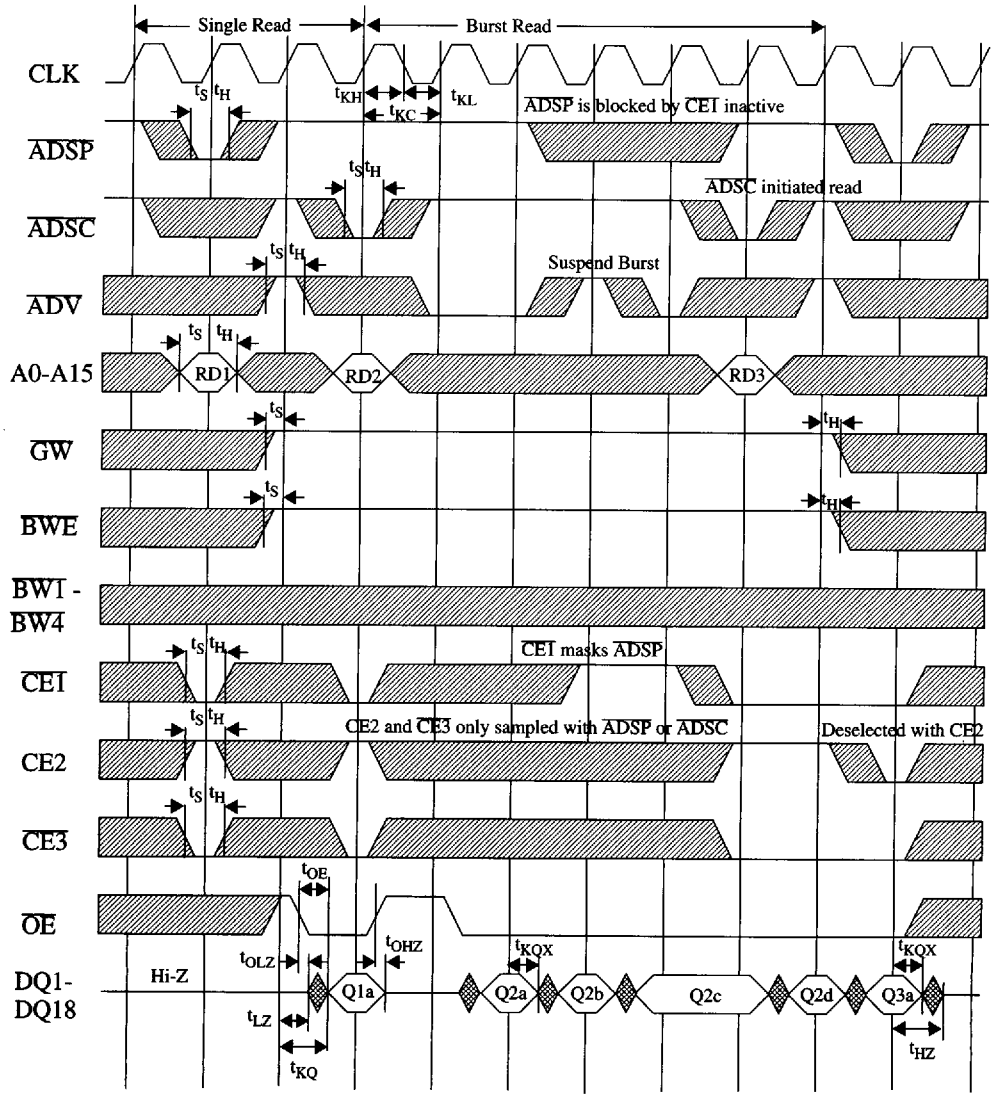
FLOW THROUGH

Read/Write Cycle Timing



PIPELINE

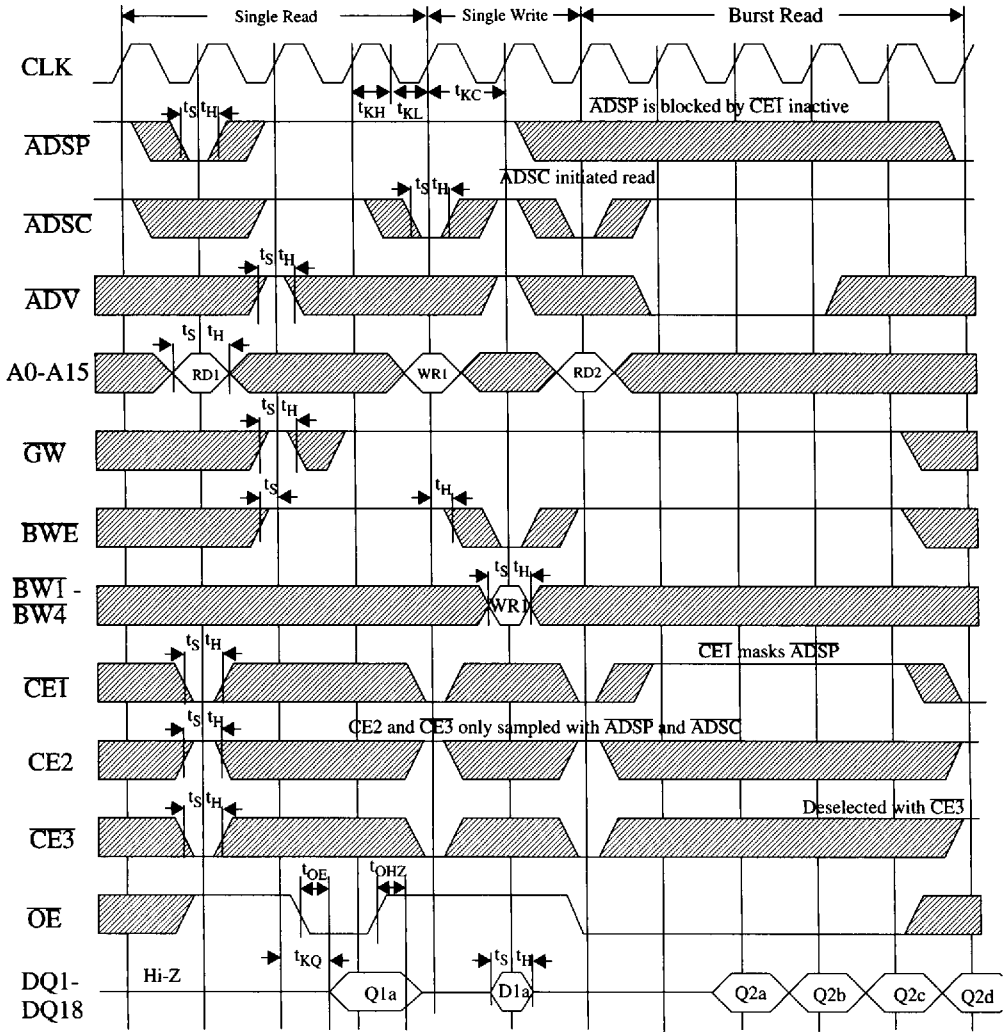
Read Cycle Timing



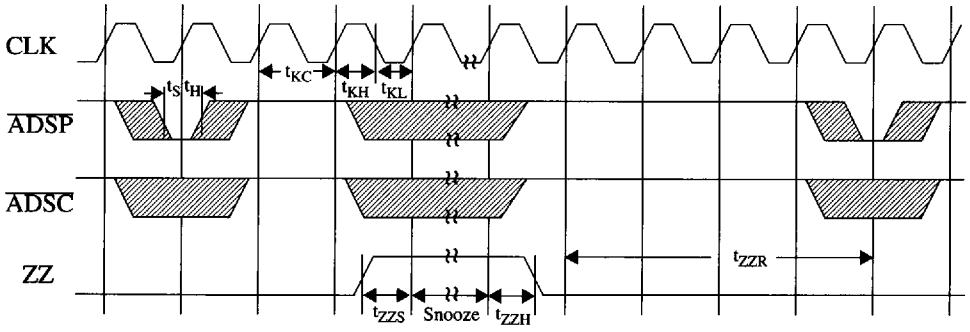
3

PIPELINE

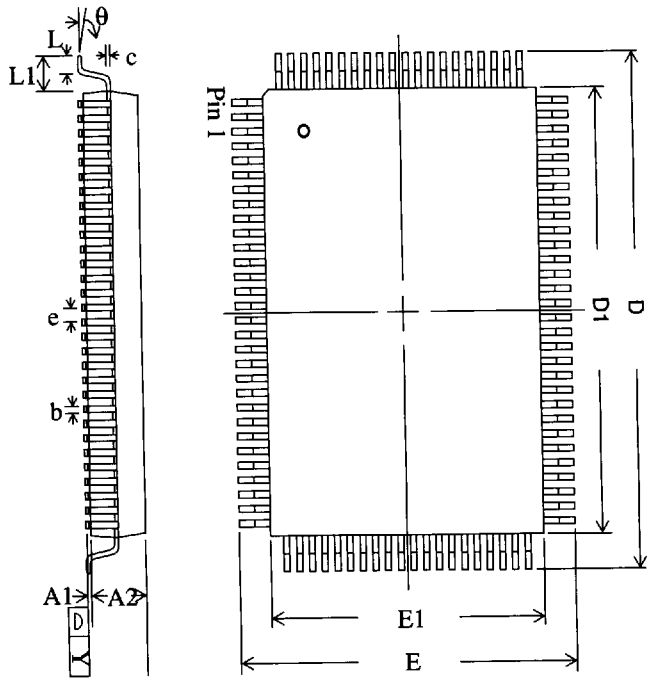
Read/Write Cycle Timing



ZZ TIMING



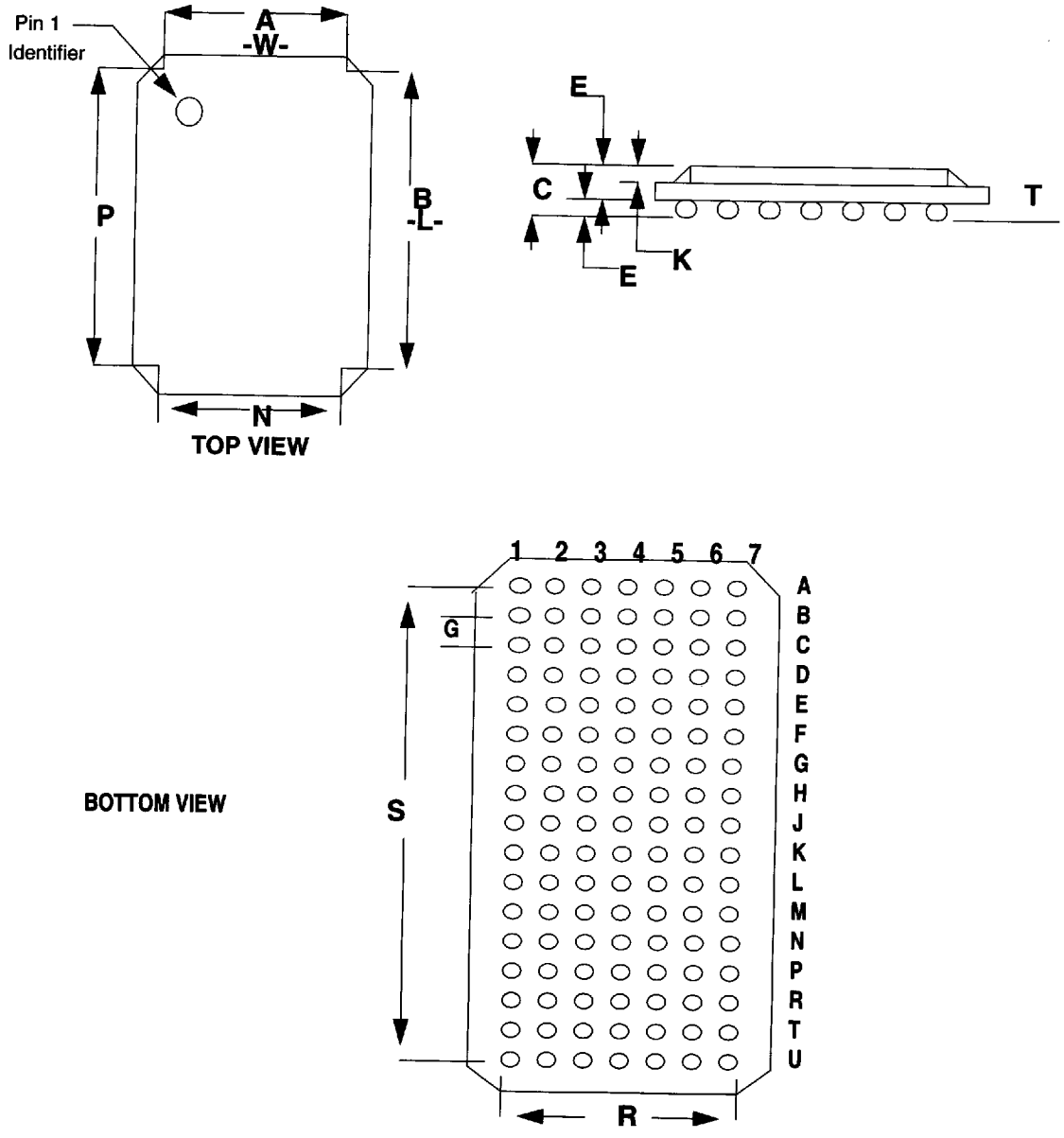
PACKAGE DIMENSIONS
100 PIN TQFP



SYMBOL	DESCRIPTION	MIN.	NOM.	MAX
A1	STANDOFF	0.05	0.10	0.15
A2	BODY THICKNESS	1.35	1.40	1.45
B	LEAD WIDTH	0.20	0.30	0.40
C	LEAD THICKNESS	0.09		0.20
D	TERMINAL DIMENSION	21.9	22.0	20.1
D1	PACKAGE BODY	19.9	20.0	20.1
E	TERMINAL DIMENSION	15.9	16.0	16.1
E1	PACKAGE BODY	13.9	14.0	14.1
E	LEAD PITCH		0.65	
L	FOOT LENGTH	0.45	0.60	0.75
L1	LEAD LENGTH		1.00	
Y	COPLANARITY			0.10
Q	LEAD ANGLE	0°		7°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION.

PACKAGE DIMESIONS - 119 PIN PBGA



PACKAGE DIMESIONS - 119 PIN PBGA

SYMBOL	DESCRIPTION	MIN.	MAX
A	WIDTH	.551	.551
B	LENGTH	.866	.866
C	PACKAGE HEIGHT (INCLUDING BALL)	-	0.094
D	BALL SIZE	0.024	0.035
E	BALL HEIGHT	0.020	0.028
F	PACKAGE HEIGHT (EXCLUDING BALLS)	0.051	0.067
G	WIDTH BETWEEN BALLS	0.050	0.050
K	PACKAGE HEIGHT ABOVE BOARD	0.031	0.039
N	CUT-OUT PACKAGE WIDTH	0.469	0.476
P	FOOT LENGTH	0.764	0.772
R	WIDTH OF PACKAGE BETWEEN BALLS	0.800	0.800
S	LENGTH OF PACKAGE BETWEEN BALLS		0.10
T	VARIANCE OF BALL HEIGHT	0.006	0.006

ORDERING INFORMATION

THE GS84018 - PIPELINE VERSION IS AVAILABLE IN THE FOLLOWING FREQUENCIES:
166MHz, 150MHz, 133MHZ, 117MHz AND 66MHz

THE GS84018 - FLOW THROUGH VERSION IS AVAILABLE IN THE FOLLOWING FREQUENCIES:
133MHz, 117MHz, 100MHz, 66MHz

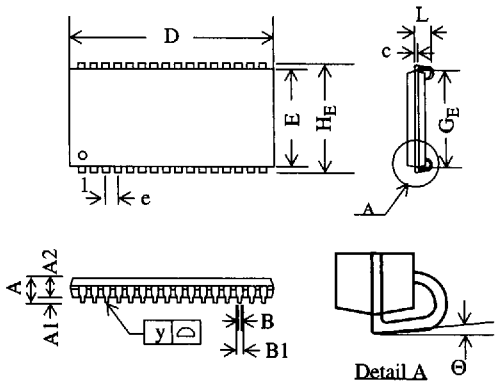
TO ORDER YOUR FAVORITE GSI TECHNOLOGY PART, REQUEST THE FOLLOWING PART:

GS84018T-(FREQUENCY DESIRED) FOR ORDERING THE 100-PIN THIN QUAD FLATPACK (TQFP)
GS84018B-(FREQUENCY DESIRED) FOR ORDERING THE 119-BALL GRID ARRAY (BGA)

****** PIPELINE AND FLOW THROUGH ARE SAME DEVICE ******

Package Dimensions

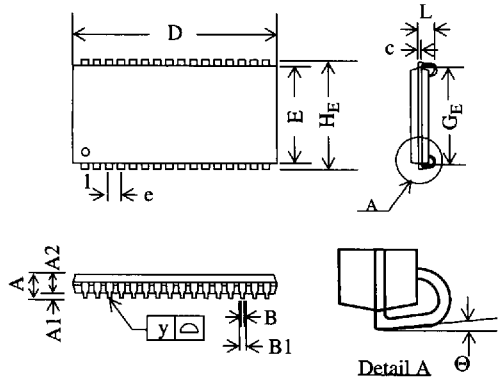
32 Pin SOJ, 400 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
H_E	0.430	0.435	0.440	10.93	11.05	11.17
G_E	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

32 Pin SOJ, 300 mil

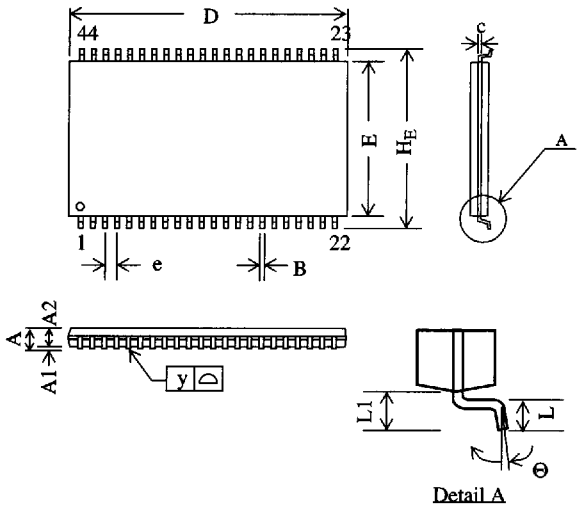


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.125	-	0.148	3.175	-	3.76
A1	0.026	-	-	0.66	-	-
A2	0.095	0.100	0.105	2.41	2.54	2.67
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.295	0.300	0.305	7.49	7.62	7.75
e	-	0.05	-	-	1.27	-
H_E	0.330	0.335	0.340	8.38	8.51	8.64
G_E	0.255	0.267	0.275	6.48	6.78	6.985
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

6

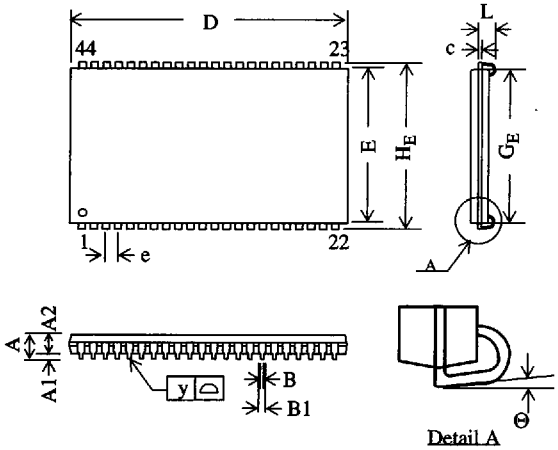
44 Pin TSOP type II, 400mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	-	0.031	-	-	0.80	-
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	5°	0°	-	5°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B does not include dambar protrusion / intrusion
3. Controlling dimension: mm

44 Pin SOJ, 400 mil

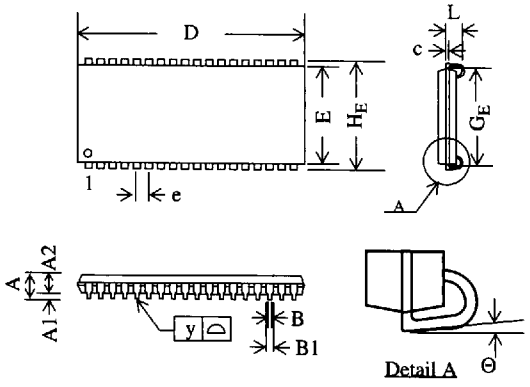


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.148	-	-	3.759
A1	0.025	-	-	0.635	-	-
A2	0.105	0.110	0.115	2.667	2.794	2.921
B	-	0.018	-	-	0.457	-
B1	0.026	0.028	0.032	0.660	0.711	0.813
c	-	0.008	-	-	0.203	-
D	1.120	1.125	1.130	28.44	28.58	28.70
E	0.395	0.400	0.405	10.033	10.160	10.287
e	-	0.05	-	-	1.27	-
H_E	0.435	0.440	0.445	11.049	11.176	11.303
G_E	0.360	0.370	0.380	9.144	9.398	9.652
L	0.082	0.087	0.106	2.083	2.210	2.70
y	-	-	0.004	-	-	0.102
Θ	0°	-	7°	0°	-	7°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

Package Dimensions

36 Pin SOJ, 400 mil

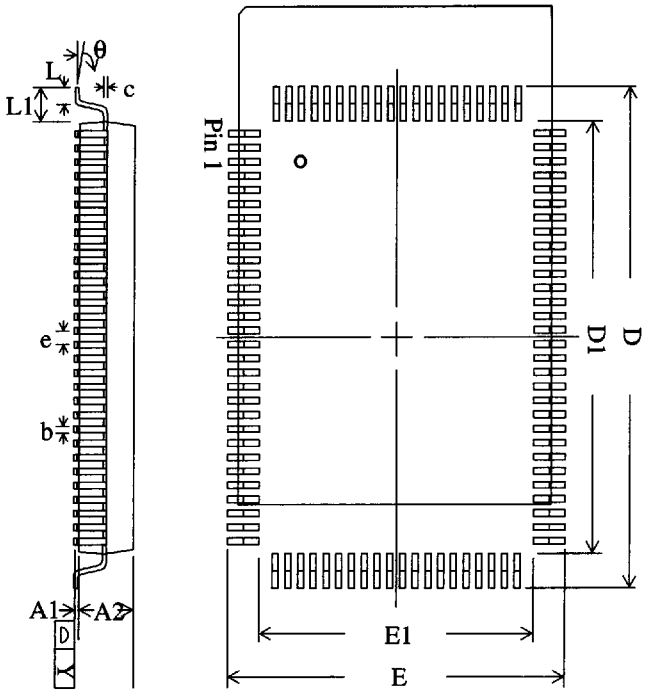


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.920	0.924	0.929	23.37	23.47	23.60
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
H_E	0.430	0.435	0.440	10.93	11.05	11.17
G_E	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Θ	0°	-	10°	0°	-	10°

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

6

Package Dimension
100 pin TQFP



		QFP (Q)			TQFP (T)		
Symbol	Description	Min.	Nom.	Max	Min.	Nom.	Max
A1	Stand Off	0.25	0.35	0.45	0.05	0.10	0.15
A2	Body Thickness	2.55	2.72	2.90	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40	0.20	0.30	0.40
c	Lead Thickness	0.10	0.15	0.20	0.09		0.20
D	Terminal Dimension	22.95	23.2	23.45	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1	19.9	20.0	20.1
E	Terminal Dimension	17.0	17.2	17.4	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1	13.9	14.0	14.1
e	Lead Pitch		0.65			0.65	
L	Foot Length	0.60	0.80	1.00	0.45	0.60	0.75
L1	Lead Length		1.60			1.00	
Y	Coplanarity			0.10			0.10
θ	Lead Angle	0°		7°	0°		7°

Note:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.