MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

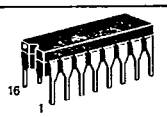
MC54/74HC75

Dual 2-Bit Transparent Latch
High-Performance Silicon-Gate CMOS

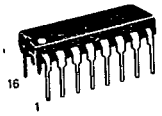
The MC54/74HC75 is identical in pinout to the LS75. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 2-bit transparent latches. Each latch stores the input data while Latch Enable is at a logic low. The outputs follow the data inputs when Latch Enable is at a logic high.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 80 FETs or 20 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06

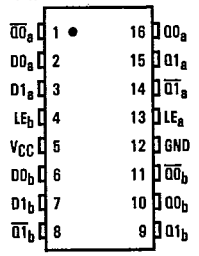
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

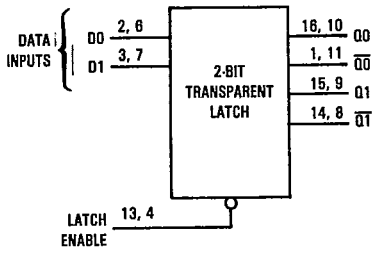
MC74HCXXN	Plastic
MC54HCXXJ	Ceramic
MC74HCXXD	SOIC

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 5 = V_{CC}
PIN 12 = GND

FUNCTION TABLE

Inputs		Outputs	
D	Latch Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

X = don't care
Q0 = latched data

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC}=2.0 V	0	1000	ns
		V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V; $\|I_{out}\|$ ≤20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V; $\|I_{out}\|$ ≤20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤4.0 mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\|$ ≤5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL}; $\|I_{out}\|$ ≤4.0 mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\|$ ≤5.2 mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND; I_{out}=0 μA	6.0	4	40	80	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q (Figures 1 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to $\overline{Q}$ (Figures 1 and 5)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to $\overline{Q}$ (Figures 2 and 5)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 5)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 35	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, D to Latch Enable (Figure 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Enable to D (Figure 4)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t_w	Minimum Pulse Width, Latch Enable Input (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

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SWITCHING WAVEFORMS

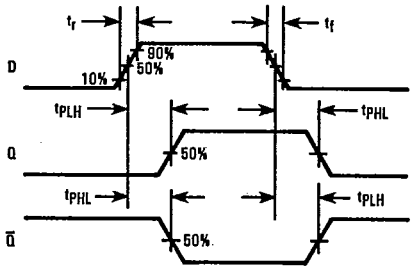


Figure 1

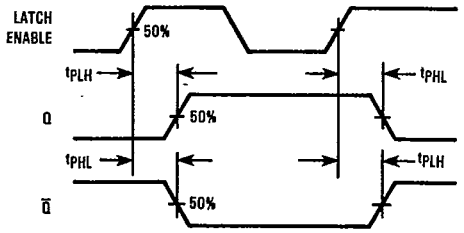


Figure 2

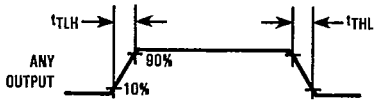


Figure 3

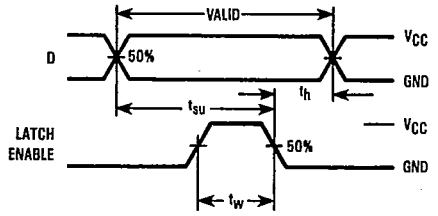
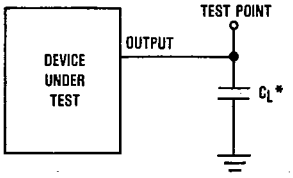


Figure 4



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

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EXPANDED LOGIC DIAGRAM