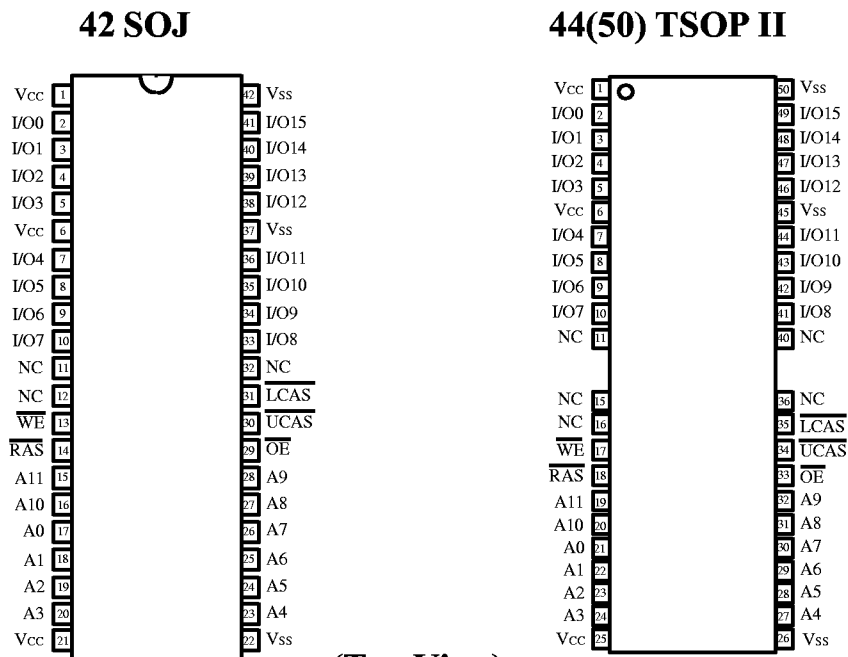


Description

The GM71C(S)16160C/CL is the new generation dynamic RAM organized 1,048,576 x 16 bit. GM71C(S)16160C/CL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C(S)16160C/CL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C(S)16160C/CL to be packaged in standard 400 mil 42 pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Pin Configuration



Features

- * 1,048,576 Words x 16 Bit Organization
- * Fast Page Mode Capability
- * Single Power Supply (5V+/-10%)
- * Fast Access Time & Cycle Time

(Unit: ns)

	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}
GM71C(S)16160C/CL-5	50	13	90	35
GM71C(S)16160C/CL-6	60	15	110	40
GM71C(S)16160C/CL-7	70	18	130	45

- * Low Power
 Active : 605/550/495mW (MAX)
 Standby : 11mW (CMOS level : MAX)
 0.83mW (L-version : MAX)
- * RAS Only Refresh, CAS before RAS Refresh,
 Hidden Refresh Capability
- * All inputs and outputs TTL Compatible
- * 4096 Refresh Cycles/64ms
- * 4096 Refresh Cycles/128ms (L-version)
- * Self Refresh Operation (L-version)
- * Battery Back Up Operation (L-version)
- * 2 CAS byte Control

Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	\overline{WE}	Read/Write Enable
A0-A11	Refresh Address Inputs	\overline{OE}	Output Enable
I/O0-I/O15	Data Input/ Data Output	V _{CC}	Power (+5V)
\overline{RAS}	Row Address Strobe	V _{SS}	Ground
$\overline{UCAS}, \overline{LCAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C(S)16160CJ/CLJ -5 GM71C(S)16160CJ/CLJ -6 GM71C(S)16160CJ/CLJ -7	50ns 60ns 70ns	400 Mil 42 Pin Plastic SOJ
GM71C(S)16160CT/CLT -5 GM71C(S)16160CT/CLT -6 GM71C(S)16160CT/CLT -7	50ns 60ns 70ns	400 Mil 44(50) Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ +70	C
T _{STG}	Storage Temperature (Plastic)	-55 ~ +125	C
V _{IN/OUT}	Voltage on any Pin Relative to V _{SS}	-1.0 ~ +7.0V	V
V _{CC}	Voltage on V _{CC} Relative to V _{SS}	-1.0 ~ +7.0V	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions ($T_A = 0 \sim +70C$)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	6.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

Note: All voltage referred to V_{SS}.

The supply voltage with all VCC pins must be on the same level. The supply voltage with all VSS pins must be on the same level.

Truth Table

\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{WE}	\overline{OE}	Output	Operation	Notes
H	D	D	D	D	Open	Standby	1,3
L	L	H	H	L	Valid	Lower byte	Read cycle 1,3
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L	D	Open	Lower byte	Early write cycle 1,2,3
L	H	L	L	D	Open	Upper byte	
L	L	L	L	D	Open	Word	
L	L	H	L	H	Undefined	Lower byte	Delayed Write cycle 1,2,3
L	H	L	L	H	Undefined	Upper byte	
L	L	L	L	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle 1,3
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
H to L	H	L	D	D	Open	Word	CBR Refresh or Self Refresh (L-series) 1,3
H to L	L	H	D	D	Open	Word	
H to L	L	L	D	D	Open	Word	
L	H	H	D	D	Open	Word	\overline{RAS} -only Refresh cycle 1,3
L	L	L	H	H	Open	Read cycle (Output disabled)	1,3

Notes: 1. H: High (inactive) L: Low(active) D: H or L

2. $twcs \geq 0ns$ Early write cycle

$twcs \leq 0ns$ Delayed write cycle

3. Mode is determined by the OR function of the \overline{UCAS} and \overline{LCAS} . (Mode is set by earliest of \overline{UCAS} and \overline{LCAS} active edge and reset by the latest of \overline{UCAS} and \overline{LCAS} inactive edge.) However write OPERATION and output High-Z control are done independently by each \overline{UCAS} , \overline{LCAS} .
ex) if $RAS = H$ to L , $UCAS = H$, $LCAS = L$, then \overline{CAS} -before- \overline{RAS} refresh cycle is selected.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0 \sim 70C$)

Symbol	Parameter	Min	Max	Unit	Note	
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	V_{CC}	V		
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	0	0.4	V		
I_{CC1}	Operating Current Average Power Supply Operating Current (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling: $t_{RC} = t_{RC \min}$)	50ns	-	110	mA	1, 2
		60ns	-	100		
		70ns	-	90		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} , $\overline{LCAS} = V_{IH}$, $D_{OUT} = \text{High-Z}$)	-	2	mA		
I_{CC3}	\overline{RAS} Only Refresh Current Average Power Supply Current \overline{RAS} Only Refresh Mode ($t_{RC} = t_{RC \min}$)	50ns	-	110	mA	2
		60ns	-	100		
		70ns	-	90		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($t_{PC} = t_{PC \min}$)	50ns	-	115	mA	1, 3
		60ns	-	105		
		70ns	-	95		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \geq V_{CC} - 0.2V$, $D_{OUT} = \text{High-Z}$)	-	1	mA		
		-	150	uA	5	
I_{CC6}	\overline{CAS} -before- \overline{RAS} Refresh Current ($t_{RC} = t_{RC \min}$)	50ns	-	110	mA	
		60ns	-	100		
		70ns	-	90		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) ($t_{RC}=31.3\mu s$, $t_{RAS} \leq 0.3\mu s$, $D_{OUT}=\text{High-Z}$)	-	500	uA	4,5	
I_{CC8}	Standby Current $\overline{RAS} = V_{IH}$ \overline{UCAS} , $\overline{LCAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	5	mA	1	
I_{CC9}	Self-Refresh Mode Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \leq 0.2V$, $D_{OUT}=\text{High-Z}$)	-	300	uA	5	
$I_{L(I)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 6V$)	-10	10	uA		
$I_{L(O)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 6V$)	-10	10	uA		

Note: 1. I_{CC} depends on output load condition when the device is selected.

$I_{CC}(\max)$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IH}$.

4. $\overline{UCAS} = L$ (≤ 0.2) and $\overline{LCAS} = L$ (≤ 0.2) while $\overline{RAS} = L$ (≤ 0.2).

5. L-version.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25C$)

Symbol	Parameter	Min	Max	Unit	Note
C _{I1}	Input Capacitance (Address)	-	5	§	1
C _{I2}	Input Capacitance (Clocks)	-	7	§	1
C _{I/O}	Output Capacitance (Data-In/Out)	-	7	§	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. UCAS and LCAS = V_{IH} to disable D_{OUT}.

AC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim +70C$, $V_{SS} = 0V$, Note 1, 2, 3, 19)

Test Conditions

Input rise and fall times : 5 ns

Input timing reference levels : 0.8V, 2.4V

Output timing reference levels : 0.4V, 2.4V

Output load : 2TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
t _{RP}	\overline{RAS} Precharge Time	30	-	40	-	50	-	ns	
t _{CP}	\overline{CAS} Precharge Time	7	-	10	-	10	-	ns	25
t _{RAS}	\overline{RAS} Pulse Width	50	10,000	60	10,000	70	10,000	ns	
t _{CAS}	\overline{CAS} Pulse Width	13	10,000	15	10,000	18	10,000	ns	
t _{ASR}	Row Address Set up Time	0	-	0	-	0	-	ns	
t _{RAH}	Row Address Hold Time	7	-	10	-	10	-	ns	
t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	22
t _{CAH}	Column Address Hold Time	7	-	10	-	15	-	ns	22
t _{RCD}	\overline{RAS} to \overline{CAS} Delay Time	17	45	20	45	20	52	ns	4
t _{RAD}	\overline{RAS} to Column Address Delay Time	12	30	15	30	15	35	ns	5
t _{RSH}	\overline{RAS} Hold Time	13	-	15	-	18	-	ns	
t _{CSH}	\overline{CAS} Hold Time	50	-	60	-	70	-	ns	
t _{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	5	-	5	-	5	-	ns	23
t _{ODD}	\overline{OE} to D _{IN} Delay Time	13	-	15	-	18	-	ns	6
t _{DZO}	\overline{OE} Delay Time from D _{IN}	0	-	0	-	0	-	ns	7
t _{DZC}	\overline{CAS} Delay Time from D _{IN}	0	-	0	-	0	-	ns	7
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8

Read Cycle

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	50	-	60	-	70	ns	9,10
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	13	-	15	-	18	ns	10,11,18
t _{AA}	Access Time from Address	-	25	-	30	-	35	ns	10,11,18
t _{OAC}	Access Time from $\overline{\text{OE}}$	-	13	-	15	-	18	ns	10,26
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	13,23
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	5	-	5	-	5	-	ns	13
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	25	-	30	-	35	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t _{OH0}	Output Data Hold Time from $\overline{\text{OE}}$	3	-	3	-	3	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	13	-	15	-	15	ns	14
t _{OEZ}	Output Buffer Turn-off Time to $\overline{\text{OE}}$	-	13	-	15	-	15	ns	14
t _{CDD}	$\overline{\text{CAS}}$ to D _{IN} Delay Time	13	-	15	-	18	-	ns	6

Write Cycle

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	15,22
t _{WCH}	Write Command Hold Time	7	-	10	-	15	-	ns	22
t _{WP}	Write Command Pulse Width	7	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	13	-	15	-	18	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	13	-	15	-	18	-	ns	24
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	16,24
t _{DH}	Data-in Hold Time	7	-	10	-	15	-	ns	16,24

Read-Modify-Write Cycle

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RWC}	Read-Modify-Write Cycle Time	131	-	155	-	181	-	ns	
t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	73	-	85	-	98	-	ns	15
t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	36	-	40	-	46	-	ns	15
t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	48	-	55	-	63	-	ns	15
t _{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	13	-	15	-	18	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	§	22
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	7	-	10	-	10	-	§	23
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	§	22

Fast Page Mode Cycle

Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	§	
t _{RASP}	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	§	17
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	§	10,18,23
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	30	-	35	-	40	-	§	

Fast Page Mode Read-Modify-Write Cycle


Symbol	Parameter	GM71C(S)16160 C/CL-5		GM71C(S)16160 C/CL-6		GM71C(S)16160 C/CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	76	-	85	-	96	-	§	
t _{CPW}	$\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge	53	-	60	-	68	-	§	15,23

Self Refresh Mode

Symbol	Parameter	GM71CS16160 CL-5		GM71CS16160 CL-6		GM71CS16160 CL-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RASS}	$\overline{\text{RAS}}$ Pulse Width(Self-Refresh)	100	-	100	-	100	-	us	27
t _{RPS}	$\overline{\text{RAS}}$ Precharge Time(Self-Refresh)	90	-	110	-	130	-	ns	
t _{CHS}	$\overline{\text{CAS}}$ Hold Time(Self-Refresh)	-50	-	-50	-	-50	-	ns	

Notes:

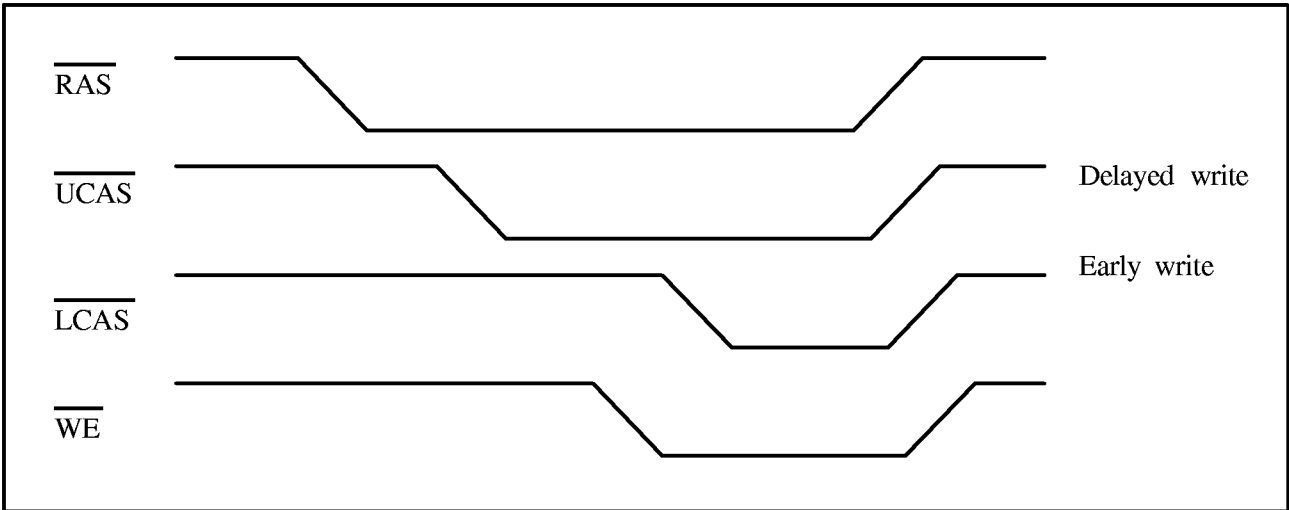
1. AC measurements assume t_T = 5ns.
2. An initial pause of 200us is required after power up followed by a minimum of eight initialization cycles(any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh).
If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. Only row address is indispensable on address A8, A9, A10, A11.
4. Operation with the t_{RCD(max)} limit insures that t_{RAC(max)} can be met, t_{RCD(max)} is specified as a reference point only; if t_{RCD} >= t_{RAD(max)} + t_{AA(max)} - t_{CAC(max)}, then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD(max)} limit insures that t_{RAC(max)} can be met, t_{RAD(max)} is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD(max)} limit, then access time is controlled exclusively by t_{AA}.
6. Either t_{ODD} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH(min)} and V_{IL(max)}.
9. Assumes that t_{RCD} <= t_{RCD(max)} and t_{RAD} <= t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2 TTL load and 100pF.
11. Assumes that t_{RCD} >= t_{RCD(max)} and t_{RCD} + t_{CAC(max)} >= t_{RAD} + t_{AA(max)}.
12. Assumes that t_{RAD} >= t_{RAD(max)} and t_{RCD} + t_{CAC(max)} <= t_{RAD} + t_{AA(max)}.

13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD(min)}$, $t_{CWD} \geq t_{CWD(min)}$, and $t_{AWD} \geq t_{AWD(min)}$, or $t_{CWD} \geq t_{CWD(min)}$, $t_{CWD} \geq t_{AWD(min)}$ and $t_{CPW} \geq t_{CPW(min)}$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.
16. These parameters are referred to \overline{UCAS} and \overline{LCAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines \overline{RAS} pulse width in fast page mode cycles.
18. Access time is determined by the longest among t_{AA} , t_{CAC} , and t_{ACP} .
19. In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device. After \overline{RAS} is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} < t_{CWL}$, invalid data will be out at each I/O.
20. When both \overline{UCAS} and \overline{LCAS} go low at the same time, all 16-bit data are written into the device. \overline{UCAS} and \overline{LCAS} cannot be staggered within the same write/read cycles.
21. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
22. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of \overline{UCAS} or \overline{LCAS} .
23. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of \overline{UCAS} or \overline{LCAS} .
24. t_{CWL} , t_{DH} , t_{DS} and t_{CSH} should be satisfied by both \overline{UCAS} and \overline{LCAS} .
25. t_{CP} is determined by that time the both \overline{UCAS} and \overline{LCAS} are high.
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained.
When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH min}/V_{IL max}$ level.
27. Please do not use t_{RASS} timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
28. If you use distributed CBR refresh within 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
29. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 64 or 16ms immediately after exiting from and before entering into the self refresh mode.
30. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
31.  H or L (H: $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$, L: $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$)

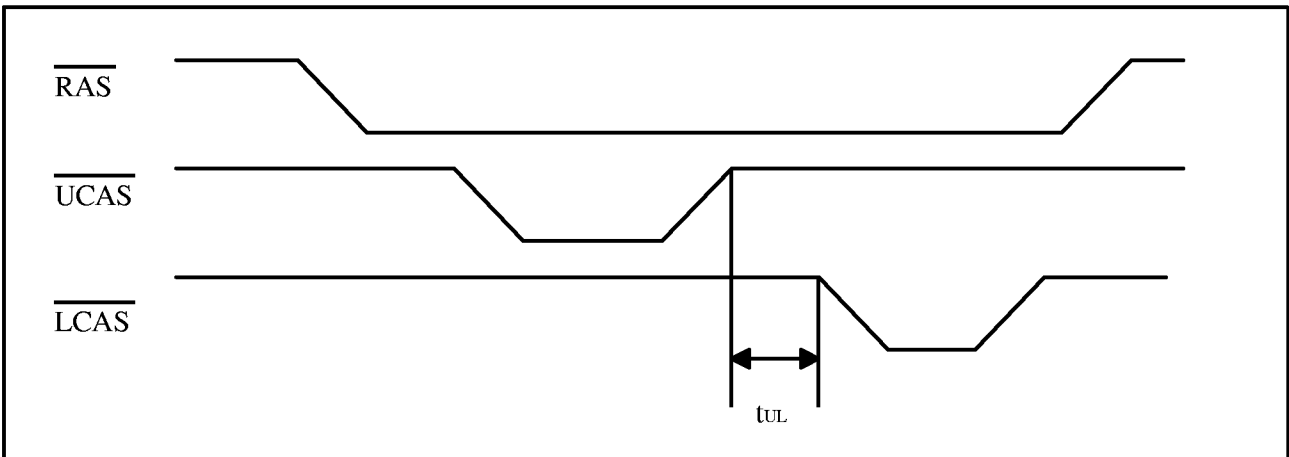
Notes concerning $\overline{2CAS}$ control

Please do not separate the \overline{UCAS} / \overline{LCAS} operation timing intentionally. However skew between \overline{UCAS} / \overline{LCAS} are allowed under the following conditions.

1. Each of the \overline{UCAS} / \overline{LCAS} should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed, such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} < t_{UL}$) is satisfied, fast page mode can be performed.



4. Byte control operation by remaining \overline{UCAS} or \overline{LCAS} high is guaranteed.

Timing Waveforms

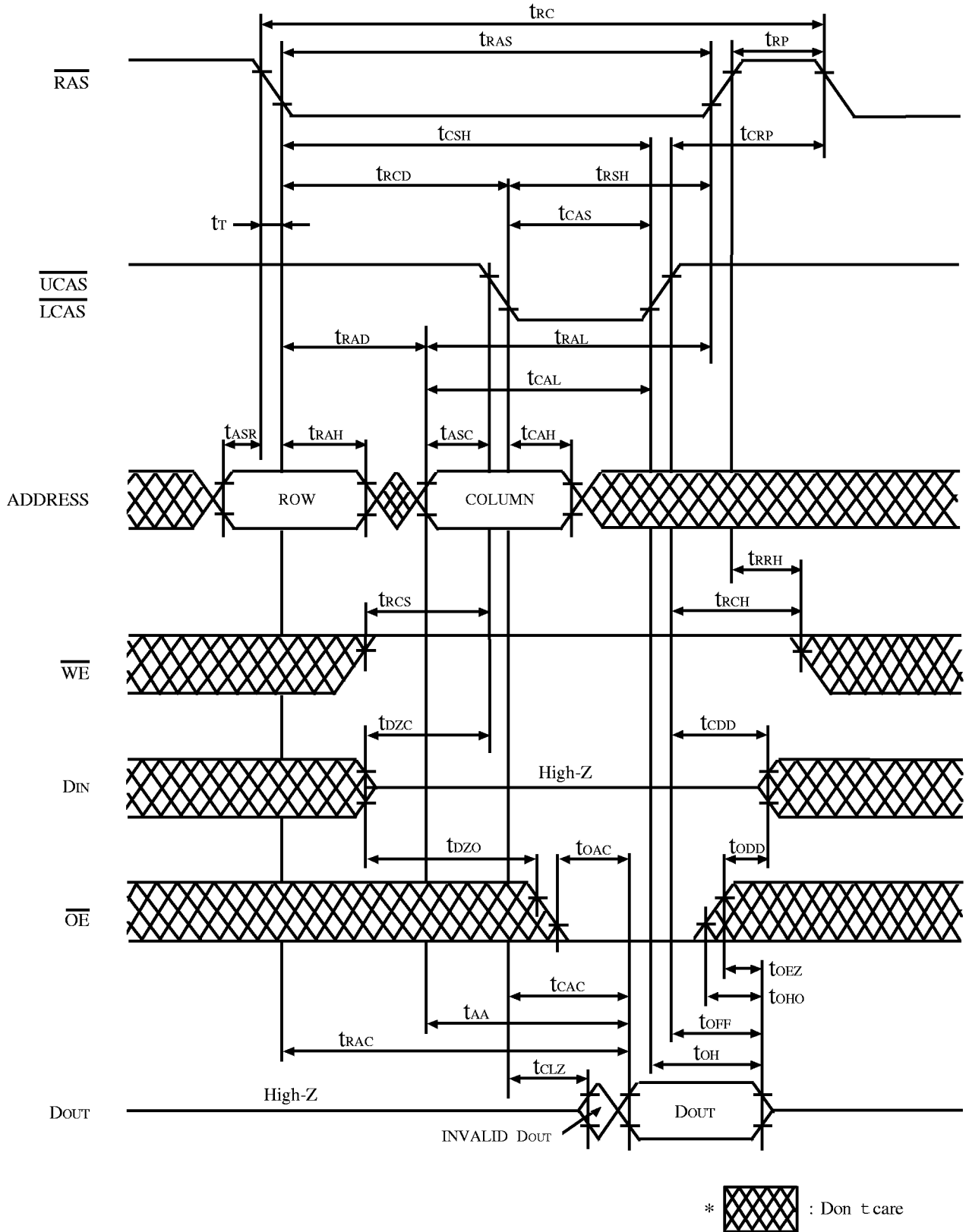
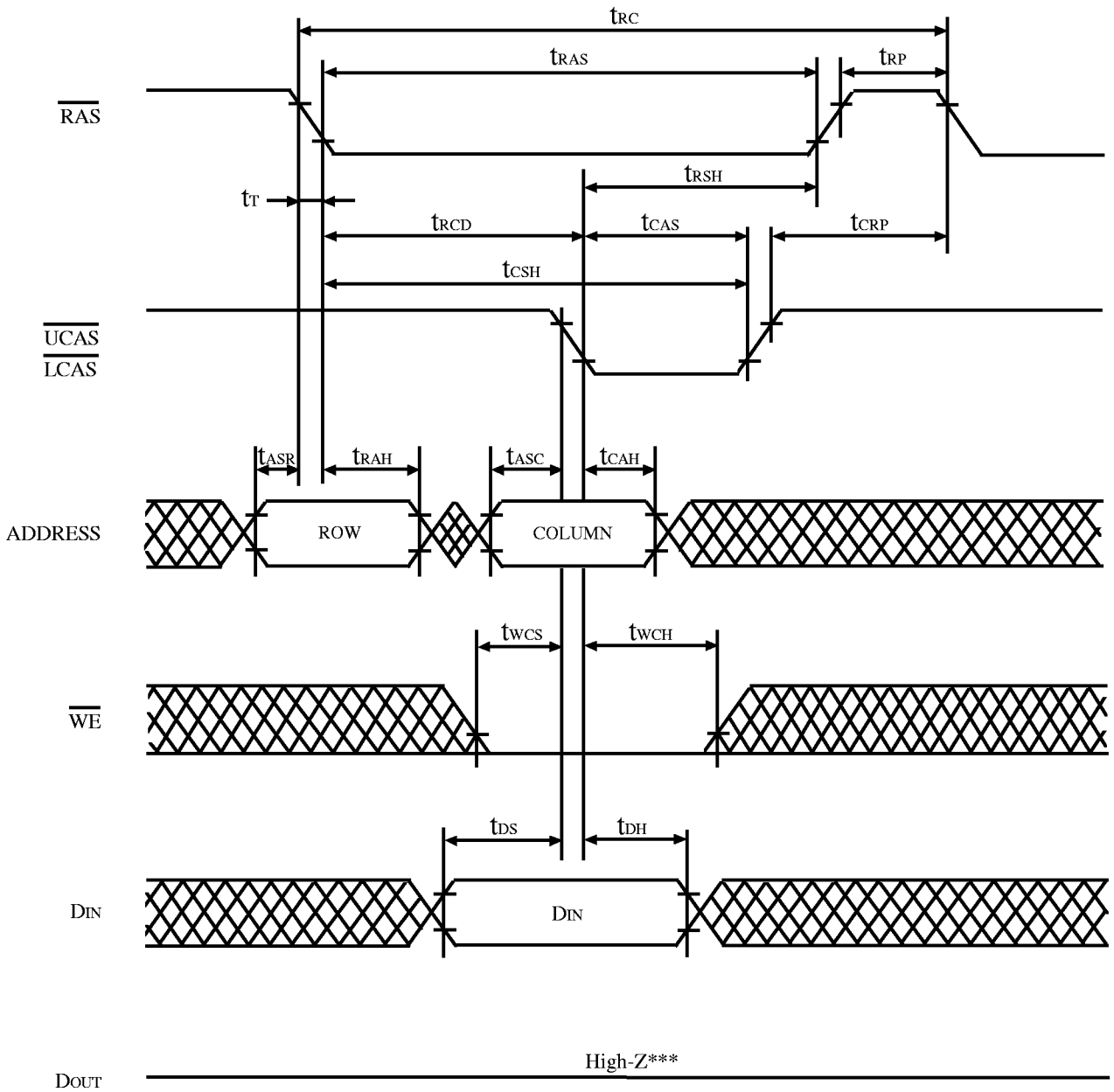


FIGURE 1. READ CYCLE



*  : Don't care

** \overline{OE} : Don't care

*** $t_{wcs} \geq t_{wcs}(\text{min})$

FIGURE 2. EARLY WRITE CYCLE

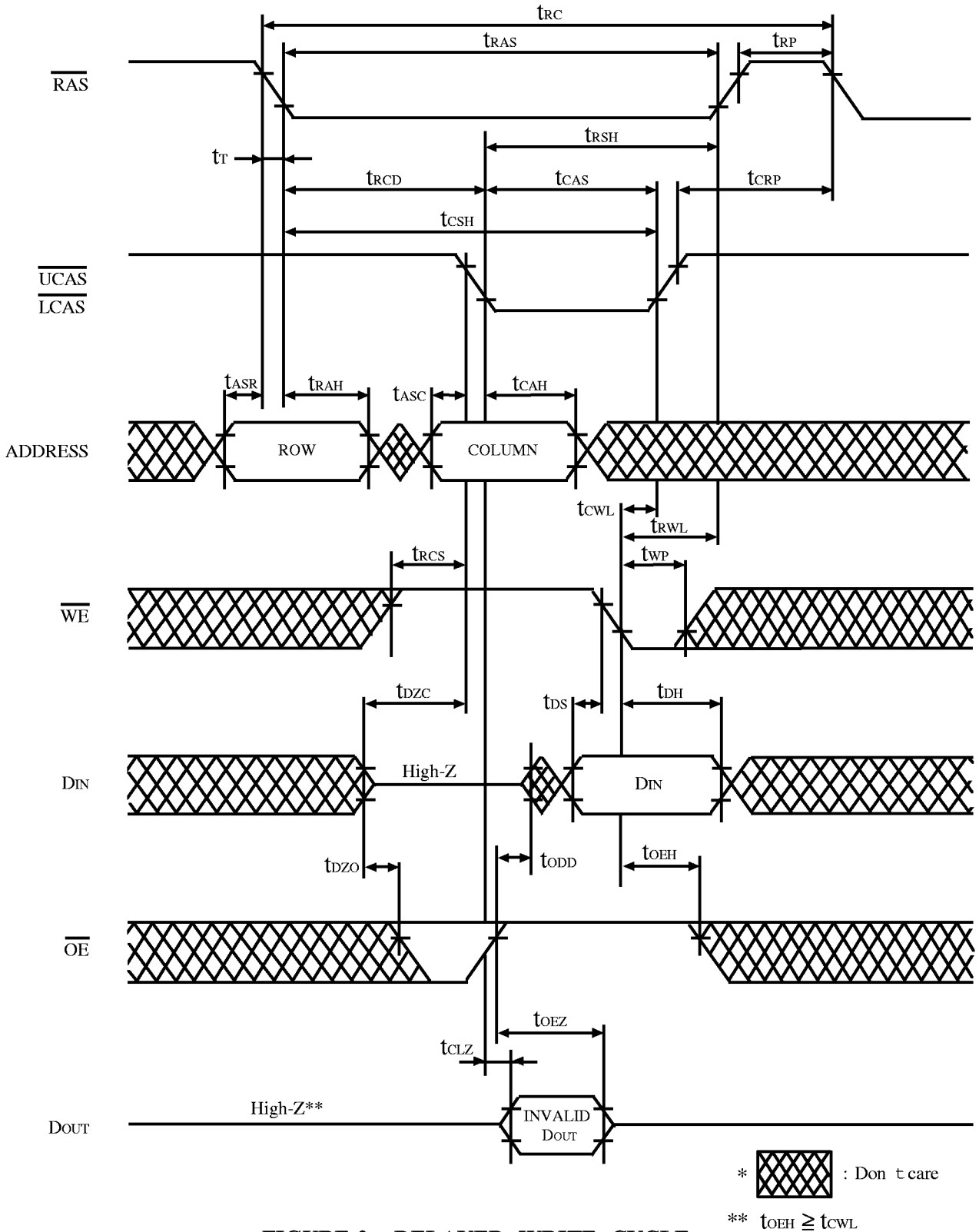


FIGURE 3. DELAYED WRITE CYCLE

*Note : In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device. After \overline{RAS} is reset, if $t_{OEH} > t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each I/O.

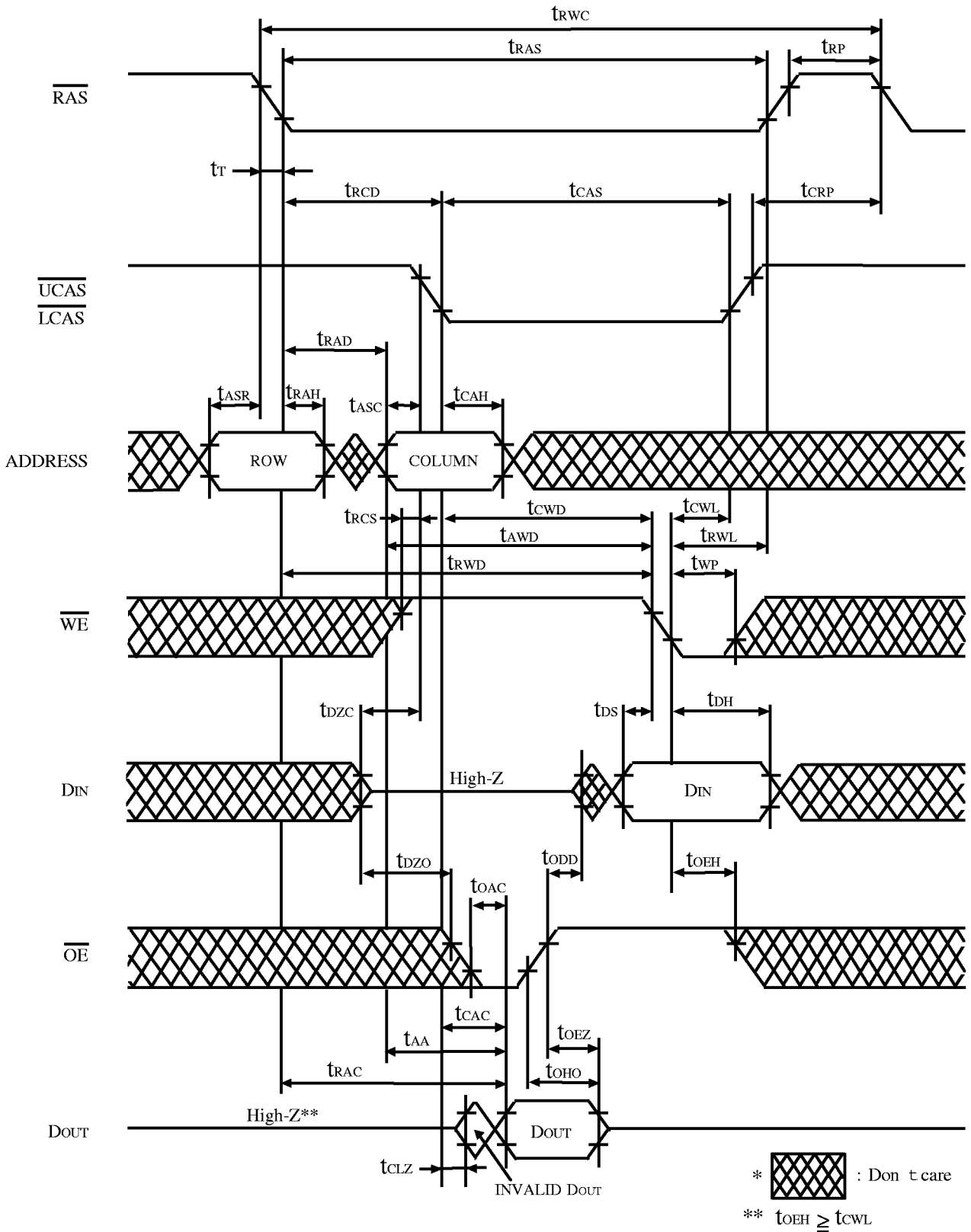


FIGURE 4. READ MODIFY WRITE CYCLE

*Note : In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device. After \overline{RAS} is reset, if $t_{toEH} \geq t_{tcWL}$, the I/O pin will remain open circuit (high impedance); if $t_{toEH} < t_{tcWL}$, invalid data will be out at each I/O.

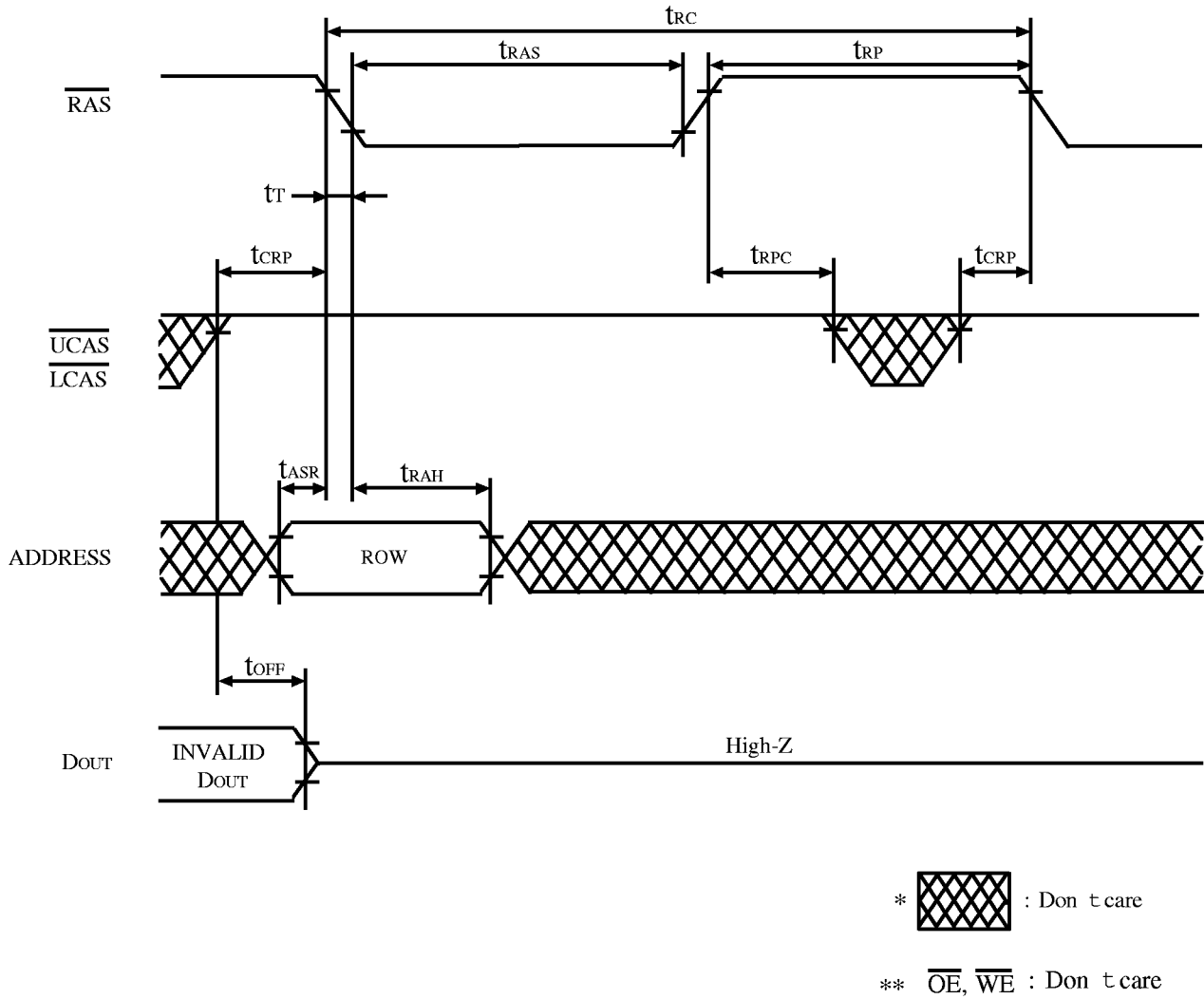


FIGURE 5. \overline{RAS} ONLY REFRESH CYCLE

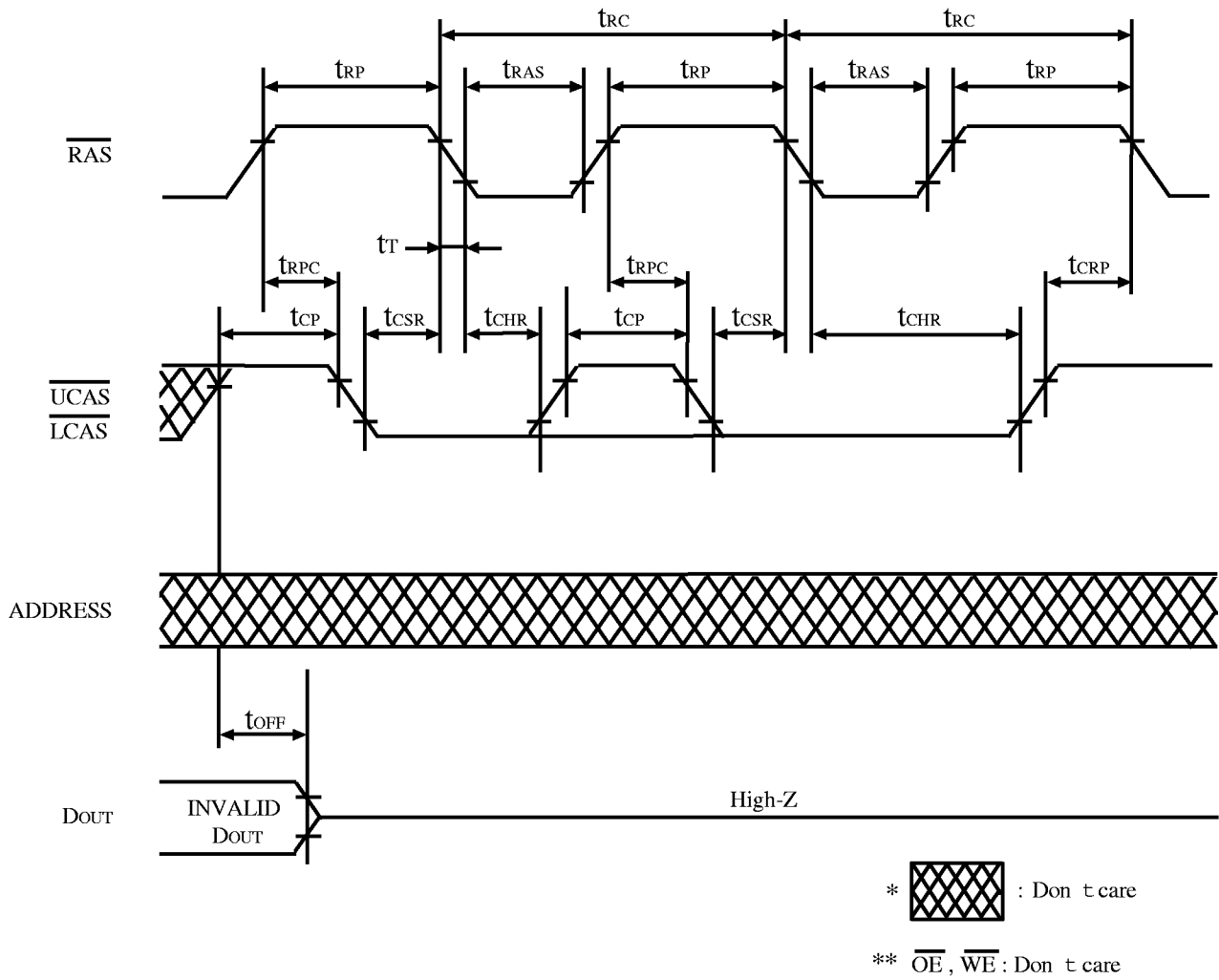


FIGURE 6. \overline{CAS} BEFORE \overline{RAS} REFRESH CYCLE

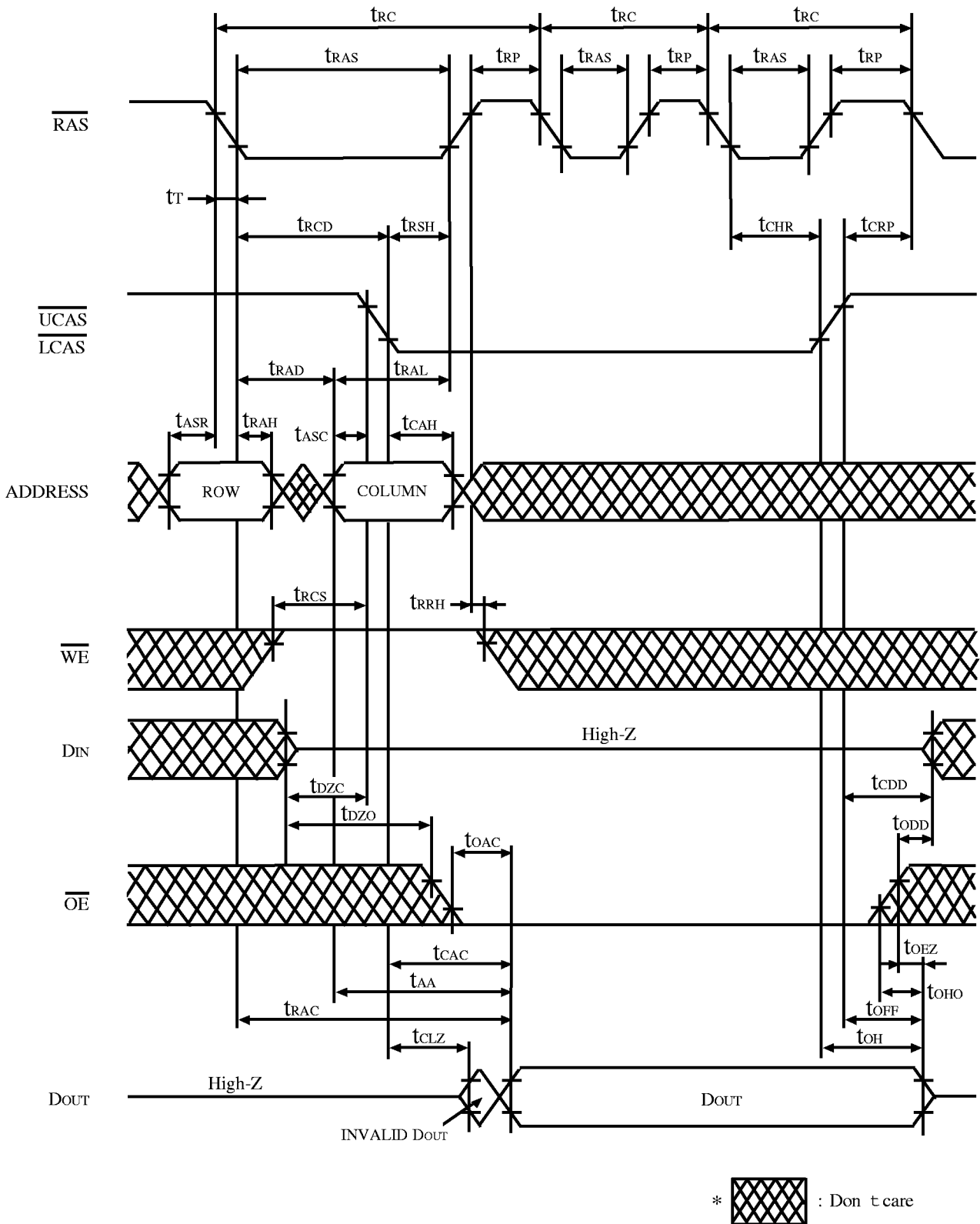


FIGURE 7. HIDDEN REFRESH CYCLE

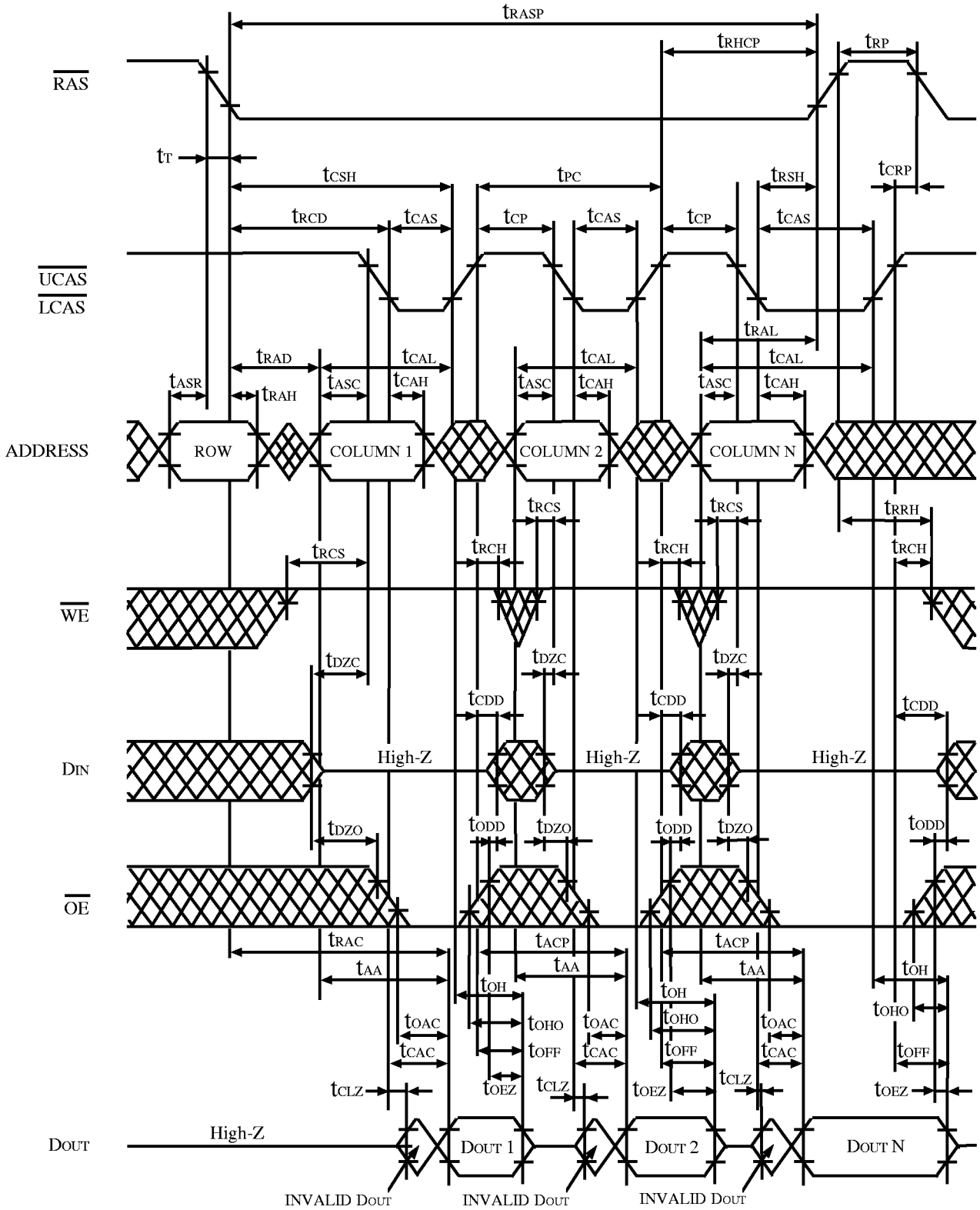
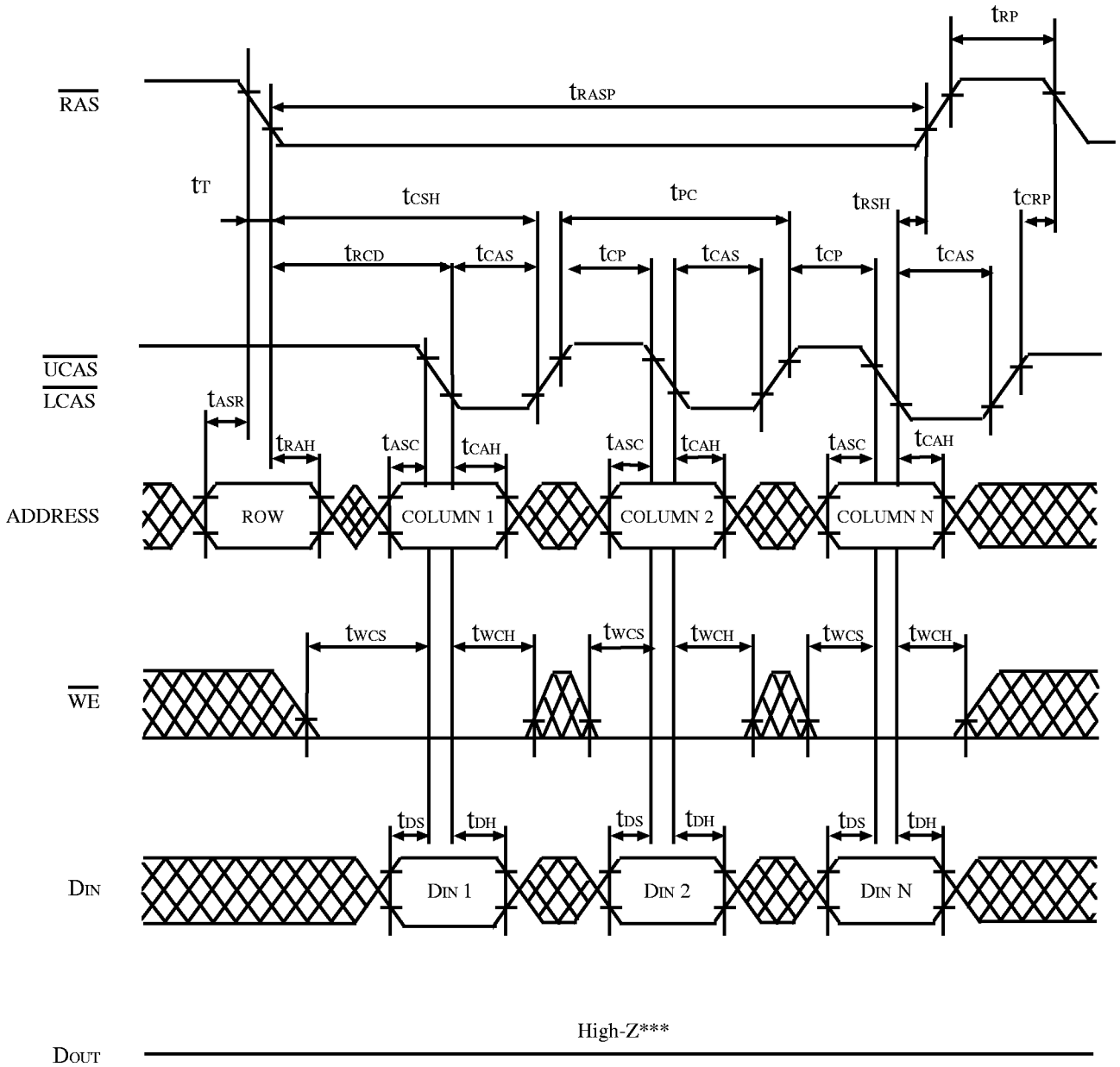


FIGURE 8. FAST PAGE MODE READ CYCLE




- *  : Don't care
- ** \overline{OE} : Don't care
- *** $t_{wcs} \geq t_{wcs}(\text{min})$

FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

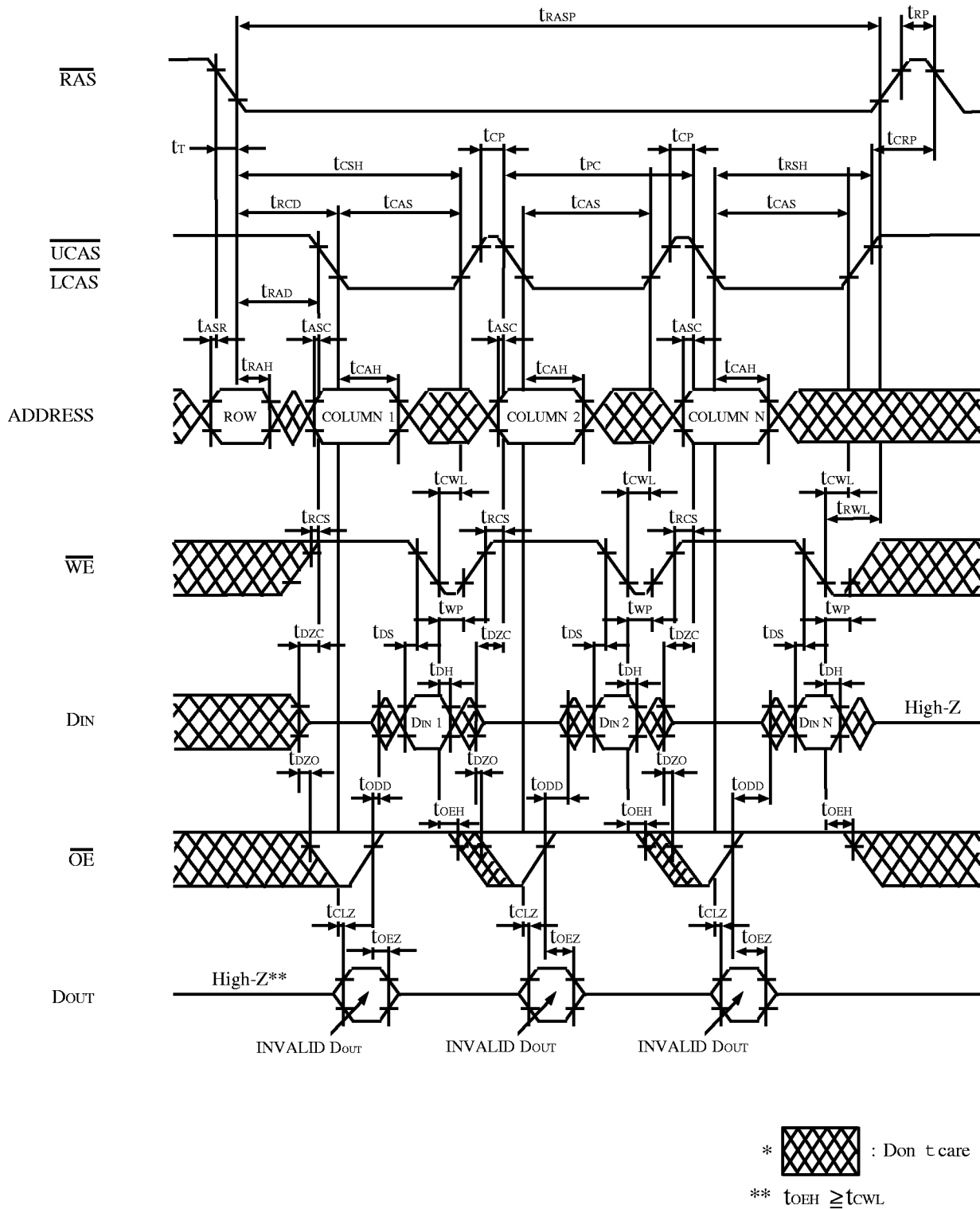


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

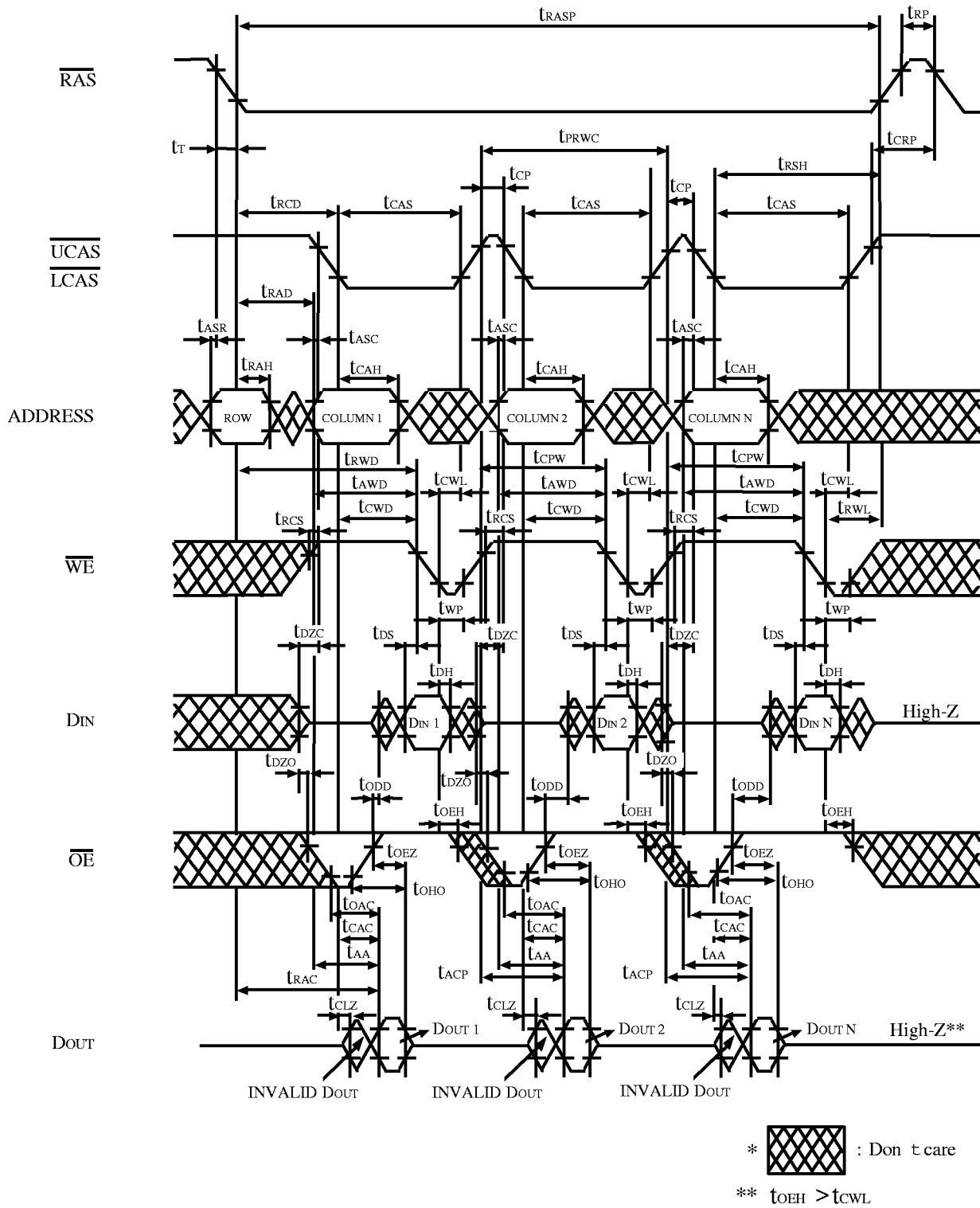
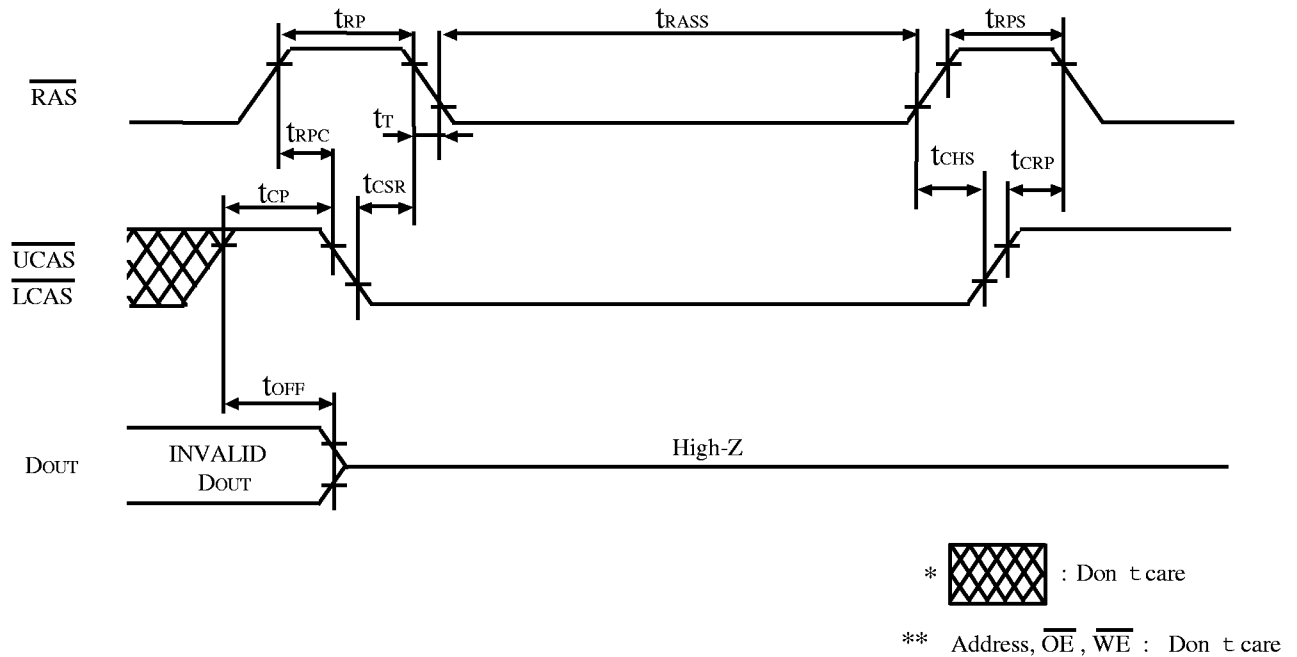


FIGURE 11. FAST PAGE MODE READ MODIFY WRITE CYCLE



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not t_{RASS} timing, $10\mu s \leq t_{RASS} \leq 100\mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
2. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 1024 or 4096 cycles of distributed CBR refresh with 15.6us interval should be executed within 16ms or 64ms immediately after exiting from and before entering into the self refresh mode.^{*1}
3. If you use distributed CBR refresh mode with 15.6us interval in normal read/write cycle, CBR refresh should be executed within 15.6us immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

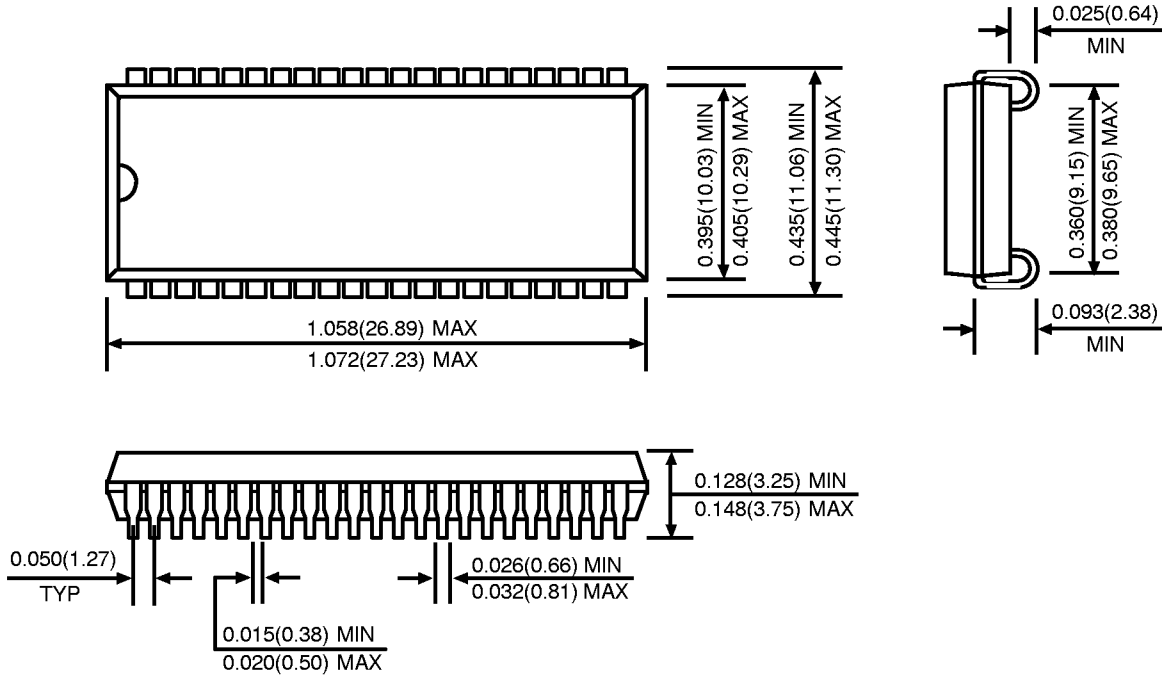
* Note 1 : GM71C(V)16160 (4096 Refresh Cycles / 64ms)
 GM71C(V)18160 (1024 Refresh Cycles / 16ms)

FIGURE 12. SELF-REFRESH CYCLE

Package Dimension

Unit: Inches (mm)

42 SOJ



44(50) TSOP I

