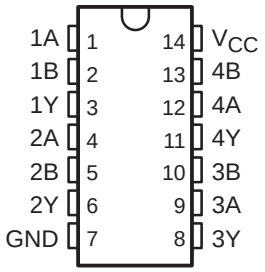
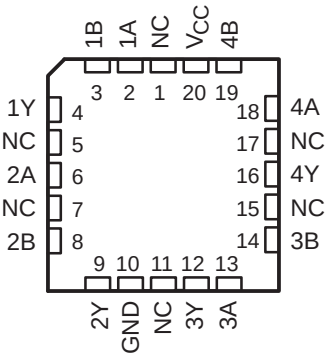
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as ’HC00**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC132 . . . J OR W PACKAGE
SN74HC132 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC132 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The ’HC132 perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

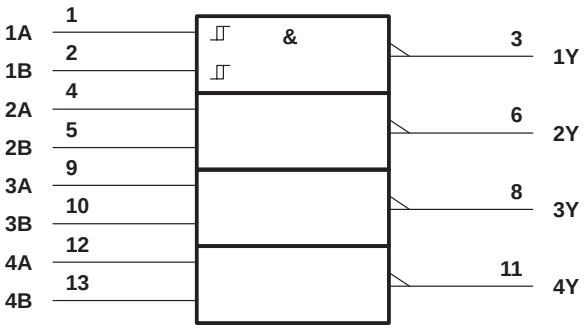
The SN54HC132 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC132 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

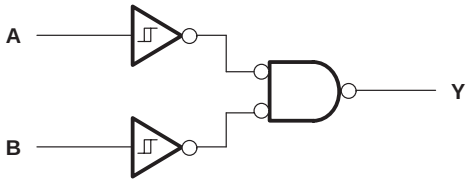
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC132			SN74HC132			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
$V_{T–}$			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} – V_{T–}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

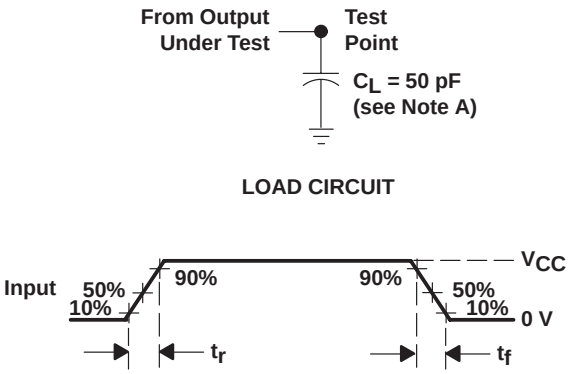
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	120		186		156	ns
			4.5 V		18	25		37		31	
			6 V		14	21		32		27	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

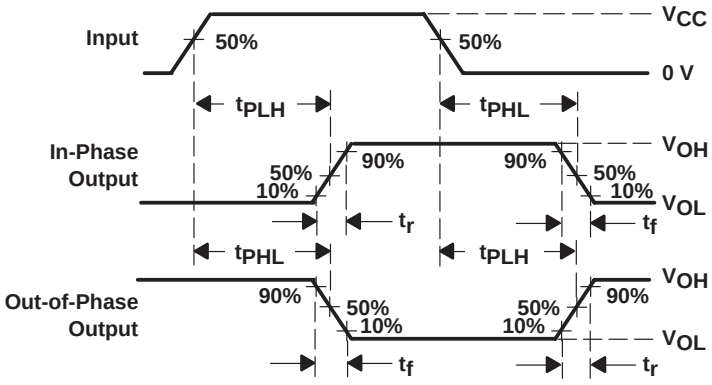
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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SN74HC132, Quadruple Positive-NAND Gates With Schmitt-Trigger Inputs

Device Status: Active

Parameter Name	SN74HC132
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	-4/4
No. of Gates	4
Static Current	0.02
tpd(max) (ns)	27

Description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'HC132 perform the Boolean function $Y = \overline{A \cdot B}$ or $\overline{\quad\quad}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC132 is characterized for operation from -40°C to 85°C.

Features

- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC00
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: scls034c.pdf (78 KB)
Full datasheet in Zipped PostScript: scls034c.psz (79 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
SN74HC132ADBLE	DB	14	-40 TO 85	OBSOLETE			
SN74HC132ADBR	DB	14	-40 TO 85	ACTIVE	0.70	2000	Check stock or order
SN74HC132APWR	PW	14	-40 TO 85	NRND	0.70	2000	Check stock or order
SN74HC132D	D	14	-40 TO 85	ACTIVE	0.74	50	Check stock or order
SN74HC132DBLE	DB	14	-40 TO 85	OBSOLETE			
SN74HC132DBR	DB	14	-40 TO 85	ACTIVE	0.62	2000	Check stock or order
SN74HC132DR	D	14	-40 TO 85	ACTIVE	0.65	2500	Check stock or order
SN74HC132N	N	14	-40 TO 85	ACTIVE	0.66	25	Check stock or order
SN74HC132PWLE	PW	14	-40 TO 85	OBSOLETE			
SN74HC132PWR	PW	14	-40 TO 85	ACTIVE	0.62	2000	Check stock or order

Application Reports

View Application Reports for Digital Logic

- CMOS Power Consumption And CPD Calculation (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (SDYA009C - Updated: 06/01/1997)
- HCMOS Design Considerations (SCLA007 - Updated: 04/01/1996)

- Implications Of Slow Or Floating CMOS Inputs (SCBA004C - Updated: 02/01/1998)
- Input And Output Characteristics Of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications And Restrictions (SCLA011 - Updated: 05/01/1996)
- Using High Speed CMOS And Advanced CMOS In Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

Related Documents

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 284 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

Table Data Updated on: 8/31/2000