32Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4•• CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V •• 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

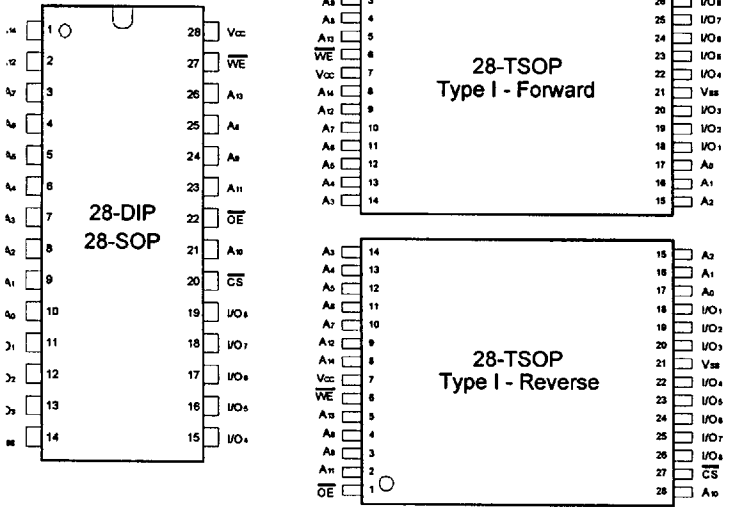
The KM62256D family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

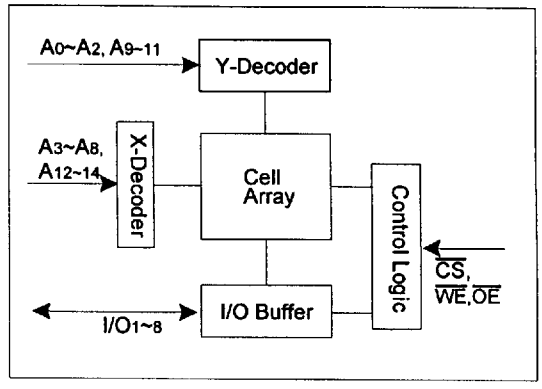
Product Family	Operating Temperature.	Speed (ns)	PKG Type	Power Dissipation	
				Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM62256DL KM62256DL-L	Commercial (0~70••)	45*/55/70ns	28-DIP,28-SOP 28-TSOP(I) R/F	50•• 10••	70mA
KM62256DLI KM62256DLI-L	Industrial (-40~85••)	70/100ns	28-SOP 28-TSOP(I) R/F	50•• 15••	

* The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



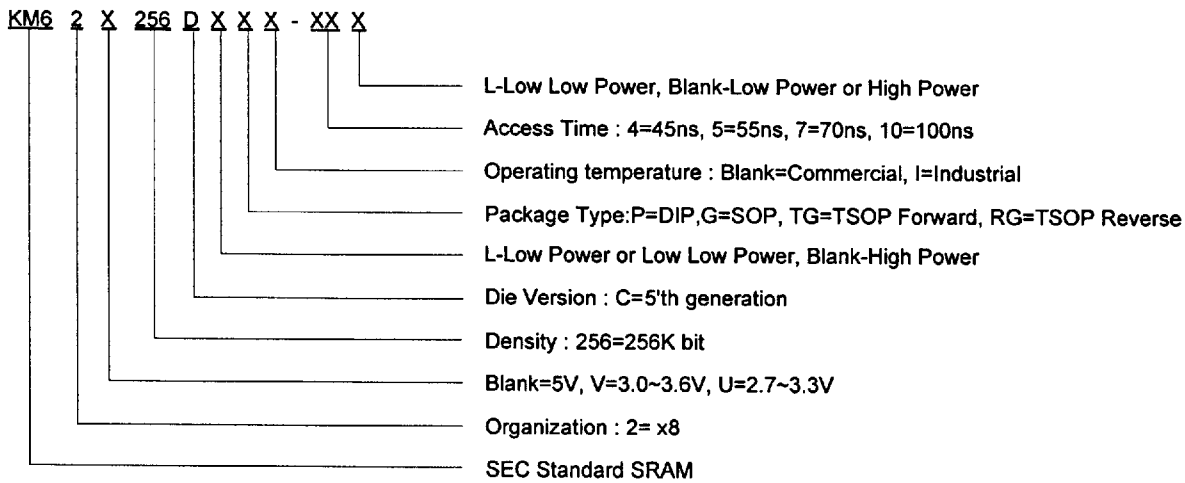
Pin Name	Function
A_0~A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70••)		Industrial Temp Products (-40~85••)	
Part Name	**Function**	**Part Name**	**Function**
KM62256DLP-4	28-DIP, 45ns, L-pwr	KM62256DLGI-7	28-SOP, 70ns, L-pwr
KM62256DLP-4L	28-DIP, 45ns, LL-pwr	KM62256DLGI-7L	28-SOP, 70ns, LL-pwr
KM62256DLP-5	28-DIP, 55ns, L-pwr	KM62256DLGI-10	28-SOP, 100ns, L-pwr
KM62256DLP-5L	28-DIP, 55ns, LL-pwr	KM62256DLGI-10L	28-SOP, 100ns, LL-pwr
KM62256DLP-7	28-DIP, 70ns, L-pwr	KM62256DLTGI-7	28-TSOP F, 70ns, L-pwr
KM62256DLP-7L	28-DIP, 70ns, LL-pwr	KM62256DLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256DLG-4	28-SOP, 45ns, L-pwr	KM62256DLTGI-10	28-TSOP F, 100ns, L-pwr
KM62256DLG-4L	28-SOP, 45ns, LL-pwr	KM62256DLTGI-10L	28-TSOP F, 100ns, LL-pwr
KM62256DLG-5	28-SOP, 50ns, L-pwr	KM62256DLRGI-7	28-TSOP R, 70ns, L-pwr
KM62256DLG-5L	28-SOP, 50ns, LL-pwr	KM62256DLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256DLG-7	28-SOP, 70ns, L-pwr	KM62256DLRGI-10	28-TSOP R, 100ns, L-pwr
KM62256DLG-7L	28-SOP, 70ns, LL-pwr	KM62256DLRGI-10L	28-TSOP R, 100ns, LL-pwr
KM62256DLTG-4	28-TSOP F, 45ns, L-pwr		
KM62256DLTG-4L	28-TSOP F, 45ns, LL-pwr		
KM62256DLTG-5	28-TSOP F, 55ns, L-pwr		
KM62256DLTG-5L	28-TSOP F, 55ns, LL-pwr		
KM62256DLTG-7	28-TSOP F, 70ns, L-pwr		
KM62256DLTG-7L	28-TSOP F, 70ns, LL-pwr		
KM62256DLRG-4	28-TSOP R, 45ns, L-pwr		
KM62256DLRG-4L	28-TSOP R, 45ns, LL-pwr		
KM62256DLRG-5	28-TSOP R, 55ns, L-pwr		
KM62256DLRG-5L	28-TSOP R, 55ns, LL-pwr		
KM62256DLRG-7	28-TSOP R, 70ns, L-pwr		
KM62256DLRG-7L	28-TSOP R, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	••	-
Operating Temperature	T_A	0 to 70	••	KM62256DL/L-L
		-40 to 85	••	KM62256DLI/LI-L
Soldering temperature and time	T_{SOLDER}	260••, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a str ss rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not im lied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70••, unless otherwise specified
2) Industrial Product : T_A=-40 to 85••, unless otherwise specified
** TA=25••
*** V_{IL}(min)=-3.0V for •• 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25••)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	••
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, V_{IO}-Vss to Vcc		-1	-	1	••
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	7	10	mA
				Write		-	25	
Average operating current		I_{CC1}	1•• Cycle 100% duty, I_{IO}=0mA, $\overline{CS_1}$•• 0.2V, CS_2 •• Vcc -0.2V	Read	-	5	10	mA
				Write		-	25	
		I_{CC2}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}/Min cycle, 100% duty I_{IO}=0mA		-	-	70	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IH}		-	-	1	mA
Standby Current (CMOS)	KM62256DL KM62256DL-L	I_{SB1}	$\overline{CS_1}$ •• Vcc-0.2V CS_2 •• Vcc-0.2V or CS_2 •• 0.2V Other Inputs=0~Vcc	Low Power Low Low Power	- -	2 1	50 10	••
	KM62256DLI KM62256DLI-L			Low Power Low Low Power	- -	- -	50 15	••

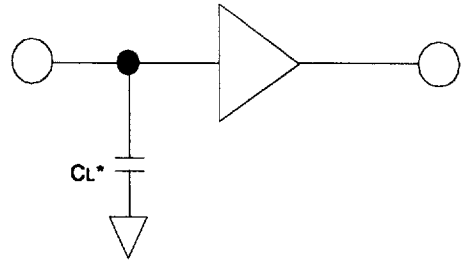
* 1) Commercial Product : T_A=0 to 70••, unless otherwise specified
2) Industrial Product : T_A=-40 to 85••, unless otherwise specified
** T_A=25••

A.C CHARACTERISTICS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference) *

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	-

* See DC Operating conditions
** Test load for 45ns commercial products



* Including scope and jig capacitance

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62256DL/L-L	0~70••	5V •• 10%	45*/55/70ns	Commercial
KM62256DLI/LI-L	-40~85••	5V •• 10%	70/100ns	Industrial

* The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	30	0	35	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	30	0	35	ns
	Output hold from address change	tOH	5	-	5	-	5	-	5	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	35	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	10	-	ns

* The parameter is measured with 30pF test load

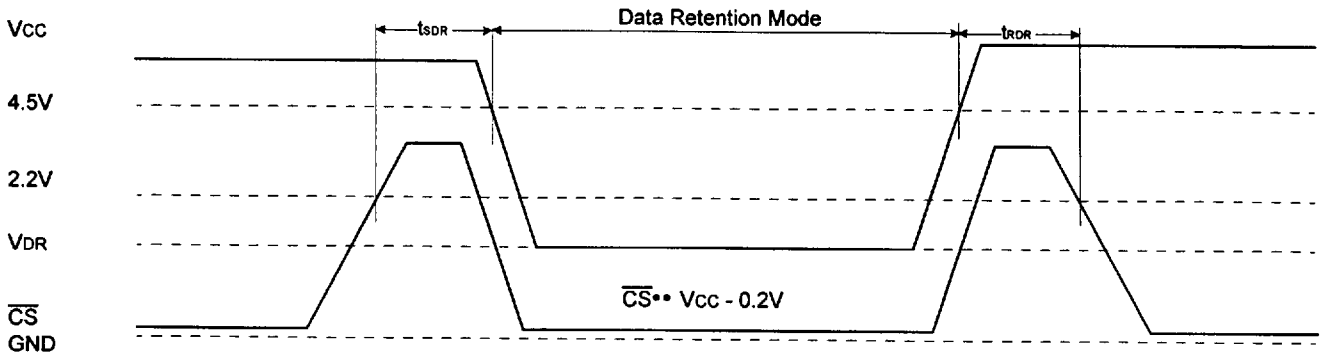
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS}$•• Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM62256DL KM62256DL-L	Vcc=3.0V $\overline{CS}$•• Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	30 10	••
		KM62256DLI KM62256DLI-L		L-Ver LL-Ver	- -	- -	30 15	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 ••, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 ••, unless otherwise specified
** T_A=25••

DATA RETENTION WAVE FORM

1) $\overline{CS}$ Controlled



FUNCTIONAL DESCRIPTION

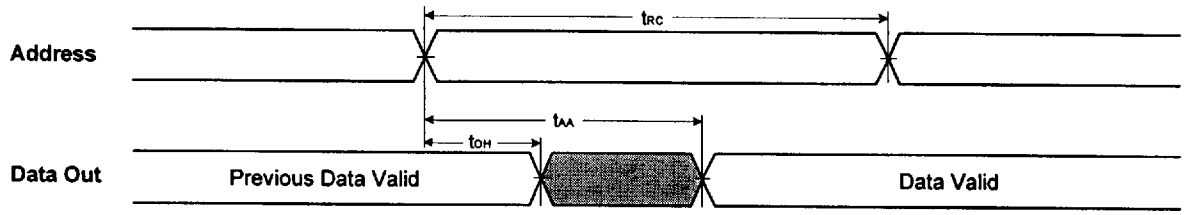
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	I_{SB} I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	Dout	I_{CC}
L	L	X	Write	Din	I_{CC}

* X means don't care

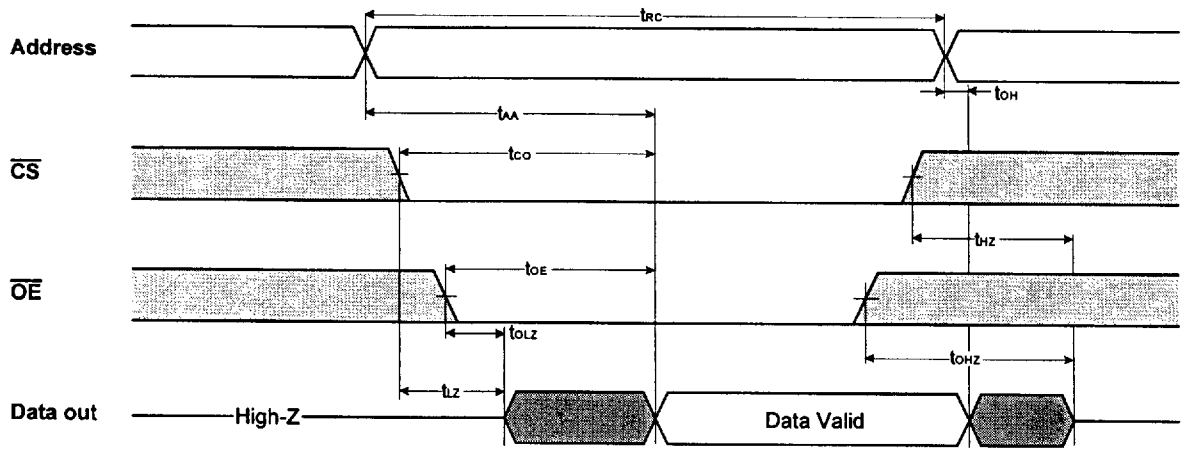
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



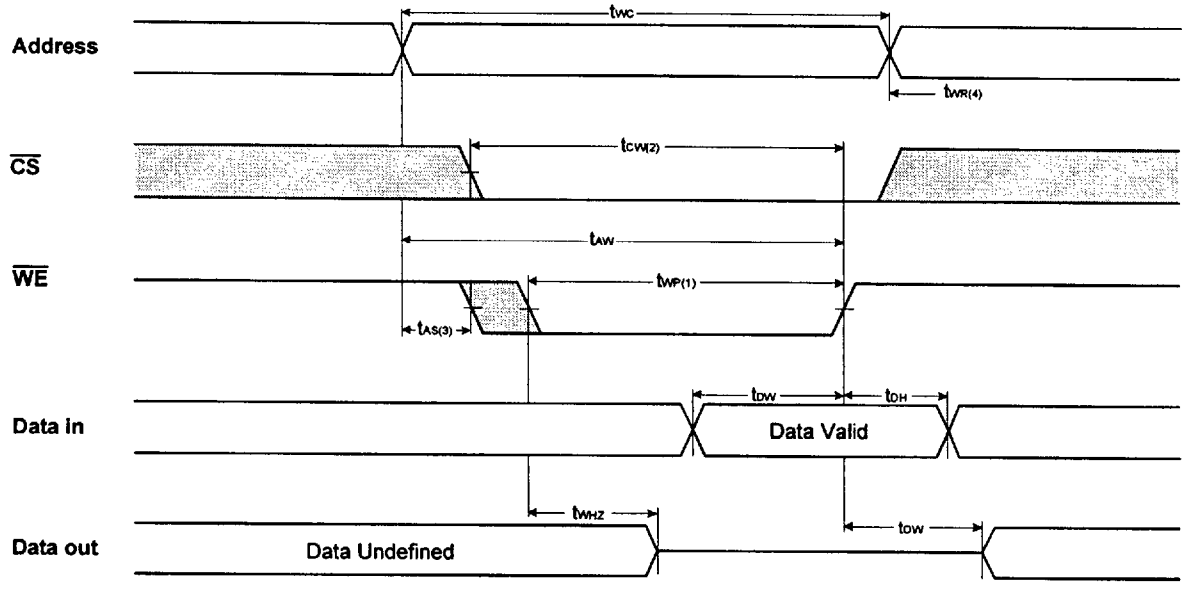
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



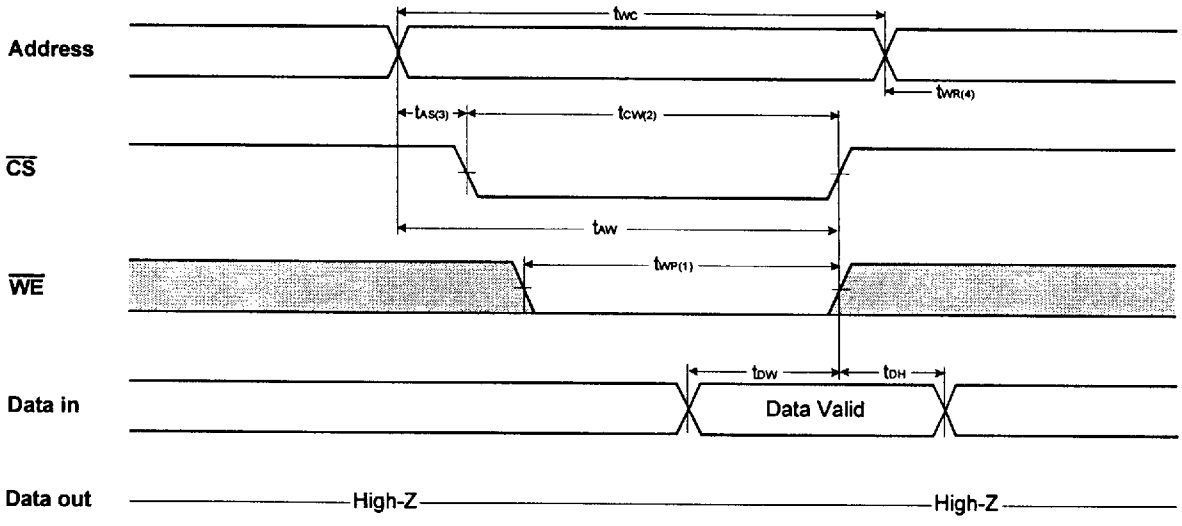
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage lev Is.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to evice.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



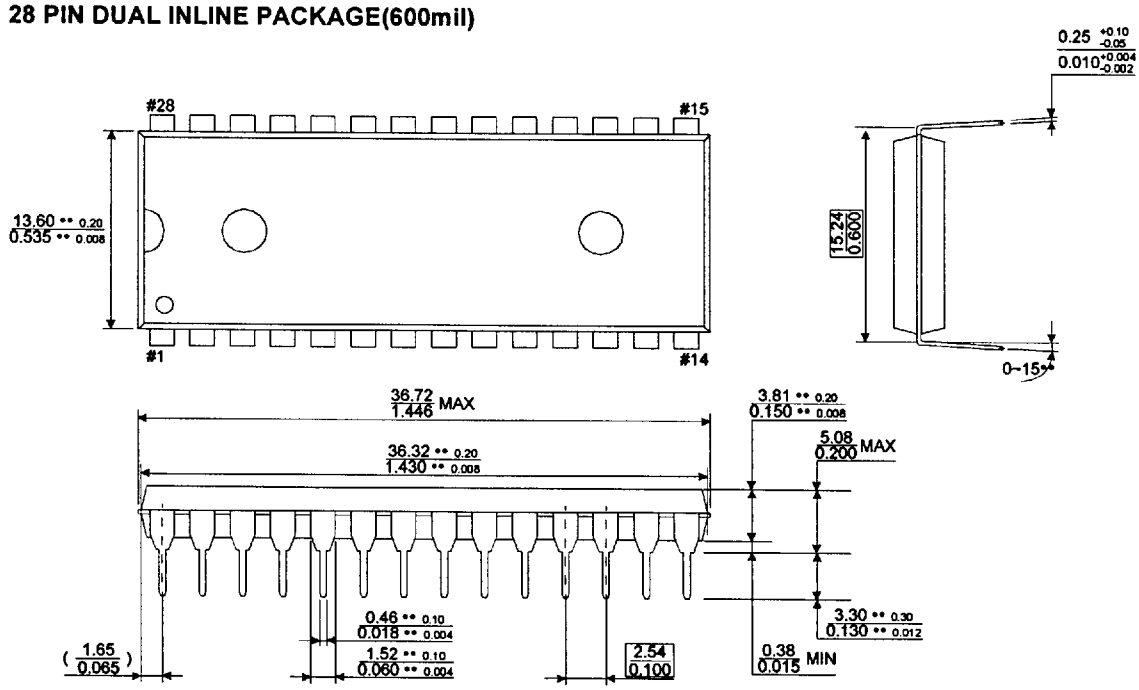
NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ goes low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

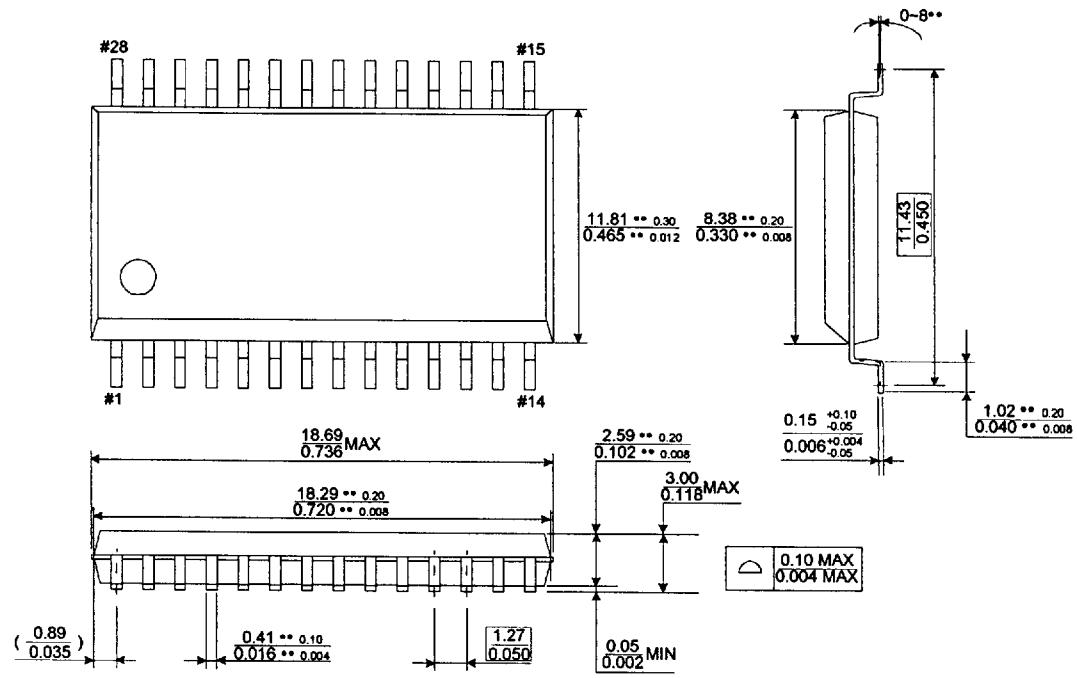
PACKAGE DIMENSIONS

Units :Millimeters(Inches)

28 PIN DUAL INLINE PACKAGE(600mil)



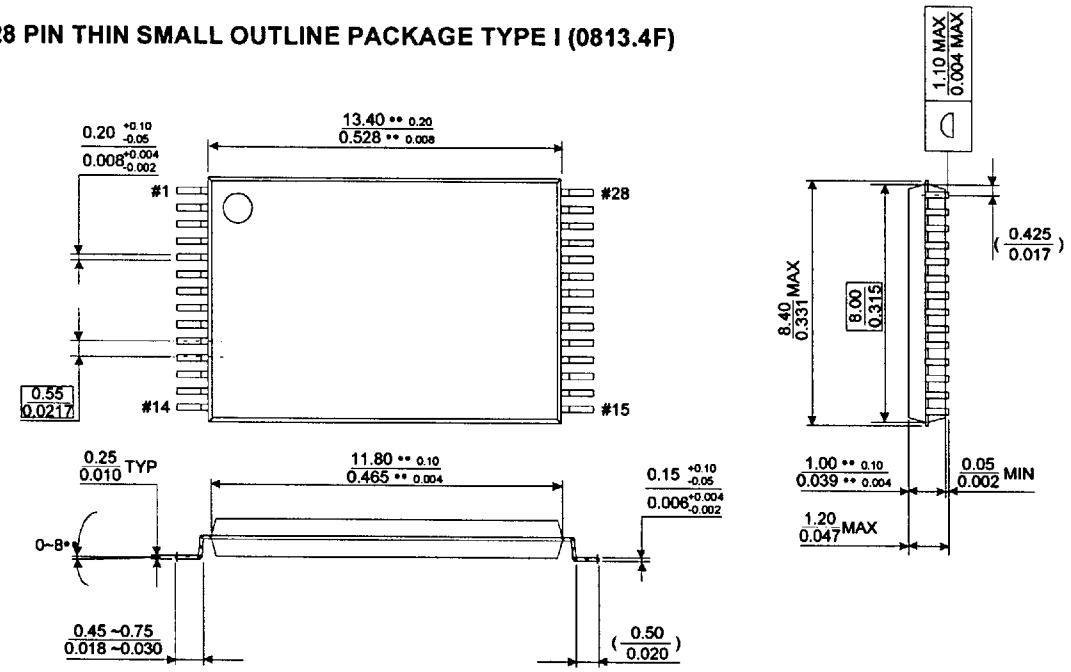
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units :Millimeters(Inches)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)