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SPA2318Z

1700MHz to 2200MHz 1 WATT POWER AMP WITH ACTIVE BIAS

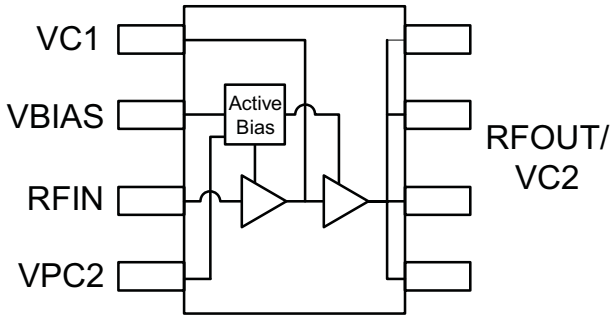
Package: Exposed Pad SOIC-8

Product Description

RFMD's SPA2318Z is a high efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot. This product is specifically designed for use as a driver amplifier for infrastructure equipment in the 1960MHz and 2140MHz bands. Its high linearity makes it an ideal choice for multi-carrier and digital applications. The matte tin finish on the lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide or halogenated fire retardants.

Optimum Technology Matching® Applied

- ✓ GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- RF MEMS



Features

- High Linearity Performance: +21dBm IS-95 Channel Power at -55dBc ACP; +20.7dBm WCDMA Channel Power at -50dBc ACP; +47dBm Typ. OIP_3
- On-Chip Active Bias Control
- High Gain: 24dB Typ. at 1960MHz
- Patented High Reliability GaAs HBT Technology
- Surface-Mountable Plastic Package

Applications

- WCDMA Systems
- PCS Systems
- Multi-Carrier Applications

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency of Operation	1700		2200	MHz	
Output Power at 1dB Compression [1]		29.5		dBm	1960MHz
		29.5		dBm	2140MHz
Adjacent Channel Power [1]		-55.0		dBc	1960MHz, IS-95 at P_{OUT}=21.0dBm, WCDMA at P_{OUT}=20.7dBm
		-50.0	-47.0	dBc	2140MHz
Small Signal Gain [1,2]		24.0		dB	1960MHz
	21.0	23.5	24.5	dB	2140MHz
Input VSWR [1,2]		1.6:1			1960MHz
		1.6:1			2140MHz
Output Third Order Intercept Point [2]		46.5		dBm	1960MHz, Power out per tone=+14dBm
		47.0		dBm	2140MHz
Noise Figure [1,2]		5.5		dB	1960MHz
		5.5		dB	2140MHz
Device Current [1,2]	360	400	425	mA	I_{BIAS}=10mA, I_{C1}=70mA, I_{C2}=320mA
Device Voltage [1,2]	4.75	5.0	5.25	V	
Thermal Resistance (Junction - Lead)		31		°C/W	T_L=85°C

Test Conditions: Z_0=50Ω Temp=25°C V_{CC}=5.0V [1] Optimal ACP tune [2] Optimal IP_3 tune

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Absolute Maximum Ratings

Parameter	Rating	Unit
Max Supply Current (I_{C1}) at V_{CC} typ.	150	mA
Max Supply Current (I_{C2}) at V_{CC} typ.	750	mA
Max Device Voltage (V_{CC}) at I_{CC} typ.	6.0	V
Max RF Input Power	16	dBm
Max Junction Temp (T_J)	+160	°C
Max Storage Temp	+150	°C
Moisture Sensitivity Level	3	MSL

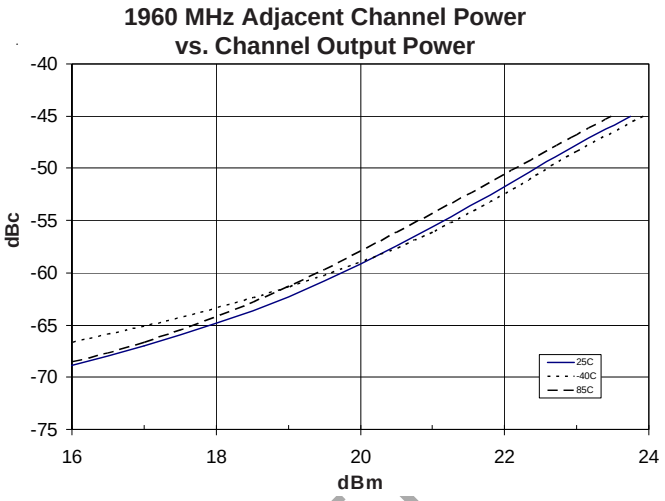
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.
Bias Conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L)/R_{TH}$, j-l

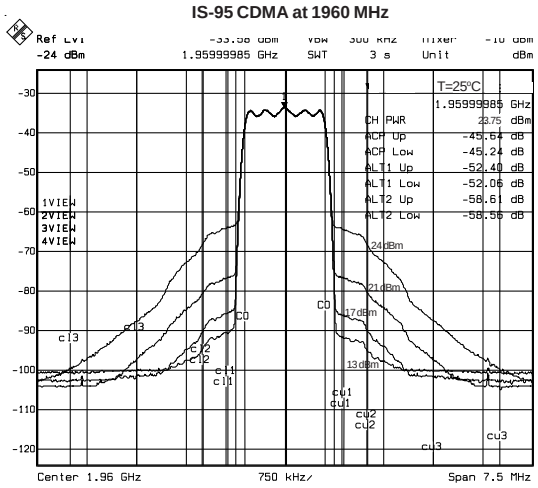
Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

ACP Optimized 1960MHz Application Circuit Data, I_{CC}=400mA, V_{CC}=5V IS-95, 9 Channels Forward





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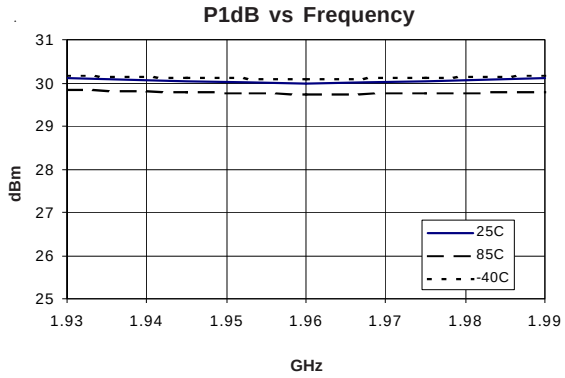
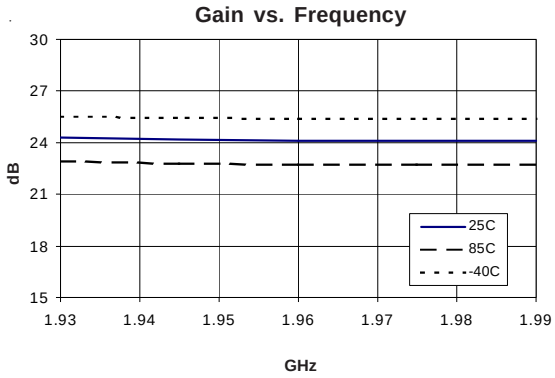
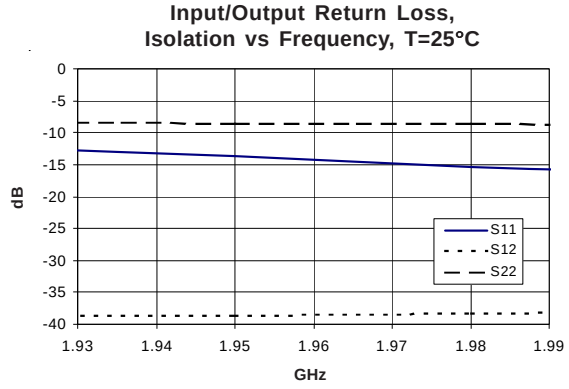
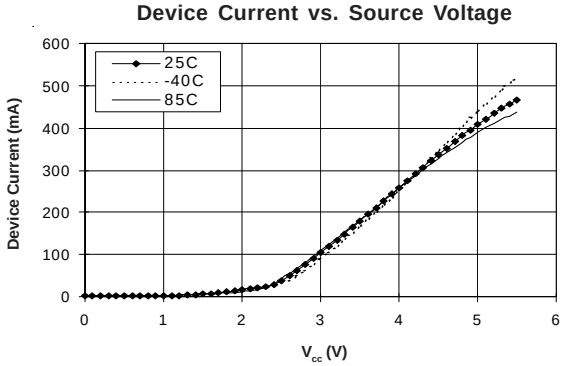


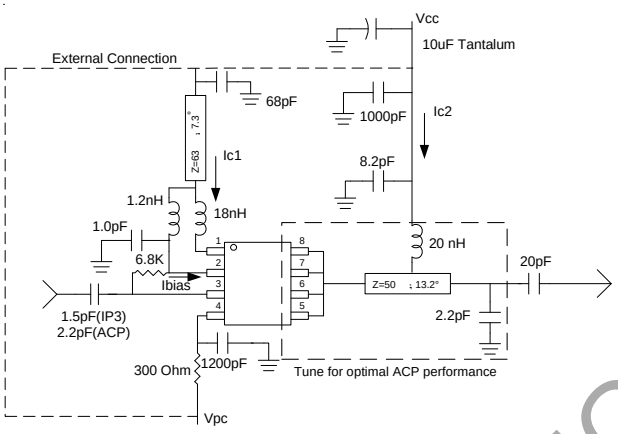


ACP Optimized 1960MHz Application Circuit Data, I_{CC}=400mA, V_{CC}=5V

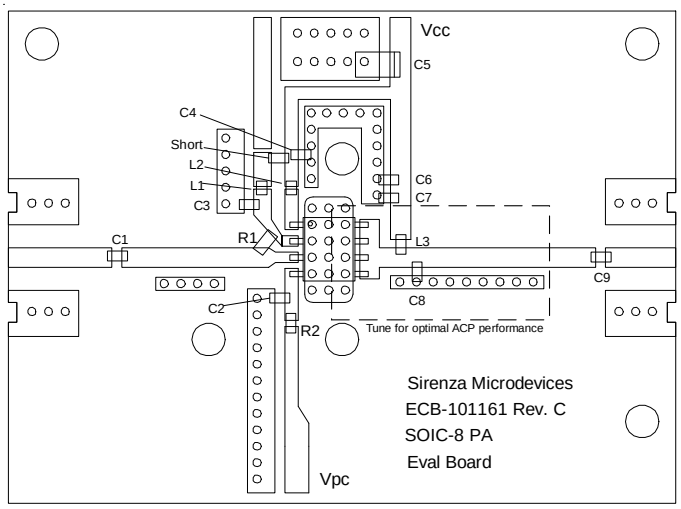




1930MHz to 1990MHz Application Schematic



1930MHz to 1990MHz Evaluation Board Layout and Bill of Materials



Ref. Des.	Value	Part Number
C1	1.5pF, ±0.25pF (IP3) 2.2pF, ±0.25pF (ACP)	Rohm MCH18 series
C2	1200pF, 5%	Rohm MCH18 series
C3	1.0pF, ±0.25pF	Rohm MCH18 series
C4	68pF, 5%	Rohm MCH18 series
C5	10uF, 10%	AVX TAJB106K020R
C6	1000pF, 5%	Rohm MCH18 series
C7	8.2pF, ±0.5pF	Rohm MCH18 series
C8	2.2pF, ±0.25pF	Rohm MCH18 series
C9	20pF, 5%	Rohm MCH18 series
L1	1.2nH, ±0.3nH	Toko LL1608-FS series
L2	18nH, 5%	Toko LL1608-FS series
L3	20nH, 5%	Coilcraft HQ 0805 series
R1	6.8K Ohm, 5%	Rohm MCR03 series
R2	300 Ohm, 5%	Rohm MCR03 series

ACP Optimized 2140MHz Application Circuit Data, I_{CC}=400mA, V_{CC}=5V IS-95, WCDMA setup is

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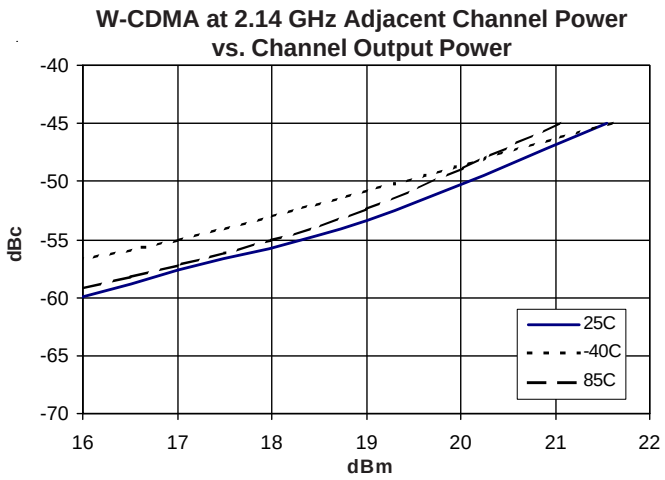
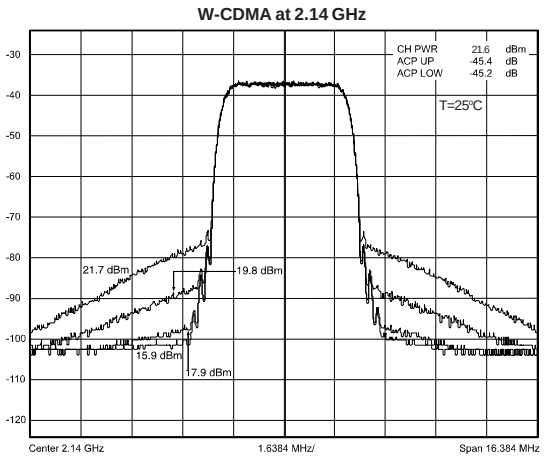
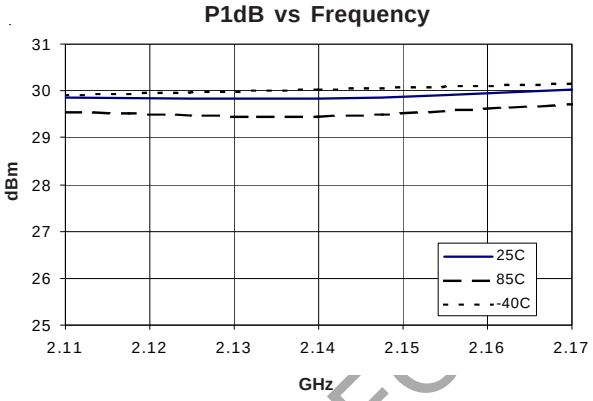
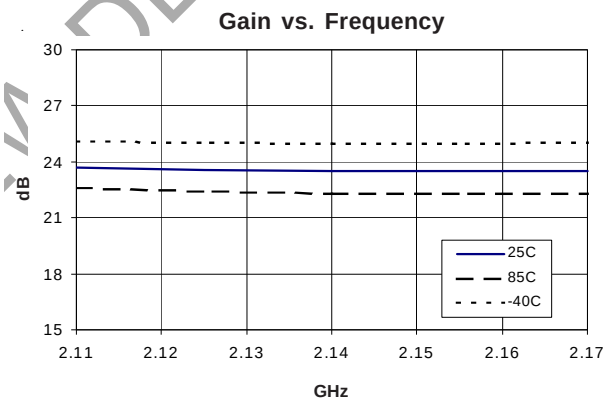
PCCPCH+PSCH+SSCH+CPICH+PICH+64DPCH, 10.5dB peak to average at 0.001% probability

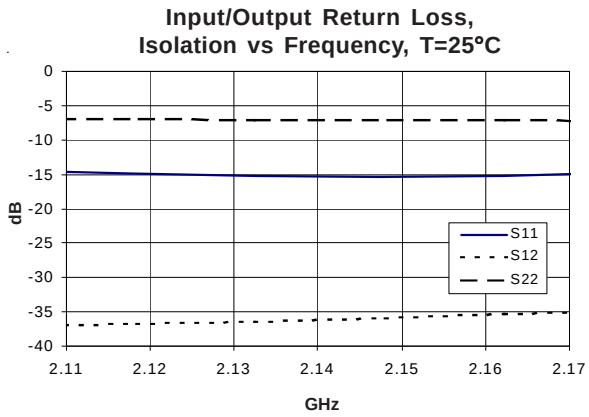


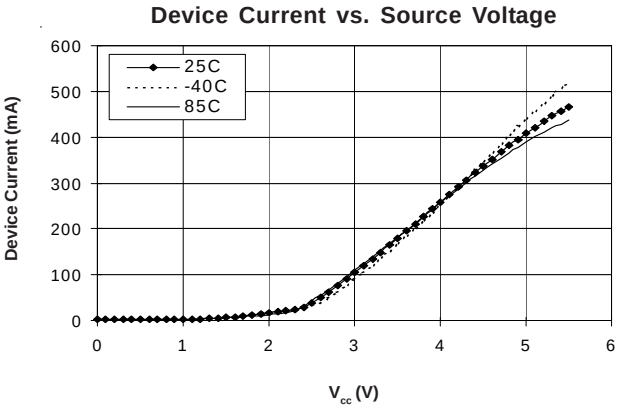


ACP Optimized at 2140MHz Application Circuit Data, I_{CC}=400mA, V_{CC}=5V

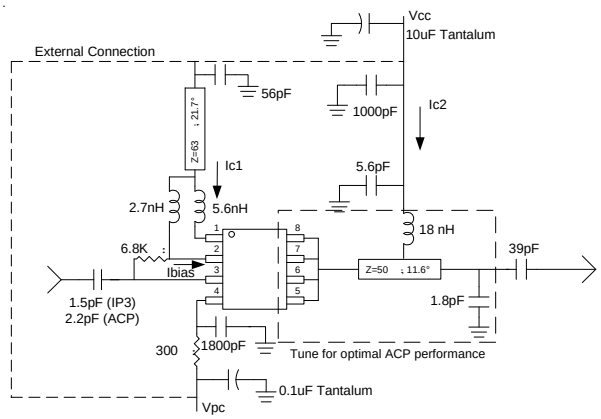




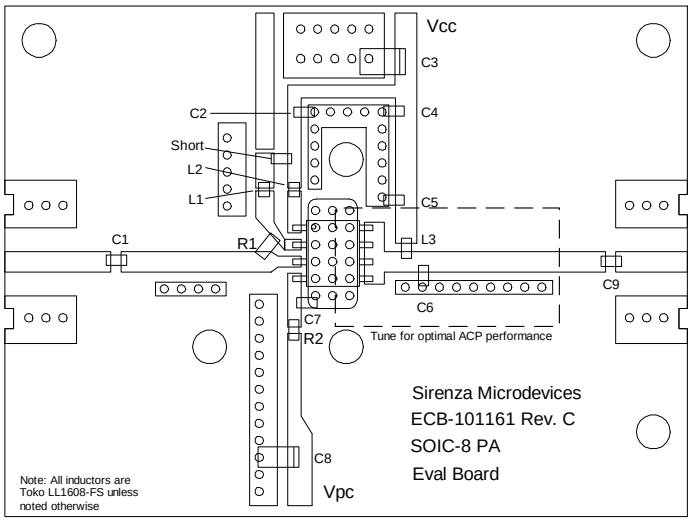




2110MHz to 2170MHz Application Schematic



2110MHz to 2170MHz Evaluation Board Layout and Bill of Materials



Ref. Des.	Value	Part Number
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C2	56pF, 5%	Rohm MCH18 series
C3	10uF, 10%	AVX TAJB106K020R
C4	1000pF, 5%	Rohm MCH18 series
C5	5.6pF, ±0.5pF	Rohm MCH18 series
C6	1.8pF, ±0.25pF	Rohm MCH18 series
C7	1800pF, 5%	Rohm MCH18 series
C8	0.1uF, 10%	Matsuo 267M3502104K
C9	39pF, 5%	Rohm MCH18 series
L1	2.7nH, ±0.3nH	Toko LL1608-FS series
L2	5.6nH, ±0.3nH	Toko LL1608-FS series
L3	18nH, 5%	Toko LL1608-FS series
R1	6.8K Ohm, 5%	Rohm MCR03 series
R2	300 Ohm, 5%	Rohm MCR03 series

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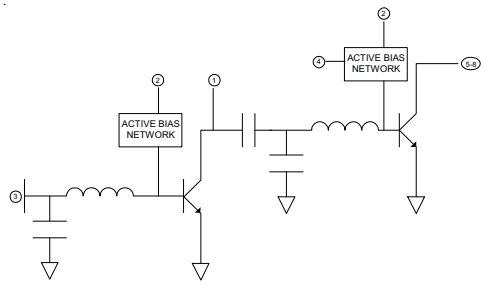
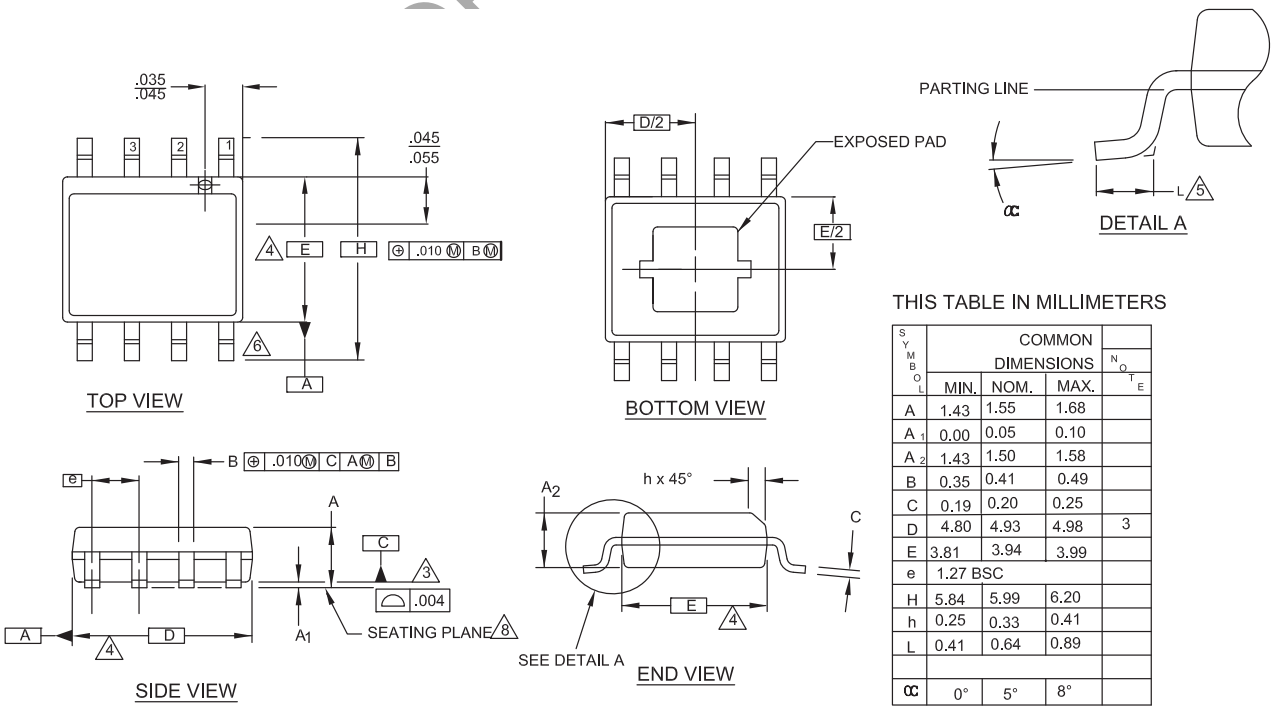
Pin	Function	Description
1	VC1	VC1 is the supply voltage for the first stage transistor. The configuration as shown on the Application Schematic is required for optimum RF performance.
2	VBIAS	VBias is the bias control pin for the active bias network. Recommended configuration is shown in the Application Schematic.
3	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the Application Schematic.
4	VPC2	VPC2 is the bias control pin for the active bias network for the second stage. The recommended configuration is shown in the Application Schematic.
5, 6, 7, 8	RF OUT / VC2	RF output and bias pins. Bias should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see Application Schematic). The supply side of the bias network should be well bypassed. An output matching network is necessary for optimum performance.
EPAD	GND	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern.

Simplified Device Schematic



Package Drawing

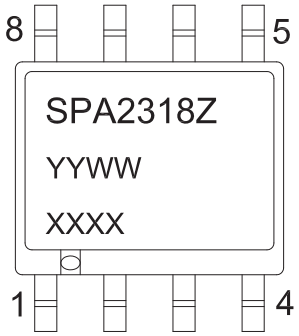
Dimensions in inches (millimeters)
Refer to drawing posted at www.rfmd.com for tolerances.



THIS TABLE IN MILLIMETERS

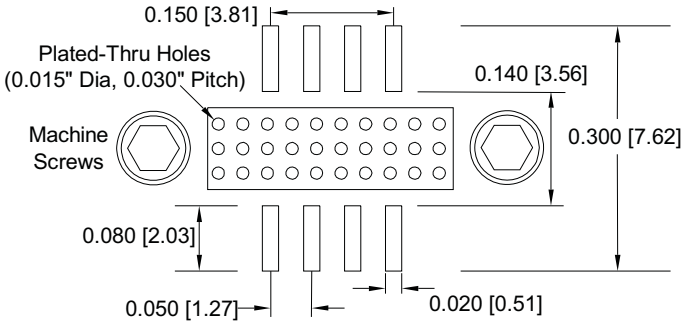
SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	1.43	1.55	1.68	
A_1	0.00	0.05	0.10	
A_2	1.43	1.50	1.58	
B	0.35	0.41	0.49	
C	0.19	0.20	0.25	
D	4.80	4.93	4.98	3
E	3.81	3.94	3.99	
e	1.27 BSC			
H	5.84	5.99	6.20	
h	0.25	0.33	0.41	
L	0.41	0.64	0.89	
α	0°	5°	8°	

Branding Diagram



YYWW = DateCode
XXXX = TraceCode assigned by Subcon

Recommended Land Pattern



Ordering Information

Ordering Code	Description
SPA2318Z	7” Reel with 500 pieces
SPA2318ZSQ	Sample bag with 25 pieces
SPA2318ZSR	7” Reel with 100 pieces
SPA2318Z-EVB1	1960MHz PCBA
SPA2318Z-EVB2	2140MHz PCBA

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