

Data sheet	
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# BSP225

## P-channel enhancement mode vertical D-MOS transistor

### FEATURES

- Low  $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

### DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

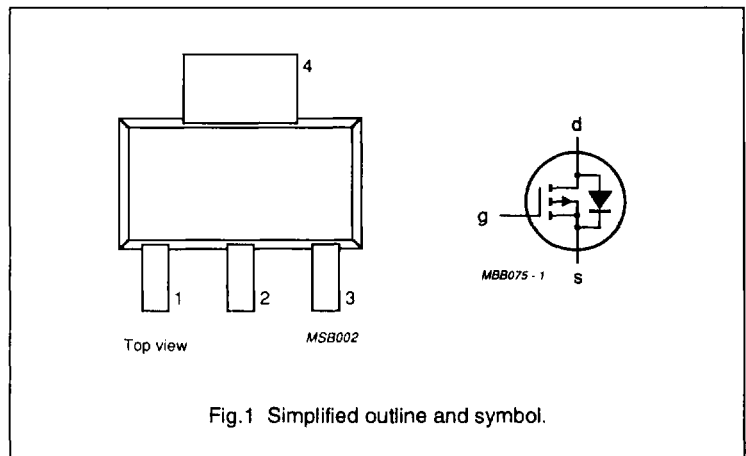
### PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200 \text{ mA}$ $-V_{GS} = 10 \text{ V}$	15	$\Omega$
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1 \text{ mA}$ $V_{GS} = V_{DS}$	2.8	V

### PIN CONFIGURATION



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### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ °C}$ (note 1)	–	1.5	W
$T_{stg}$	storage temperature range		–65	150	°C
$T_j$	junction temperature		–	150	°C

### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

### THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3	K/W

### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm<sup>2</sup>.

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### CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D = 10\text{ }\mu\text{A}$ $V_{GS} = 0$	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 200\text{ V}$ $V_{GS} = 0$	–	–	1	$\mu\text{A}$
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20\text{ V}$	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1\text{ mA}$ $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200\text{ mA}$ $-V_{GS} = 10\text{ V}$	–	10	15	$\Omega$
$ y_{fs} $	transfer admittance	$-I_D = 200\text{ mA}$ $-V_{DS} = 25\text{ V}$	100	200	–	mS
$C_{iss}$	input capacitance	$-V_{DS} = 25\text{ V}$ $-V_{GS} = 0$ $f = 1\text{ MHz}$	–	65	90	pF
$C_{oss}$	output capacitance	$-V_{DS} = 25\text{ V}$ $-V_{GS} = 0$ $f = 1\text{ MHz}$	–	20	30	pF
$C_{rss}$	feedback capacitance	$-V_{DS} = 25\text{ V}$ $-V_{GS} = 0$ $f = 1\text{ MHz}$	–	6	15	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$-I_D = 250\text{ mA}$ $-V_{DD} = 50\text{ V}$ $-V_{GS} = 0\text{ to }10\text{ V}$	–	5	10	ns
$t_{off}$	turn-off time	$-I_D = 250\text{ mA}$ $-V_{DD} = 50\text{ V}$ $-V_{GS} = 0\text{ to }10\text{ V}$	–	20	30	ns

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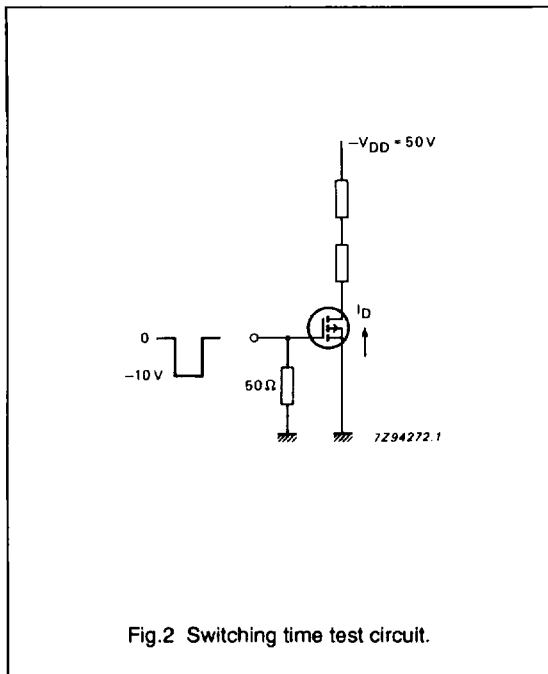


Fig.2 Switching time test circuit.

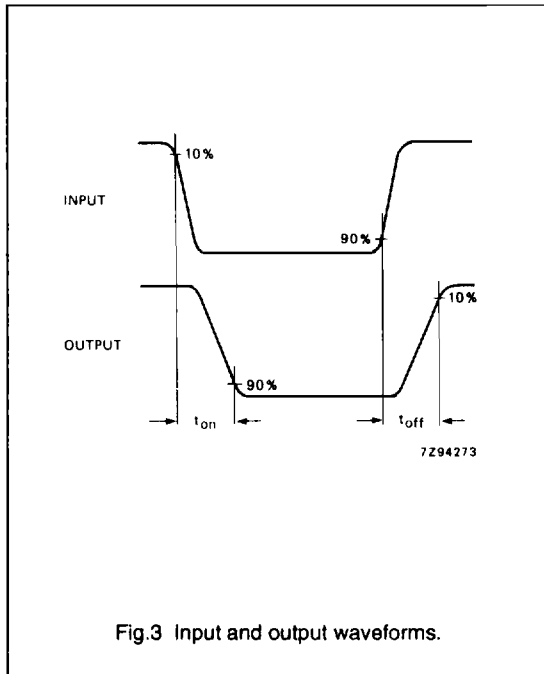


Fig.3 Input and output waveforms.

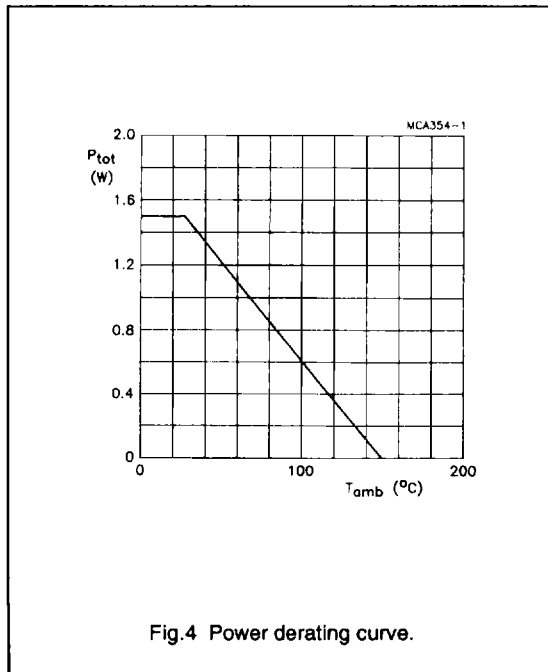


Fig.4 Power derating curve.

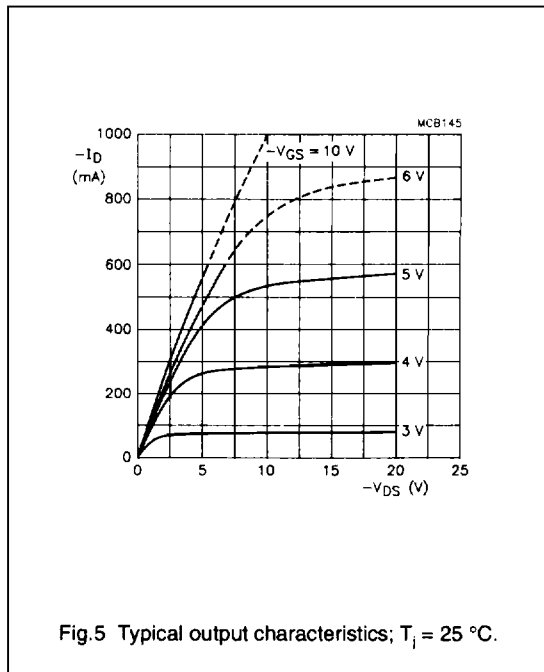
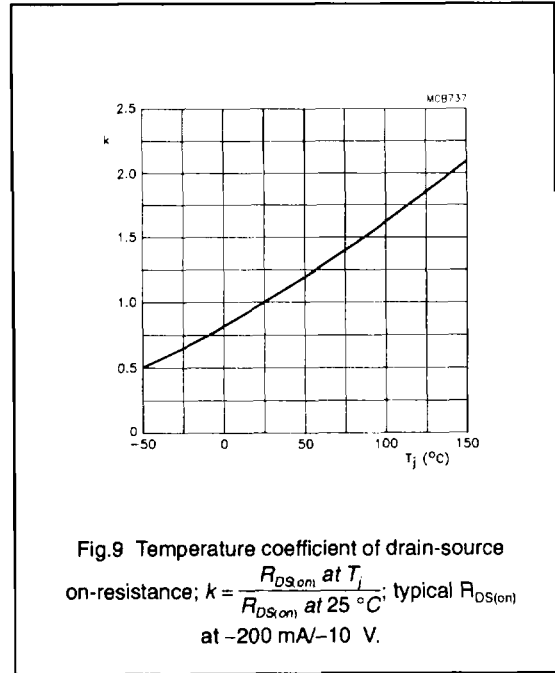
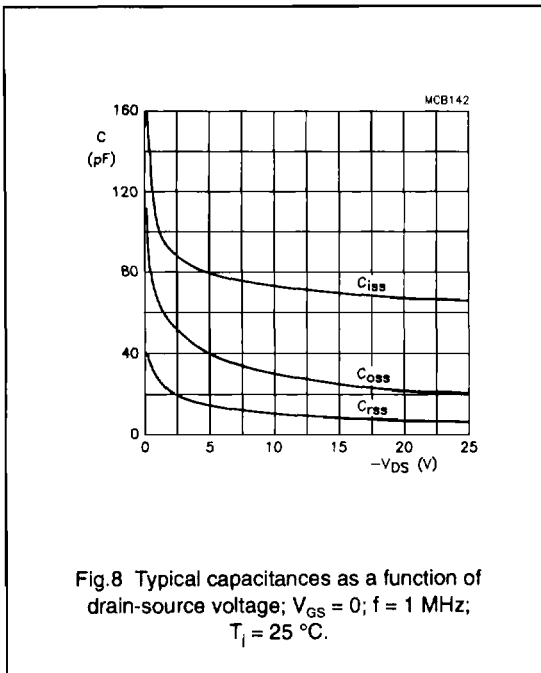
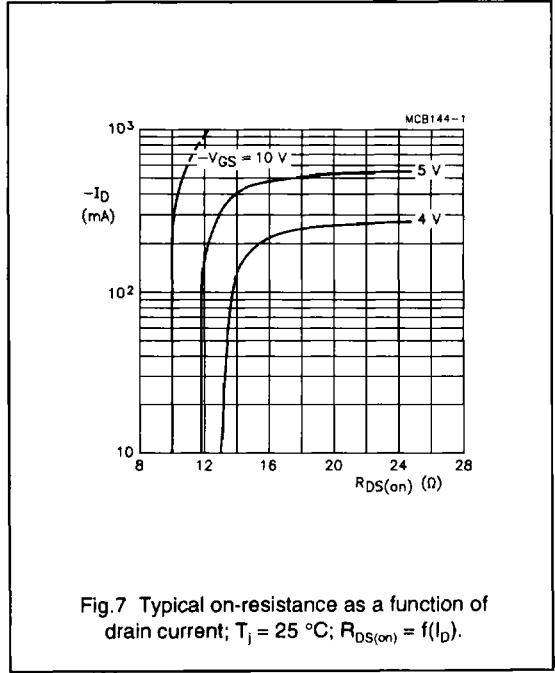
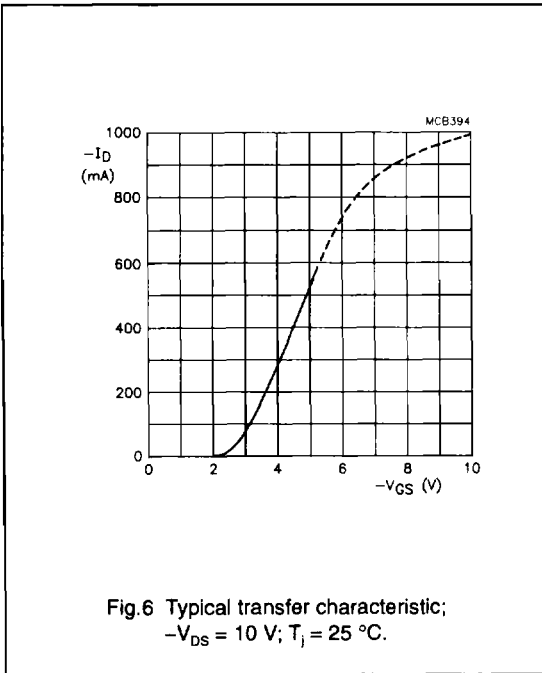


Fig.5 Typical output characteristics; T<sub>j</sub> = 25 °C.

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