



Integrated Device Technology, Inc.

# CMOS STATIC RAM 16K (2K x 8 BIT)

IDT6116SA  
IDT6116LA

### FEATURES:

- High-speed access and chip select times
  - Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - Commercial: 15/20/25/35/45ns (max.)
- Low-power consumption
- Battery backup operation
  - 2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin Thin Dip and Plastic DIP, 28- and 32-pin LCC, 24-pin SOIC, 24-lead CERPACK and 24-pin SOJ
- Military product compliant to MIL-STD-883, Class B

### DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

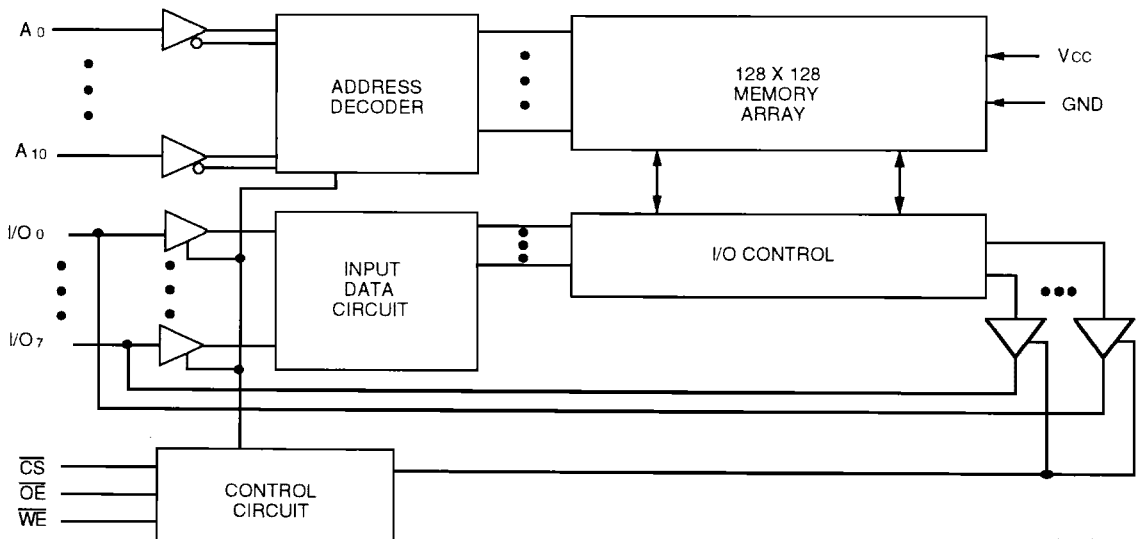
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When  $\overline{CS}$  goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as  $\overline{CS}$  remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 $\mu$ W to 4 $\mu$ W operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### FUNCTIONAL BLOCK DIAGRAM



3089 drw 01

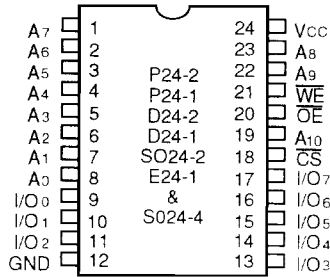
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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**MAY 1994**

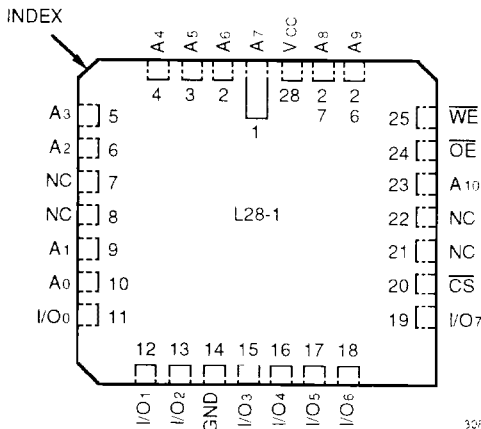
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**PIN CONFIGURATIONS**



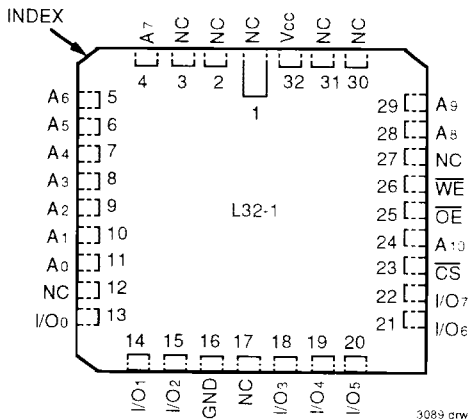
3089 drw 02

**DIP/SOIC/CERPACK/SOJ  
TOP VIEW**



3089 drw 03

**28-PIN LCC  
TOP VIEW**



3089 drw 04

**32-PIN LCC  
TOP VIEW**

**PIN DESCRIPTIONS**

A0-A13	Address Inputs
I/O0-I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

3089 tbl 01

**TRUTH TABLE<sup>(1)</sup>**

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATA <sub>OUT</sub>
Read	L	H	H	High-Z
Write	L	X	L	DATA <sub>IN</sub>

NOTE:

1 H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't Care.

3089 tbl 02



**CAPACITANCE (TA = +25°C, F = 1.0 MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>N</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	8	pF

NOTE:

1 This parameter is determined by device characterization, but is not production tested.

3089 tbl 03

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

NOTES:

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 V<sub>TERM</sub> must not exceed V<sub>CC</sub> +0.5V

3089 tbl 04

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3089 tbl 05

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5 <sup>(2)</sup>	V
GND	Supply Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	3.5	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTES:**

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.
- V<sub>IH</sub> must not exceed V<sub>CC</sub> + 0.5V.

3089 tbl 06

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions	IDT6116SA		IDT6116LA		Unit	
			Min.	Max.	Min.	Max.		
I <sub>L</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max. CS̄ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	—	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	2.4	—	V	

3089 tbl 07

**DC ELECTRICAL CHARACTERISTICS (1)**

V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Power	6116SA15 <sup>(2)</sup> 6116LA15 <sup>(2)</sup>		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I <sub>CC1</sub>	Operating Power Supply Current, CS̄ ≤ V <sub>IL</sub> , Outputs Open, V <sub>CC</sub> = Max., f = 0	SA	105	—	105	130	80	90	80	90	mA
		LA	95	—	95	120	75	85	75	85	
I <sub>CC2</sub>	Dynamic Operating Current, CS̄ ≤ V <sub>IL</sub> , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(4)</sup>	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) CS̄ ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(4)</sup>	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level), CS̄ ≥ V <sub>HC</sub> , V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>HC</sub> or V <sub>IN</sub> ≤ V <sub>LC</sub> , f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

**NOTES:**

- All values are maximum guaranteed values.
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- f<sub>MAX</sub> = 1/t<sub>RC</sub>, only address inputs are cycling at f<sub>MAX</sub>, f = 0 means address inputs are not changing.

3089 tbl 08

**DC ELECTRICAL CHARACTERISTICS <sup>(1)</sup> (Continued)**

V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45		6116SA55 <sup>(3)</sup> 6116LA55 <sup>(3)</sup>		6116SA70 <sup>(3)</sup> 6116LA70 <sup>(3)</sup>		6116SA90 <sup>(3)</sup> 6116LA90 <sup>(3)</sup>		6116SA120 <sup>(3)</sup> 6116LA120 <sup>(3)</sup>		6116SA150 <sup>(3)</sup> 6116LA150 <sup>(3)</sup>		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I <sub>CC1</sub>	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I <sub>CC2</sub>	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$ , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(4)</sup>	SA	100	100	—	100	—	100	—	100	—	100	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(4)</sup>	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$ , V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>HC</sub> or V <sub>IN</sub> ≤ V <sub>LC</sub> , f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

**NOTES:**

1. All values are maximum guaranteed values.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f<sub>MAX</sub> = 1/t<sub>RC</sub>, only address inputs are toggling at f<sub>MAX</sub>. f = 0 means address inputs are not changing.

3089 tbl 09



**DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES**

(LA Version Only) V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

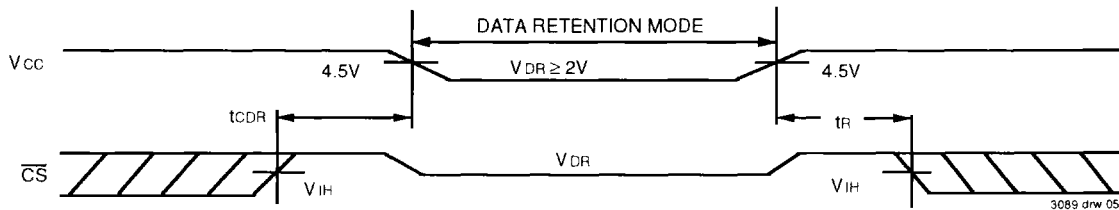
Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>		Max.		Unit	
				V <sub>CC</sub>		V <sub>CC</sub>			
				2.0V	3.0V	2.0V	3.0V		
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	—	2.0	—	—	—	—	V	
I <sub>CCDR</sub>	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL	—	0.5	1.5	200	300	μA
			COM'L	—	0.5	1.5	20	30	
t <sub>CDR</sub> <sup>(3)</sup>	Data Deselect to Data Retention Time	V <sub>IN</sub> ≥ V <sub>HC</sub> or ≤ V <sub>LC</sub>	—	0	—	—	—	ns	
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time			—	—	—	—	ns	
I <sub>LI</sub>	Input Leakage Current		—	—	—	2	2	μA	

**NOTES:**

1. T<sub>A</sub> = +25°C
2. t<sub>RC</sub> = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

3089 tbl 10

**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM**



**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3089 tbi 1.1

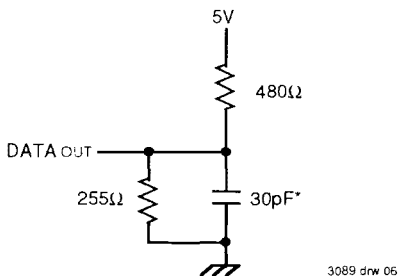


Figure 1. AC Test Load

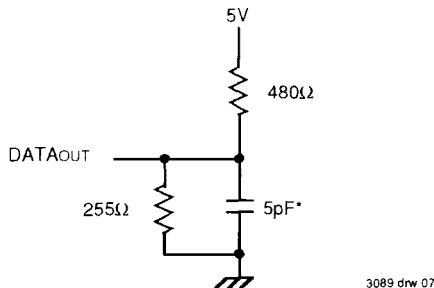


Figure 2. AC Test Load  
(for tOLZ, tCLZ, tOHZ,  
tWHZ, tCHZ & tOW)

\*Including scope and jig.

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)

Symbol	Parameter	6116SA15 <sup>(1)</sup> 6116LA15 <sup>(1)</sup>		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
tCLZ <sup>(3)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
tOLZ <sup>(3)</sup>	Output Enable to Output in Low-Z	0	—	0	—	5	—	5	—	ns
tCHZ <sup>(3)</sup>	Chip Deselect to Output in High-Z	—	10	—	11	—	12	—	15	ns
tOHZ <sup>(3)</sup>	Output Disable to Output in High-Z	—	8	—	8	—	10	—	13	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU <sup>(3)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD <sup>(3)</sup>	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns

3089 tbi 12

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**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges) (Continued)

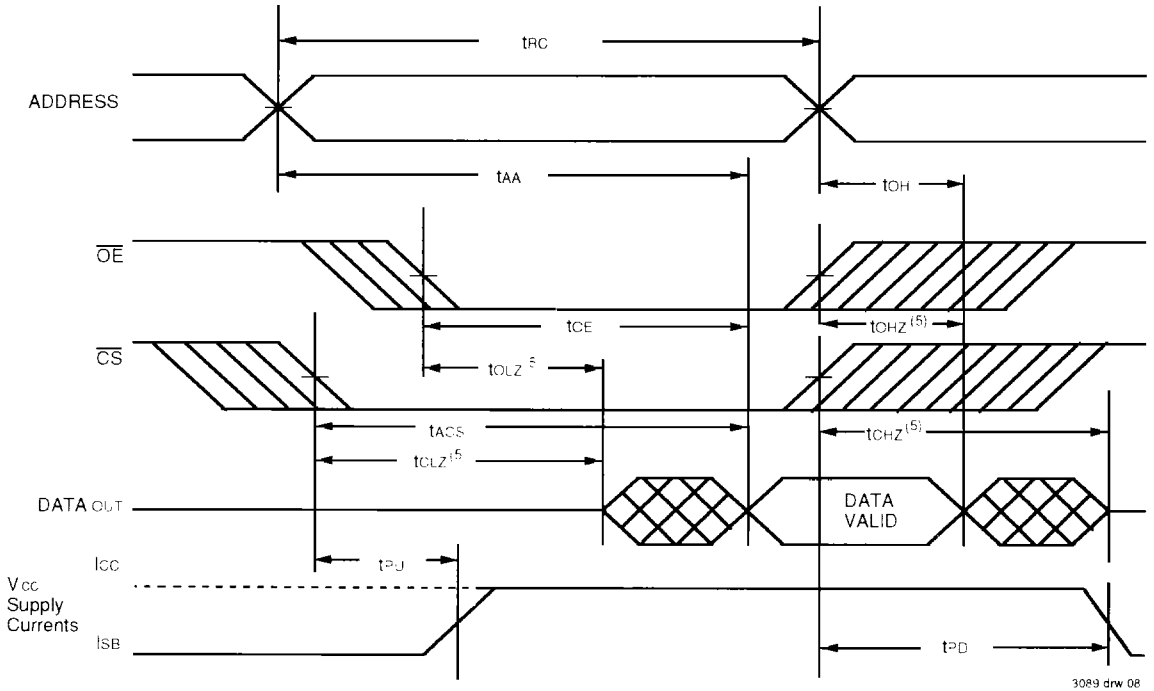
Symbol	Parameter	6116SA45 6116LA45		6116SA55 <sup>(2)</sup> 6116LA55 <sup>(2)</sup>		6116SA70 <sup>(2)</sup> 6116LA70 <sup>(2)</sup>		6116SA90 <sup>(2)</sup> 6116LA90 <sup>(2)</sup>		6116SA120 <sup>(2)</sup> 6116LA120 <sup>(2)</sup>		6116SA150 <sup>(2)</sup> 6116LA150 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>														
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
tACS	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
tCLZ <sup>(3)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
tOLZ <sup>(3)</sup>	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ <sup>(3)</sup>	Chip Deselect to Output in High-Z	—	20	—	30	—	35	—	40	—	40	—	40	ns
tOHZ <sup>(3)</sup>	Output Disable to Output in High-Z	—	15	—	30	—	35	—	40	—	40	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

**NOTES:**

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

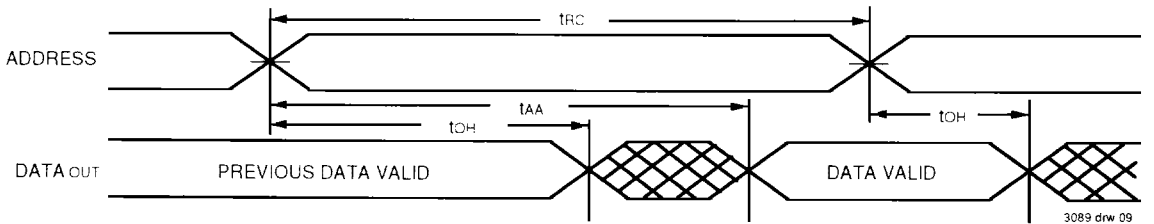
3089 tbi 13

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1, 3)</sup>**



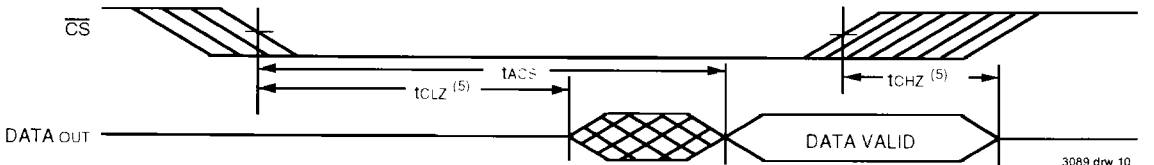
3089 drw 08

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



3089 drw 09

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**



3089 drw 10

**NOTES:**

1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. OE is LOW.
5. Transition is measured  $\pm 500\text{mV}$  from steady state.

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)

Symbol	Parameter	6116SA15 <sup>(1)</sup> 6116LA15 <sup>(1)</sup>		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End-of-Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ <sup>(3)</sup>	Write to Output in High-Z	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH <sup>(4)</sup>	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW <sup>(3,4)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

3089 tbl 14



**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)

Symbol	Parameter	6116SA45 6116LA45		6116SA55 <sup>(2)</sup> 6116LA55 <sup>(2)</sup>		6116SA70 <sup>(2)</sup> 6116LA70 <sup>(2)</sup>		6116SA90 <sup>(2)</sup> 6116LA90 <sup>(2)</sup>		6116SA120 <sup>(2)</sup> 6116LA120 <sup>(2)</sup>		6116SA150 <sup>(2)</sup> 6116LA150 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tWHZ <sup>(3)</sup>	Write to Output in High-Z	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH <sup>(4)</sup>	Data Hold from Write Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW <sup>(3,4)</sup>	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

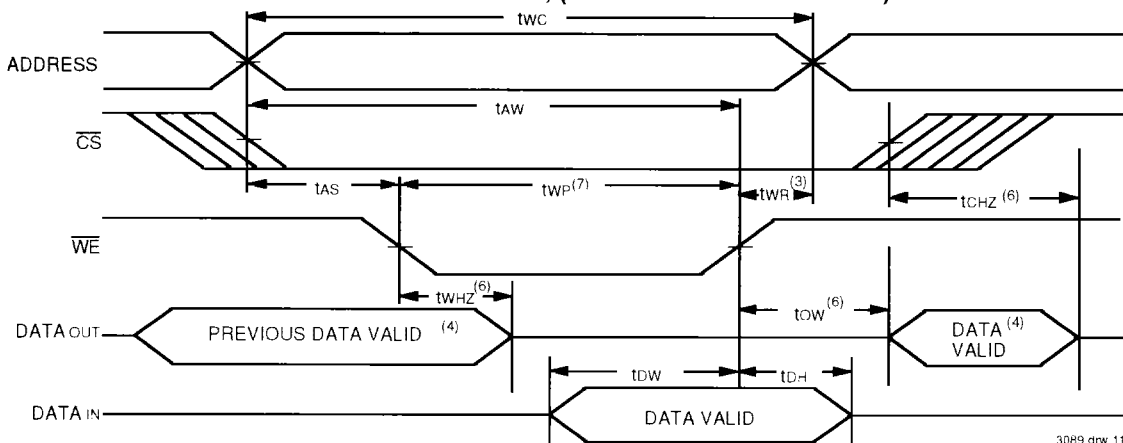
**NOTES:**

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
- The specification for t<sub>DH</sub> must be met by the device supplying write data to the RAM under all operation conditions. Although t<sub>DH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.

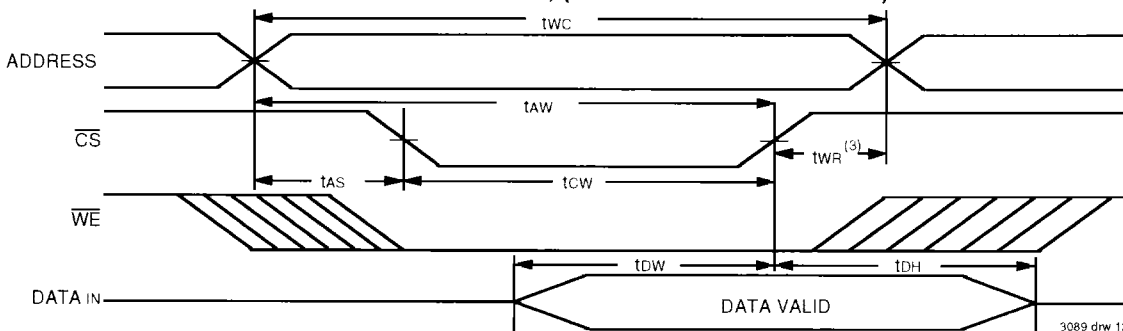
3089 tbl 15



**TIMING WAVEFORM OF WRITE CYCLE NO. 1, ( $\overline{WE}$  CONTROLLED TIMING) (1, 2, 5, 7)**



**TIMING WAVEFORM OF WRITE CYCLE NO. 2, ( $\overline{CS}$  CONTROLLED TIMING) (1, 2, 3, 5, 7)**



**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $tWR$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured  $\pm 500mV$  from steady state
7.  $\overline{OE}$  is continuously HIGH. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $tWP$  or  $(tWHZ + tOW)$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $tOW$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse is the specified  $tWP$ . For a  $\overline{CS}$  controlled write cycle,  $\overline{OE}$  may be LOW with no degradation to  $tCW$ .

**ORDERING INFORMATION**

IDT	6116	XX	XXX	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
						Blank Commercial (0°C to +70°C)
						B Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
						TP 300 mil Plastic DIP (P24-2)
						P 600 mil Plastic DIP (P24-1)
						TD 300 mil CERDIP (D24-2)
						D 600 mil CERDIP (D24-1)
						L28 Leadless Chip Carrier (L28-1)
						L32 Leadless Chip Carrier (L32-1)
						SO 300 mil Small Outline IC, Gull-Wing Bend (SO24-2)
						E 300 mil CERPACK (E24-1)
						Y 300 mil SOJ, J-Bend (SO24-4)
						15 Commercial Only
						20
						25
						35
						45
						55 Military Only
						70 Military Only
						90 Military Only
						120 Military Only
						150 Military Only
						SA Standard Power
						LA Low Power

} Speed in nanoseconds

3089 drw 13



