PMC-SIERRA

# GEN-M7K-56-000 Data Sheet

A MEMBER OF PMC-SIERRA'S CLOCK FAMILY



## System Clock Generator For MIPS-Based Designs

PMC-Sierra's GEN-M7K-56-000 is perfectly tailored to perform the clock generation required in a design using MIPS-based™ processors. The GEN-M7K-56-000 covers the clocking needs of the 5K and 7K generations of MIPS® processors including PMC-Sierra's own leading line: RM5231A, RM5261A, RM7000A, RM7000B, RM7000C, RM7035C, RM7065C, RM7900, RM7935 and RM7965.

PMC-Sierra's CM5470 clock generator is superior in price, size, power and performance to other discrete solutions.

## Features

### Generated Clocks

- Uses a single 14.31818 MHz crystal or single-ended LVTTL input reference. Outputs a 3.3V LVTTL copy of the reference frequency.
- Generates three copies of a CPU clock output, each can be independently powered for 3.3V or 2.5V LVTTL operation.
- CPU clock frequency is pin-selectable for eight common system clock frequencies: 50.00 MHz, 66.67 MHz, 83.33 MHz, 100.00 MHz, 125.00 MHz, 133.33 MHz, 166.67 MHz, and 200.00 MHz.
- Generates six copies of a RAM clock output at same frequency as CPU clock, with dedicated output enable (for power saving mode). The RAM clocks can be operated as 2.5V SSTL_2 Class I (supports DDR RAM), 3.3V LVTTL or 2.5V LVTTL (supports SDRAM).
- Generates four copies of a 3.3V or 2.5V LVTTL PCI clock output, pin-configurable for 33.33 or 66.67 MHz.
- Generates one copy of a 3.3V or 2.5V LVTTL USB clock output, pin-configurable for 12.00, 24.00, 30.00 or 48.00 MHz.
- Generates one copy of a 3.3V or 2.5V LVTTL 25.00 MHz clock suitable for LAN or S-ATA reference.
- CPU and RAM clock maximum cycle-to-cycle phase jitter of 150ps and maximum period jitter of 150 ps.
- Maximum output-to-output phase skew (within same group) of 100ps.

### Spread Spectrum

- Provides optional spread spectrum phase modulation applied to all CPU, RAM and PCI clock outputs, enabled and configured via dedicated control pins.

### Power Supply

- 3.3V ± 5%
- 2.5V ± 8% for 2.5V SSTL_2 supplies
- 2.5V ± 5% for all other 2.5V supplies

### Temperature Range

- 0C to 70C ("Commercial")

### Packaging

- 56-pin TSSOP
- "Green" lead-free (matte-tin) packaging option available

### ESD Protection

- 2 kV HBM
- 500V CDM



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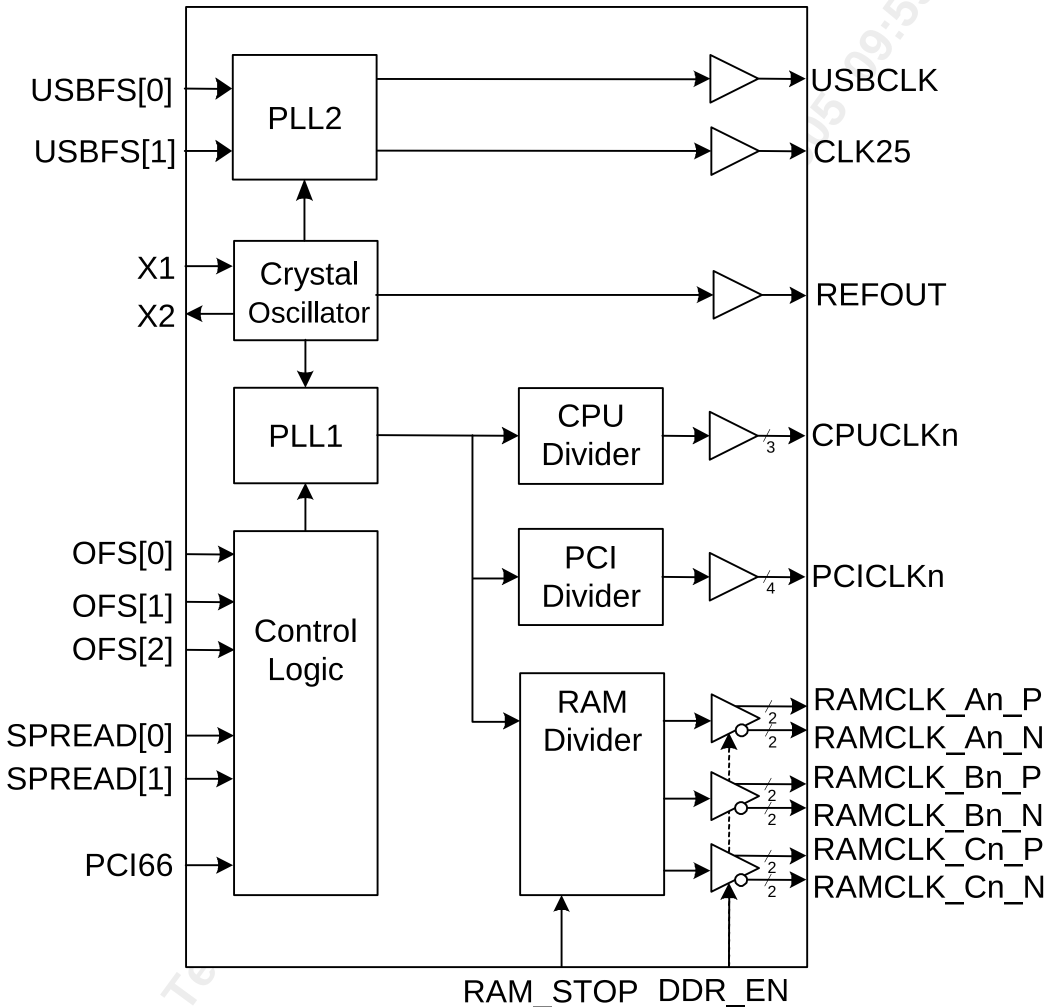
## Block Diagram



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# GEN-M7K-56-000 Data Sheet

## Pin Diagram

**CM5470**

| Pin Name | Pin No. | Pin No. | Pin Name |
|---|---|---|---|
| VDD_USB | 1 | 56 | USBCLK |
| PCICLK1 | 2 | 55 | VSS |
| PCICLK2 | 3 | 54 | CLK25 |
| VDD_PCI | 4 | 53 | VDD_CLK25 |
| PCICLK3 | 5 | 52 | VDD_RAM_A |
| PCICLK4 | 6 | 51 | VSS |
| VSS | 7 | 50 | RAMCLK_A1_P |
| VSS | 8 | 49 | RAMCLK_A1_N |
| X1 | 9 | 48 | RAMCLK_A2_P |
| X2 | 10 | 47 | RAMCLK_A2_N |
| DDR_EN | 11 | 46 | RAMCLK_B1_P |
| RAM_STOP | 12 | 45 | RAMCLK_B1_N |
| VDD_REF | 13 | 44 | VSS |
| VSS | 14 | 43 | VDD_RAM_B |
| USBFS[0] | 15 | 42 | RAMCLK_B2_P |
| USBFS[1] | 16 | 41 | RAMCLK_B2_N |
| REFOUT | 17 | 40 | RAMCLK_C1_P |
| VDD | 18 | 39 | RAMCLK_C1_N |
| SPREAD[0] | 19 | 38 | RAMCLK_C2_P |
| SPREAD[1] | 20 | 37 | RAMCLK_C2_N |
| OFS[0] | 21 | 36 | VSS |
| OFS[1] | 22 | 35 | VDD_RAM_C |
| OFS[2] | 23 | 34 | VDD_CPU1 |
| VDD | 24 | 33 | CPUCLK1 |
| VSS | 25 | 32 | VSS |
| PCI66 | 26 | 31 | VDD_CPU2 |
| VDD_CPU3 | 27 | 30 | CPUCLK2 |
| VSS | 28 | 29 | CPUCLK3 |



## Pin Assignment and Description

| Pin Name | Pin No. | Type | Pin Description |
|---|---|---|---|
| CLK25 | 54 | O | 25 MHz Clock Output: This is a 25.00 MHz output clock, suitable for LAN and S-ATA reference. |
| CPUCLK1, CPUCLK2, CPUCLK3 | 33, 30, 29 | O | CPU Clock Output #1, #2, and #3. The frequency is controlled by the OFS[2:0] inputs as shown in the table "CPUCLK and RAMCLK Output Frequency Options" The available frequencies are 50.00 MHz, 66.67 MHz, 83.33 MHz, 100.00 MHz, 125.00 MHz, 133.33 MHz, 166.67 MHz or 200.00 MHz. |

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| Pin Name | Pin No. | Type | Pin Description |
|---|---|---|---|
| DDR_EN | 11 | I | DDR Mode Enable: When logic low, the RAMCLK outputs RAMCLK_xn_P act as single-ended outputs (RAMCLK_xn_N outputs are high-impedance); when logic high, the RAMCLK outputs act as differential outputs (RAMCLK_xn_N is the complement to RAMCLK_xn_P).<br><br>There is an integrated pull-up resistor (Note 1) on this input. |
| OFS[2:0] | 23, 22, 21 | I | Output Frequency Select [2:0]: Controls the CPUCLK and RAMCLK_xn output frequency. See table “CPU and RAMCLK Output Frequency Options” for settings.<br><br>There are integrated pull-up resistors (Note 1) on these inputs. |
| PCI66 | 26 | I | PCI Clock Frequency Select: Controls the output frequency of the PCI clock outputs. When logic low, the PCI clock frequency is 33.33 MHz; when logic high, the PCI clock frequency is 66.67 MHz.<br><br>There is an integrated pull-up resistor (Note 1) on this input. |
| PCICLK1,<br>PCICLK2,<br>PCICLK3,<br>PCICLK4 | 2,<br>3,<br>5,<br>6 | O | PCI Clock Output 1, 2, 3 and 4. The frequency (33.33 MHz or 66.66 MHz) is controlled by the PCI66 input.<br><br>These PCI clocks are free-running. There is no PCI STOP function in this device. |
| RAM_STOP | 12 | I | RAM_STOP: When logic low, the RAMCLK_xn outputs operate normally; when logic high, all the RAMCLK_xn outputs are disabled to support system power saving schemes. The RAMCLK_xn outputs are disabled with no glitches. Refer to the “RAM_STOP Timing” section for a timing diagram of the RAM_STOP operation.<br><br>In LVTTL mode, the RAMCLK_An_P output is forced to logic 0. In SSTL_2 Class I mode, the RAMCLK_An_N output is forced to logic 1 and the RAMCLK_An_P is forced to logic 0.<br><br>There is an integrated pull-down resistor (Note 1) on this input. |
| RAMCLK_A1_P,<br>RAMCLK_A1_N,<br>RAMCLK_A2_P,<br>RAMCLK_A2_N, | 50, | O | RAM Clock Differential Pair #A1 and #A2:<br><br>**LVTTL mode**: If DDR_EN is logic low, then RAMCLK_An_P acts as a single-ended LVTTL output running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs as shown in the table “CPUCLK and RAMCLK Output Frequency Options”). The RAMCLK_An_N output is high-impedance. The LVTTL outputs can operate at 2.5V or 3.3V depending on the |

| Pin Name | Pin No. | Type | Pin Description |
|---|---|---|---|
| | | | voltage applied to VDD_RAM_A.<br><br>**SSTL_2 Class I mode**: If DDR_EN is logic high, then RAMCLK_An_P and RAMCLK_An_N form a 2.5V SSTL_2 Class I differential pair running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs).<br><br>**Power Savings mode**: If RAM_STOP is logic low then RAMCLK_An_P and RAMCLK_An_N operate as described above; if RAM_STOP is logic high then the outputs are held static. In LVTTL mode, the RAMCLK_An_P output is forced to logic 0. In SSTL_2 Class I mode, the RAMCLK_An_N output is forced to logic 1 and the RAMCLK_An_P is forced to logic 0.<br><br>**Power Down mode**: If the RAM clock output pairs #A1 and #A2 are unused they should be powered down by grounding VDD_RAM_A. |
| RAMCLK_B1_P,<br>RAMCLK_B1_N,<br>RAMCLK_B2_P,<br>RAMCLK_B2_N, | 46,<br>45,<br>42,<br>41 | O | RAM Clock Differential Pair #B1 and #B2:<br><br>**LVTTL mode**: If DDR_EN is logic low, then RAMCLK_Bn_P acts as a single-ended LVTTL output running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs as shown in the table "CPUCLK and RAMCLK Output Frequency Options"). The RAMCLK_Bn_N output is high-impedance. The LVTTL outputs can operate at 2.5V or 3.3V depending on the voltage applied to VDD_RAM_B.<br><br>**SSTL_2 Class I mode**: If DDR_EN is logic high, then RAMCLK_Bn_P and RAMCLK_Bn_N form an SSTL_2 Class I differential pair running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs).<br><br>**Power Savings mode**: If RAM_STOP is logic low then RAMCLK_Bn_P and RAMCLK_Bn_N operate as described above; if RAM_STOP is logic high then the outputs are held static. In LVTTL mode, the RAMCLK_Bn_P output is forced to logic 0. In SSTL_2 Class I mode, the RAMCLK_Bn_N output is forced to logic 1 and the RAMCLK_Bn_P is forced to logic 0.<br><br>**Power Down mode**: If the RAM clock output pairs #B1 and #B2 are unused they should be powered down by grounding VDD_RAM_B. |

| Pin Name | Pin No. | Type | Pin Description |
|---|---|---|---|
| RAMCLK_C1_P,<br>RAMCLK_C1_N,<br>RAMCLK_C2_P,<br>RAMCLK_C2_N | 40,<br>39,<br>38,<br>37 | O | RAM Clock Differential Pair #C1 and #C2:<br><br>**LVTTL mode**: If DDR_EN is logic low, then RAMCLK_Cn_P acts as a single-ended LVTTL output running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs as shown in the table "CPUCLK and RAMCLK Output Frequency Options"). The RAMCLK_Cn_N output is high-impedance. The LVTTL outputs can operate at 2.5V or 3.3V depending on the voltage applied to VDD_RAM_C.<br><br>**SSTL_2 Class I mode**: If DDR_EN is logic high, then RAMCLK_Cn_P and RAMCLK_Cn_N form an SSTL_2 Class I differential pair running at the CPUCLKn frequency (as controlled by the OFS[2:0] inputs).<br><br>**Power Savings mode**: If RAM_STOP is logic low then RAMCLK_Cn_P and RAMCLK_Cn_N operate as described above; if RAM_STOP is logic high then the outputs are held static. In LVTTL mode, the RAMCLK_Cn_P output is forced to logic 0. In SSTL_2 Class I mode, the RAMCLK_Cn_N output is forced to logic 1 and the RAMCLK_Cn_P is forced to logic 0.<br><br>**Power Down mode**: If the RAM clock output pairs #C1 and #C2 are unused they should be powered down by grounding VDD_RAM_C. |
| REFOUT | 17 | O | 14.31818 MHz Reference Clock Output: This is a buffered copy of the clock generated by the internal crystal oscillator controlled by the crystal between X1 and X2 pins or a single-ended input applied to X1. |
| SPREAD[1:0] | 20, 19 | I | Spread Spectrum Control [1:0]: Enables spread spectrum modulation on all CPUCLKn, RAMCLK_xn and PCICLKn clock outputs. See table "Spread Spectrum Algorithm Options" for configuration information.<br><br>There are integrated pull-up resistors (Note 1) on these inputs. |
| USBCLK | 56 | O | USB Clock Output: The frequency (12 MHz, 24 MHz, 30 MHz or 48 MHz) is controlled by the USBFS[1:0] inputs. |
| USBFS[1:0] | 16, 15 | I | USB Frequency Select [1:0]: Controls the USB clock output frequency. See table "USBCLK Output Frequency Options" for configuration information.<br><br>There are integrated pull-up resistors (Note 1) on these inputs. |

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| Pin Name | Pin No. | Type | Pin Description |
|---|---|---|---|
| VDD_CLK25 | 53 | PWR | 3.3V or 2.5V Power Supply: Power for CLK25 output.<br><br>If the CLK25 output is not used, this power pin should be grounded to minimize power consumption. |
| VDD_CPU1,<br>VDD_CPU2,<br>VDD_CPU3 | 34,<br>31,<br>27 | PWR | 3.3V or 2.5V Power Supply: Each CPUCLKn output can be independently powered to either 3.3V or 2.5V.<br><br>If a CPUCLKn output is not used, the associated power pin should be grounded to minimize power consumption. |
| VDD_PCI | 4 | PWR | 3.3V or 2.5V Power Supply: Power for PCICLKn outputs.<br><br>If the PCICLKn outputs are not used, this power pin should be grounded to minimize power consumption. |
| VDD_RAM_A | 52 | PWR | 3.3V or 2.5V Power Supply: For RAMCLK_An clock outputs.<br><br>If the RAMCLK_An outputs are not used, this power pin should be grounded to minimize power consumption. |
| VDD_RAM_B | 43 | PWR | 3.3V or 2.5V Power Supply: For RAMCLK_Bn clock outputs.<br><br>If the RAMCLK_Bn outputs are not used, this power pin should be grounded to minimize power consumption. |
| VDD_RAM_C | 35 | PWR | 3.3V or 2.5V Power Supply: For RAMCLK_Cn clock outputs.<br><br>If the RAMCLK_Cn outputs are not used, this power pin should be grounded to minimize power consumption. |
| VDD_REF | 13 | PWR | 3.3V Power Supply |
| VDD_USB | 1 | PWR | 3.3V or 2.5V Power Supply: Power for USBCLK output.<br><br>If the USBCLK output is not used, this power pin should be grounded to minimize power consumption. |
| VDD | 24, 18 | PWR | 3.3V Power Supply |
| VSS | 7, 8, 14, 25, 28, 32, 36, 44, 51, 55 | GND | Ground Reference |
| X1,<br>X2 | 9<br>10 | I/O | Crystal Reference In & Out: These can either be spanned by a crystal or accept a single-ended reference input (X1 only). The input frequency is 14.31818 MHz. When using a crystal, the load capacitance (Cload) rating must be 18 pF.<br><br>For single-ended operation, X2 must be left unconnected. |

**Notes On Pin Assignment And Description**

1. Integrated pull-up and pull-down resistors are nominally 200 kΩ.

## Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal operating conditions.

### Absolute Maximum Ratings

| | |
|---|---|
| Ambient Temperature under Bias | 0C to +70C |
| Storage Temperature | -65°C to +150°C |
| Supply Voltage $V_{DD}$ | -0.5V to +4.6V |
| Voltage on Any Pin | -0.5V to +4.6V |
| Static Discharge Voltage (HBM) | ±2000V |
| Static Discharge Voltage (CDM) | ±500V |
| Latch-Up Current | ±100mA |
| DC Input Current | ±20mA |
| Lead Temperature | +225°C |
| Junction Temperature | +150°C |

## D.C. Characteristics

**$T_A$ = 0C to +70C, $V_{DD}$ = 3.3V ± 5%**
**(Typical Conditions: $T_A$ = 25C, $V_{DD}$ = 3.3V)**

### Device D.C. Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VDD3V3 | 3.3V Power Supply | 3.135 | 3.465 | V | Referenced to GND |
| $VDD2V5_{LVTTL}$ | LVTTL 2.5V Power Supply | 2.375 | 2.625 | V | Referenced to GND |
| $VDD2V5_{SSTL\_2}$ | SSTL_2 2.5V Power Supply | 2.3 | 2.7 | V | Referenced to GND |
| VIL | Input Low Voltage | | 0.8 | V | Guaranteed Input LOW Voltage |
| VIH | Input High Voltage | 2.0 | VDD3V3 | V | Guaranteed Input HIGH Voltage |
| IIL | Input Low Current | -10 | +10 | µA | VIL = GND. See Notes 1 and 2 |
| IIH | Input High Current | -10 | +10 | µA | VIH = VDD3V3. See Notes 1 and 2 |
| $I_{LUP}$ | Input Low Leakage Current For Inputs With Pull-Up Resistors | -60 | -10 | µA | VIL = GND. See Note 1 and 2 |
| $I_{HUP}$ | Input High Leakage Current For Inputs With Pull-Up Resistors | -10 | +10 | µA | VIH = VDD3V3. See Note 1 |
| $I_{LDWN}$ | Input Low Current For Inputs With Pull-Down Resistors | -10 | +10 | µA | VIL = GND. See Note 1 and 2 |
| $I_{HDWN}$ | Input High Current For Inputs With Pull-Down Resistors | +10 | +60 | µA | VIH = VDD3V3. See Note 1 |

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| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| CIN | Input Capacitance | | 5 | pF | |
| COUT | Output Capacitance | | 5 | pF | |
| $C_{xtal}$ | X1, X2 Pin Capacitance | 28.8 | 43.2 | pF | Nominal capacitance of 36 pF |
| $C_{load\_LVTTL}$ | Max output load, 2.5V or 3.3V LVTTL | | 30 | pF | See Note 3 |

**Notes On Device D.C. Characteristics**

1. Positive currents sink into the device.
2. Negative currents are sourced from the device.
3. Output loading is constrained by thermal conditions. See section “Power Considerations”.

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### Device Power D.C. Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| IDDOPvdd | Operating current on VDD power supply | | 65.8 | 72.1 | mA | |
| IDDOPcpun33 | Operating current on each 3.3V VDD_CPUn power supply | | TBD | TBD | mA | Operation at 200 MHz (maximum frequency), outputs unloaded. See Power Considerations section. |
| IDDOPcpun25 | Operating current on each 2.5V VDD_CPUn power supply | | TBD | TBD | mA | Operation at 200 MHz (maximum frequency), outputs unloaded. See Power Considerations section. |
| IDDOPram33 | Operating current on each 3.3V VDD_RAM_n power supply | | TBD | TBD | mA | Operation at 200 MHz (maximum frequency). DDR_EN = 0. RAM_STOP = 0. Outputs unloaded. See Power Considerations section. |
| IDDOPram25 | Operating current on each 2.5V VDD_RAM_n power supply | | TBD | TBD | mA | Operation at 200 MHz (maximum frequency). DDR_EN = 0. RAM_STOP = 0. Outputs unloaded. See Power Considerations section. |
| IDDOPramsstl2 | Operating current on each 2.5V VDD_RAM_n power supply | | TBD | TBD | mA | Operation at 200 MHz (maximum frequency). DDR_EN = 1. RAM_STOP = 0. Outputs unloaded. See Power Considerations section. |
| IDDOPusb33 | Operating current on 3.3V VDD_USB power supply | | TBD | TBD | mA | Operation at 48 MHz (maximum frequency), output unloaded. See Power Considerations section. |
| IDDOPusb25 | Operating current on 2.5V VDD_USB power supply | | TBD | TBD | mA | Operation at 48 MHz (maximum frequency), output unloaded. See Power Considerations section. |
| IDDOPpci33 | Operating current on 3.3V VDD_PCI power supply | | TBD | TBD | mA | PCI66 = 1. Outputs unloaded. See Power Considerations section. |
| IDDOPpci25 | Operating current on 2.5V VDD_PCI power supply | | TBD | TBD | mA | PCI66 = 1. Outputs unloaded. See Power Considerations section. |
| IDDOPref33 | Operating current on 3.3V VDD_REF power supply | | TBD | TBD | mA | Outputs unloaded. See Power Considerations section. |
| IDDOPclk2533 | Operating current on 3.3V VDD_CLK25 power supply | | TBD | TBD | mA | Outputs unloaded. See Power Considerations section. |
| IDDOPclk2525 | Operating current on 2.5V VDD_CLK25 power supply | | TBD | TBD | mA | Outputs unloaded. See Power Considerations section. |

## CPUCLK, RAMCLK (DDR_EN = 0) and REFOUT (3.3V data only) D.C. Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VOL3V3 | Output Low Voltage | | 0.4 | V | VDD_xxx=3.3V, IOL = 18mA, See Notes 1 and 3 |
| VOH3V3 | Output High Voltage | 2.4 | | V | VDD_xxx=3.3V, IOH = -18mA, See Notes 2 and 3 |
| IOH3V3 | Output High Current | -37.5 | | mA | VDD_xxx=3.3V, VOH = 1.0V. See Note 3 |
| IOH3V3 | Output High Current | | -35 | mA | VDD_xxx=3.3V, VOH = 3.135V. See Note 3 |
| IOL3V3 | Output Low Current | 37.5 | | mA | VDD_xxx=3.3V, VOL = 1.95V. See Note 3 |
| IOL3V3 | Output Low Current | | 30 | mA | VDD_xxx=3.3V, VOL = 0.4V. See Note 3 |
| VOL2V5 | Output Low Voltage | | 0.4 | V | VDD_xxx=2.5V, IOL = 13mA, See Notes 1 and 3 |
| VOH2V5 | Output High Voltage | 2.0 | | V | VDD_xxx=2.5V, IOH = -7mA, See Notes 2 and 3 |
| IOH2V5 | Output High Current | -20 | | mA | VDD_xxx=2.5V, VOH = 0.75V. See Note 3 |
| IOH2V5 | Output High Current | | -22 | mA | VDD_xxx=2.5V, VOH = 2.375V. See Note 3 |
| IOL2V5 | Output Low Current | 22 | | mA | VDD_xxx=2.5V, VOL = 1.48V. See Note 3 |
| IOL2V5 | Output Low Current | | 23 | mA | VDD_xxx=2.5V, VOL = 0.3V. See Note 3 |

**Notes On CPUCLK, RAMCLK (DDR_EN = 0) and REFOUT (3.3V data only) D.C. Characteristics**

1. Positive currents sink into the device.
2. Negative currents are sourced from the device.
3. 'VDD_xxx' is the general symbol to denote the respective VDD_CPU1-3, VDD_RAM_A-C and VDD_REF supplies.

## RAMCLK (DDR_EN = 1) D.C. Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VOHSSTL21 | Output High Voltage | 1.74 | | V | IHsstl21 = -8.1mA, VDD_RAM = 2.3V. See Note 2. |
| VOLSSTL21 | Output Low Voltage | | 0.56 | V | ILsstl21 = 8.1mA, VDD_RAM = 2.3V. See Note 2. |
| IOHSSTL21 | Output High Current | -8.1 | | mA | VOH @ min = 1.74V. VDD_RAM = 2.3V. See Notes 2 and 4. |
| IOLSSTL21 | Output Low Current | 8.1 | | mA | VOL @ min = 0.56V. VDD_RAM = 2.3V. See Notes 1 and 4. |
| ROSSTL21 | On Resistance | | 69 | Ω | |

**Notes On RAMCLK (DDR_EN = 1) D.C. Characteristics**

1. Positive currents sink into the device.
2. Negative currents are sourced from the device.
3. Termination conditions for SSTL_2 Class I are defined in JEDEC standard JESD8-9B[3].
4. Vtt is defined as VDD_RAM/2, Rs = 25Ω and Rt = 50Ω as per JESD8-9B.

 

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### PCICLK, USBCLK and CLK25 D.C. Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| VOL3V3 | Output Low Voltage | | 0.4 | V | VDD_xxx=3.3V, IOL = 10.8mA, See Notes 1 and 3 |
| VOH3V3 | Output High Voltage | 2.4 | | V | VDD_xxx=3.3V, IOH = -10.8mA, See Notes 2 and 3 |
| IOH3V3 | Output High Current | -22.5 | | mA | VDD_xxx=3.3V, VOH = 1.0V. See Note 3 |
| IOH3V3 | Output High Current | | -21 | mA | VDD_xxx=3.3V, VOH = 3.135V. See Note 3 |
| IOL3V3 | Output Low Current | 22.5 | | mA | VDD_xxx=3.3V, VOL = 1.95V. See Note 3 |
| IOL3V3 | Output Low Current | | 18 | mA | VDD_xxx=3.3V, VOL = 0.4V. See Note 3 |
| VOL2V5 | Output Low Voltage | | 0.4 | V | VDD_xxx=2.5V, IOL = 7.8mA, See Notes 1 and 3 |
| VOH2V5 | Output High Voltage | 2.0 | | V | VDD_xxx=2.5V, IOH = -4.2mA, See Notes 2 and 3 |
| IOH2V5 | Output High Current | -12 | | mA | VDD_xxx=2.5V, VOH = 0.75V. See Note 3 |
| IOH2V5 | Output High Current | | -13.2 | mA | VDD_xxx=2.5V, VOH = 2.375V. See Note 3 |
| IOL2V5 | Output Low Current | 13.2 | | mA | VDD_xxx=2.5V, VOL = 1.48V. See Note 3 |
| IOL2V5 | Output Low Current | | 13.8 | mA | VDD_xxx=2.5V, VOL = 0.3V. See Note 3 |

**Notes On PCICLK, USBCLK and CLK25 D.C. Characteristics**

1. Positive currents sink into the device.
2. Negative currents are sourced from the device.
3. 'VDD_xxx' is the general symbol to denote the respective VDD_PCI, VDD_USB and VDD_CLK25 supplies.

## A.C. Characteristics

### $T_A$ = 0C to +70C, $V_{DD}$ = 3.3V ± 5%
### (Typical Conditions: $T_A$ = 25C, $V_{DD}$ = 3.3V)

### Parameters valid for both 3.3V and 2.5V operation

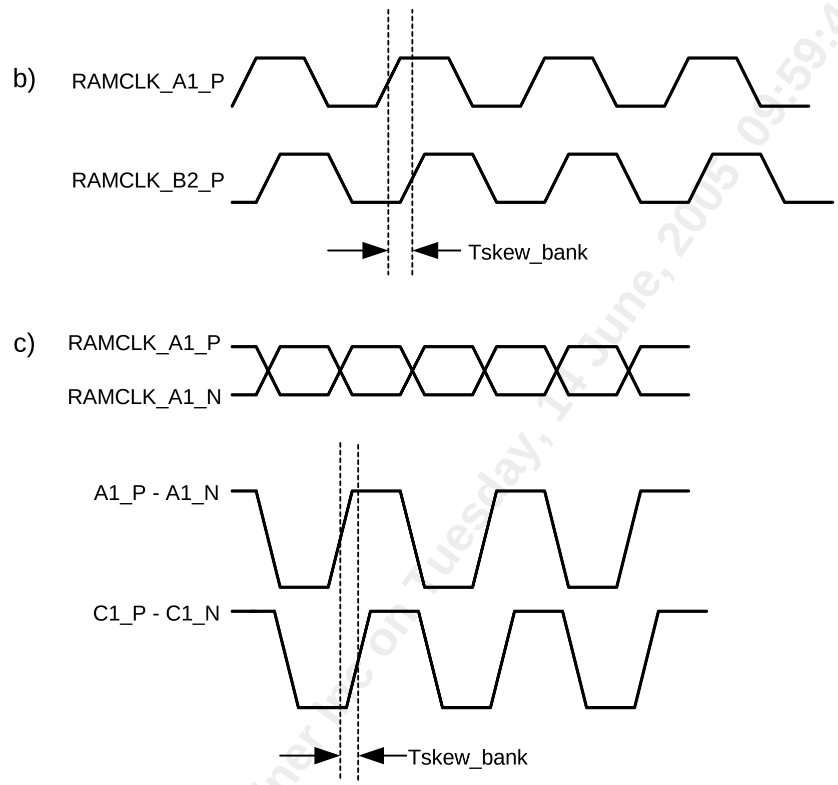
| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{out\_cpu}$ | CPUCLK Output Frequency | Nominal frequency controlled by OFS[2:0] inputs. See Note 1. | 50.00 | 200.00 | MHz |
| $f_{out\_RAM}$ | RAMCLK Output Frequency | Nominal frequency controlled by OFS[2:0] inputs. See Note 1. | 50.00 | 200.00 | MHz |
| $f_{out\_PCI}$ | PCICLK Output Frequency | Nominal frequency controlled by PCI66 input. See Note 1. | 33.33 | 66.66 | MHz |
| $f_{out\_usb}$ | USBCLK Output Frequency | Nominal frequency controlled by USBFS[1:0] inputs. See Note 1. | 12.00 | 48.00 | MHz |
| $f_{out\_25}$ | CLK25 Output Frequency | Nominally 25.00 MHz. See Note 1. | 25.00 | 25.00 | MHz |
| $f_{out\_ref}$ | REFOUT Output Frequency | Nominally 14.31818 MHz. See Note 1. | 14.31818 | 14.31818 | MHz |
| $f_{in\_ref}$ | X1/X2 Input Reference Frequency | Nominal VDD supply voltage, process and temperature. Range guaranteed by design. | TBD | TBD | MHz |
| $T_{rise}$ | Rise Time | 0.4V to 2.4V; 15 pF load | 0.5 | 2 | ns |
| $T_{fall}$ | Fall Time | 2.4V to 0.4V; 15 pF load | 0.5 | 2 | ns |
| D | Duty Cycle | | 45 | 55 | % |

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $T_{trans}$ | Transition Time | From VDD and VDDA to 1st crossing of target frequency. | | 5 | ms |
| Ts | Settling Time | From 1st crossing to ±1% target frequency. | | 5 | ms |
| $T_{STAB}$ | Clock Stabilization | From VDD and VDDA to ±1% target frequency. | | 100 | ms |
| $T_{CPU\_JC-C}$ | CPUCLK Cycle-To-Cycle Jitter | See Note 2. | | 150 | ps |
| $T_{CPU\_JP}$ | CPUCLK Period Jitter | See Note 2. | | 150 | ps |
| $T_{RAM\_JC-C}$ | RAMCLK Cycle-To-Cycle Jitter | See Note 2. | | 150 | ps |
| $T_{RAM\_JP}$ | RAMCLK Period Jitter | See Note 2. | | 150 | ps |
| $T_{PCI\_JC-C}$ | PCICLK Cycle-To-Cycle Jitter | See Note 2. | | 250 | ps |
| $T_{USB\_JC-C}$ | USBCLK Cycle-To-Cycle Jitter | See Note 2. | | 250 | ps |
| $T_{CLK25\_JP}$ | CLK25 Cycle-To-Cycle Jitter | See Note 2. | | 250 | ps |
| $T_{REF\_JP}$ | REFOUT Cycle-To-Cycle Jitter | See Note 2. | | 500 | ps |
| $T_{skew\_bank}$ | Output-To-Output Skew | Skew between outputs of same group, equally loaded and terminated. See Note 3. | | 100 | Ps |
| $F_{TOL}$ | Output Frequency Tolerance | Based on crystal reference with 100 ppm frequency stability | | 300 | ppm |

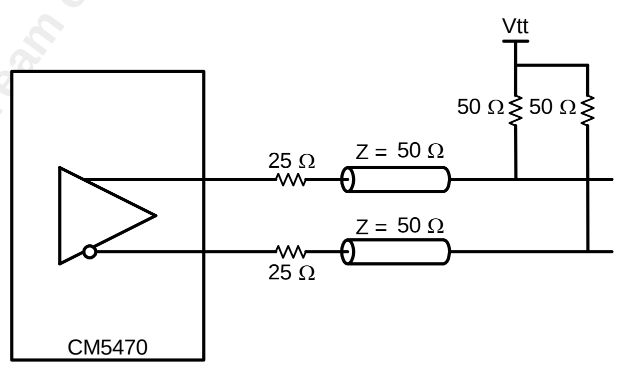
**Notes On A.C. Characteristics**

1. The output frequency tolerance will match the frequency tolerance of the crystal or reference clock applied to the X1 input.
2. Refer to the “Cycle-to-Cycle and Period Jitter Description” section for a visual representation of cycle-to-cycle and period jitter.
3. The output groups consist of the following signals:
   a) CPUCLK1-3
   b) RAMCLKA/B/C1-2_P (SSTL_2 mode). See ‘SSTL_2 Skew Definitions’ figure part b).
   c) RAMCLKA/B/C1-2 differential output pair (SSTL_2 mode). See ‘SSTL_2 Skew Definitions’ figure part c).
   d) PCICLK1-4

## SSTL_2 Skew Definitions



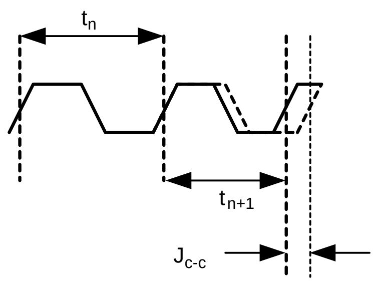

## SSTL_2 Test Load Circuit




SSTL_2 Output Load Test Circuit

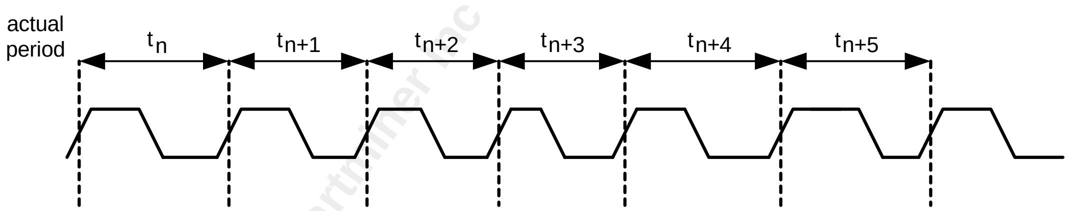
## Cycle-To-Cycle and Period Jitter Description

**Cycle-To-Cycle Jitter**: The difference in period length between two adjacent cycles. Over 10,000 adjacent cycle groups are sampled and measured to determine the largest cycle-to-cycle variation of the period length.




$$J_{c\text{-}c} = \left| t_n - t_{n+1} \right|$$

**Period Jitter:** The deviation from the mean clock period derived from a random sample of cycles.




$$J_{period}(x) = \left| t_x - \frac{\sum \left[ t_n + t_{n+1} + t_{n+2} + \cdots \right]}{\text{number of periods in sample}} \right|$$

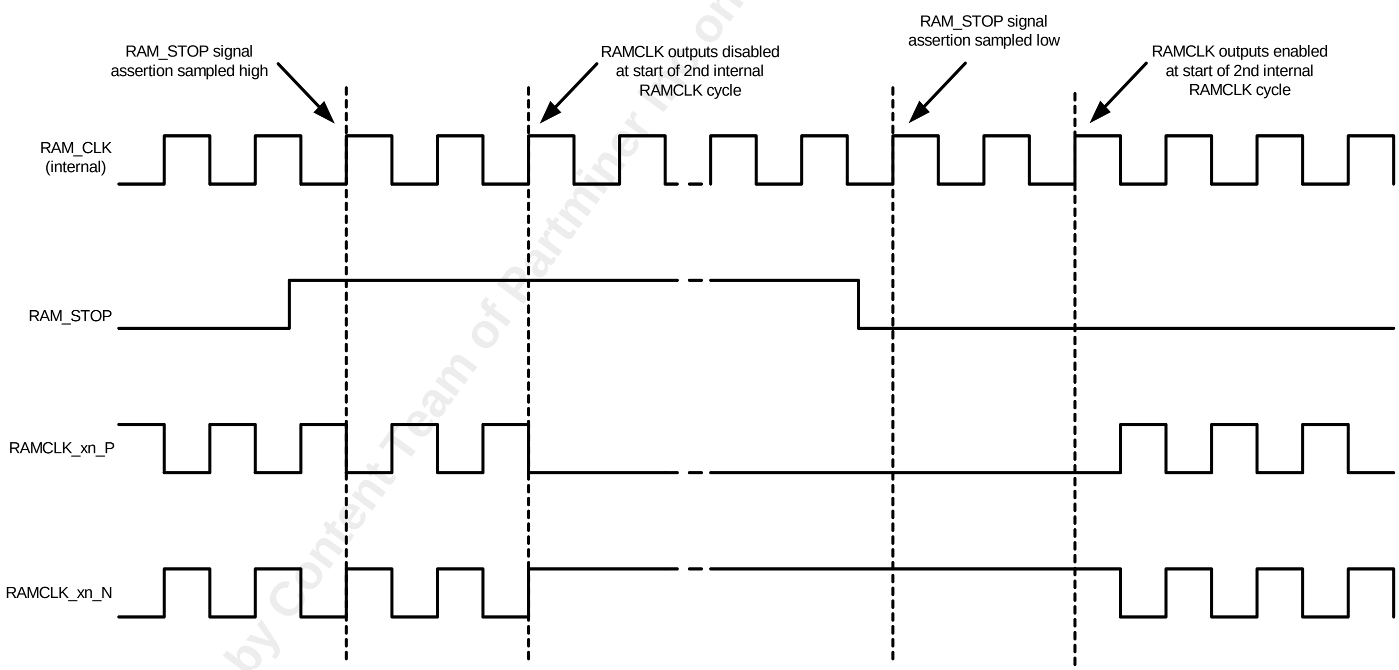
## RAM_STOP Timing

The RAM_STOP signal is an asynchronous input that controls the RAMCLK_An_P/N, RAMCLK_Bn_P/N and RAMCLK_Cn_P/N clock outputs. The internal RAM_STOP signal is synchronized to the internal RAM_CLK clock signal. When the RAM_STOP signal is logic 0, the RAMCLK_xn outputs will be generated by the CM5470. When the RAM_STOP signal is logic 1, the RAMCLK_xn outputs are set as follows:

1) LVTTL mode: RAMCLK_xn_P is forced to logic 0 (RAMCLK_xn_N is high-impedance)
2) SSTL_2 mode: RAMCLK_xn_P is forced to logic 0. RAMCLK_xn_N is forced to logic 1.

There is one complete RAMCLK_xn cycle on all outputs before reaching the static state. The latency from RAM_STOP assertion/de-assertion detection to RAMCLK_xn off/on is two clock cycles maximum. Refer to the figure ‘RAM_STOP Timing Diagram’ for a visual representation of the RAM_STOP function.

### RAM_STOP Timing Digram



# GEN-M7K-56-000 Data Sheet

## Functional Options

The CM5470 has several control inputs. These inputs select the functional mode of the device, as explained in the following tables.

### CPUCLK and RAMCLK Output Frequency Options

| OFS[2:0] | Freq. (MHz) |
|---|---|
| 000 | 50.00 |
| 001 | 66.67 |
| 010 | 83.33 |
| 011 | 100.00 |
| 100 | 125.00 |
| 101 | 133.33 |
| 110 | 166.67 |
| 111 | 200.00 |

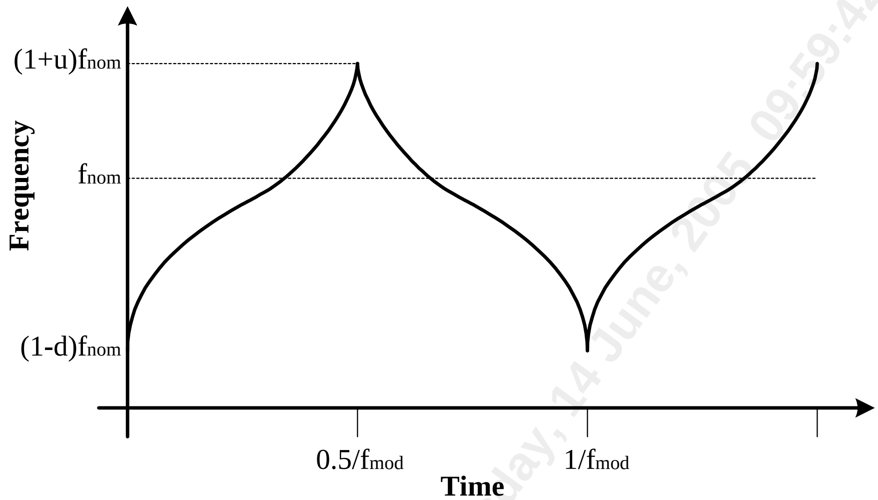
### USBCLK Output Frequency Options

| USBFS[2:0] | Freq. (MHz) |
|---|---|
| 00 | 12.00 |
| 01 | 24.00 |
| 10 | 30.00 |
| 11 | 48.00 |

### Spread Spectrum Algorithm Options

| | | Spread Spectrum Algorithm | | |
|---|---|---|---|---|
| SPREAD1 | SPREAD0 | $f_{mod}$ | d | u |
| 0 | 0 | 31 kHz | 0.50% | 0.00% |
| 0 | 1 | 31 kHz | 1.00% | 0.00% |
| 1 | 0 | 31 kHz | 1.30% | 0.00% |
| 1 | 1 | disabled | | |

**Spread Spectrum Algorithm Diagram**




## Power Considerations

### Calculating Maximum Operating Power

The maximum operating power is determined by the thermal limits of the device, as specified in the Thermal Information section. Based on the $\theta_{JA}$ value of 56°C/W and the maximum long term junction temperature of 105°C (case temperature of 102°C), the CM5470 can support a power consumption of 625 mW at 70°C and 1.4 W at 25°C. Contact PMC-Sierra applications support at apps@pmc-sierra.com for information on power consumption estimates and thermal limits.

### Minimizing Total Operating Power

#### Power Down Unused Output Clocks

On the CM5470, if certain clock outputs are not being used they can be powered down by grounding the associated power supply pin. For example, if an application does not require the CLK25 output, then the VDD_CLK25 pin should be tied directly to ground to minimize power consumption.Ω

#### Use 2.5V Signaling

I/O power is proportional to the square of the voltage swing based on the following equation:

$$P_{IO} = \sum fCV^2 \quad ;\text{ where } C \text{ is capacitive load}$$

$$f \text{ is frequency of operation}$$

$$V \text{ is signal voltage swing}$$

# GEN-M7K-56-000 Data Sheet

Therefore, choosing 2.5V (rather than 3.3V) LVTTL output levels wherever possible can reduce power consumption of that output significantly.

### Reduce Signal Loading

As seen in the equations above, the I/O power is proportional to the capacitive loading on the signal. Therefore, reducing the capacitive loading on a signal will reduce the power consumption of that output.

### If You Need Further Assistance

If you need assistance to calculate the expected operating power for a specific application, please contact PMC-Sierra's Applications engineering team at apps@pmc-sierra.com.

## Thermal Information

### Junction Temperature

| | | |
|---|---|---|
| CM5470-AC | Maximum Junction Temperature for Long Term Reliability | 105C |
| CM5470-AGC | Maximum Junction Temperature for Long Term Reliability | 105C |

### Theta Ja vs. Airflow

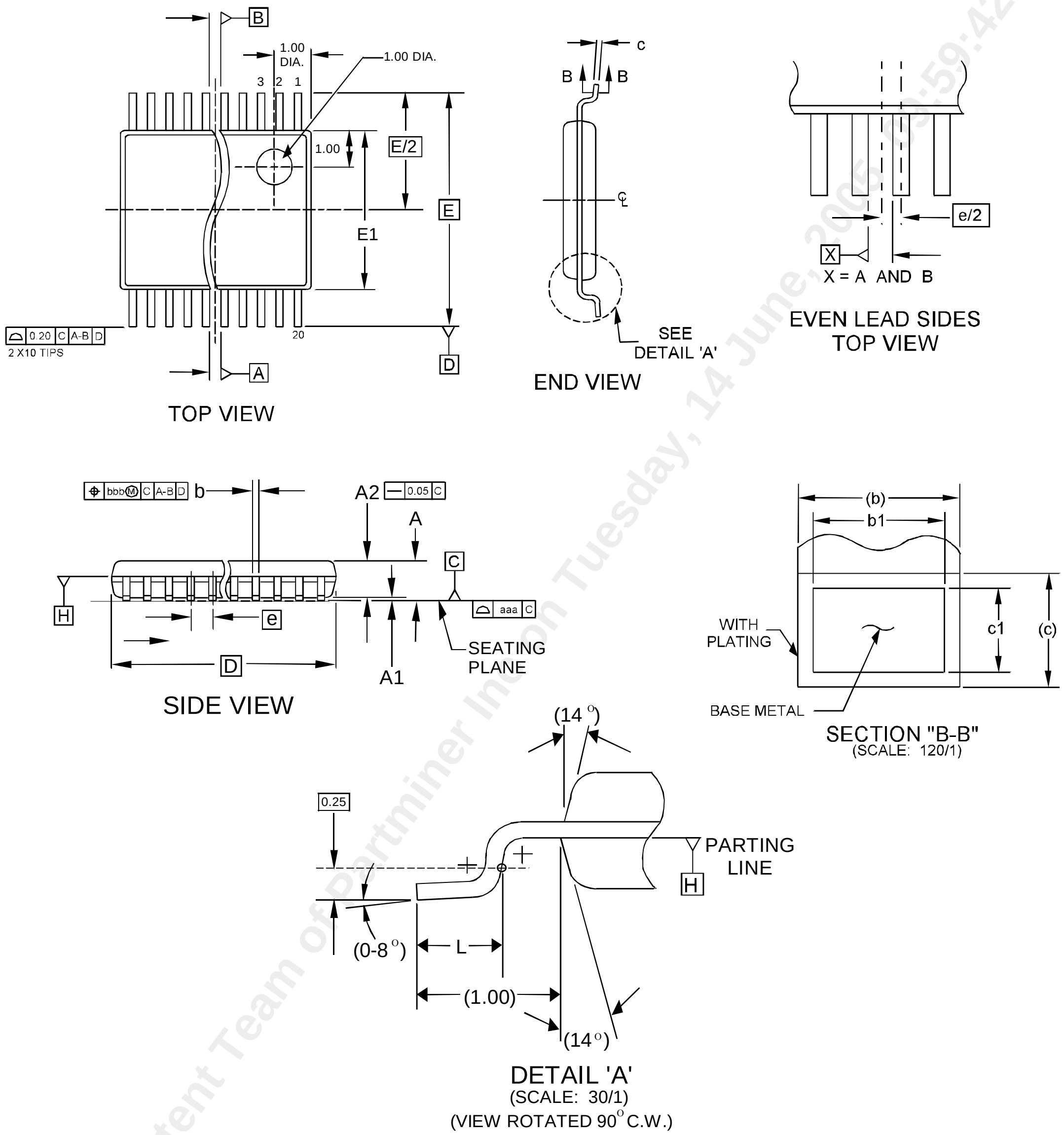
| | | | | Forced Air (Linear Feet per Minute) | |
|---|---|---|---|---|---|
| **Part No.** | **Case Temp.** | **Theta J-A at 2.5 Watts** | **Conv** | **200** | 400 |
| CM5470-AC | 0C to 70C | JEDEC Board | 56 | 50 | 48 |
| CM5470-AGC | 0C to 70C | JEDEC Board | 56 | 50 | 48 |

### Theta JT, JB

| Part No. | Case Temperature | Theta JT | Theta JB |
|---|---|---|---|
| CM5470-AC | 0C to +70C | 30.3 | 64.7 |
| CM5470-AGC | 0C to +70C | 30.3 | 64.7 |

# GEN-M7K-56-000 Data Sheet

## 56-Pin TSSOP Packaging Option




| PACKAGE TYPE : 56 Pin THIN SHRINK SMALL OUTLINE PACKAGE- TSSOP | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BODY SIZE : 6.1 X 14.0 x 1.10 MM | | | | | | | | | | | | | |
| Dim. | A | A1 | A2 | D | E | E1 | b | b1 | c | c1 | e | L | aaa | bbb |
| Min. | - | 0.05 | 0.85 | 13.90 | - | 6.00 | 0.17 | 0.17 | 0.09 | 0.09 | - | 0.50 | - | - |
| Nom. | - | - | 0.90 | 14.00 | 8.10 BSC | 6.10 | - | 0.20 | - | 0.127 | 0.50 BSC | 0.60 | 0.10 | 0.08 |
| Max. | 1.10 | 0.15 | 0.95 | 14.10 | - | 6.20 | 0.27 | 0.23 | 0.20 | 0.16 | - | 0.70 | - | - |

NOTE: ALL DIMENSIONS IN MILLILETERS
THIS PART IS COMPLIANT WITH JEDEC SPECIFICATIONS MO-153 VARIATION EE

# GEN-M7K-56-000 Data Sheet

## Ordering Information

### Ordering Information

| Part No. | Description |
|---|---|
| CM5470-AC | 56-pin Thin Shrink Small Outline Package (TSSOP) |
| CM5470-AGC | “Green” lead-free 56-pin Thin Shrink Small Outline Package (TSSOP) |