LMP7731

LMP7731 2.9 nV/sqrt(Hz) Low Noise, Precision, RRIO Amplifier

Literature Number: SNOSAT6D

National Semiconductor

May 20, 2009

LMP7731

2.9 nV/sqrt(Hz) Low Noise, Precision, RRIO Amplifier

General Description

The LMP7731 is a single, low noise, rail-to-rail input and output, low voltage amplifier. The LMP7731 is part of the LMP® precision amplifier family and is ideal for precision and low noise applications with low voltage requirements.

This operational amplifier offers low voltage noise of 2.9 nV/√Hz with a 1/f corner of only 3 Hz. The LMP7731 has bipolar input stages with a bias current of only 1.5 nA. This low input bias current, complemented by the very low level of voltage noise, makes the LMP7731 an excellent choice for photometry applications.

The LMP7731 provides a wide GBW of 22 MHz while consuming only 2 mA of current. This high gain bandwidth along with the high open loop gain of 130 dB enables accurate signal conditioning in applications with high closed loop gain requirements.

The LMP7731 has a supply voltage range of 1.8V to 5.5V, making it an ideal choice for battery operated portable applications.

The LMP7731 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC packages.

Features

(Typical values, T_A = 25°C, V_S = 5V)

- Input voltage noise
  — f = 3 Hz   3.3 nV/√Hz
  — f = 1 kHz   2.9 nV/√Hz
- CMRR   130 dB
- Open loop gain   130 dB
- GBW   22 MHz
- Slew rate   2.4 V/µs
- THD @ f = 10 kHz, A_V = +1, R_L = 2 kΩ   0.001%
- Supply current per channel   2.2 mA
- Supply voltage range   1.8V to 5.5V
- Operating temperature range   −40°C to 125°C
- Input bias current   ±1.5 nA
- RRIO

Applications

- Gas analysis instruments
- Photometric instrumentation
- Medical instrumentation

Typical Performance Characteristics

Input Voltage Noise vs. Frequency

20175261

Input Current Noise vs. Frequency

20175262
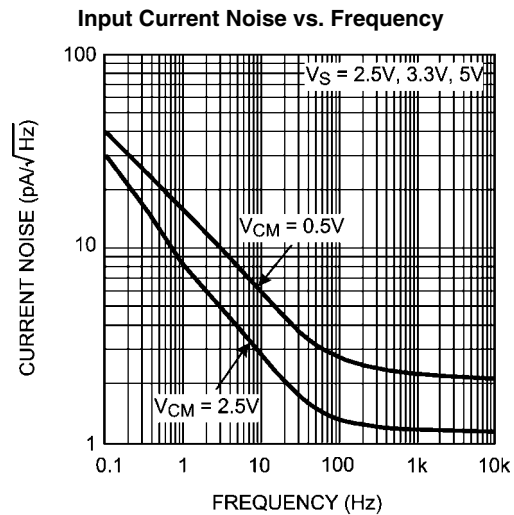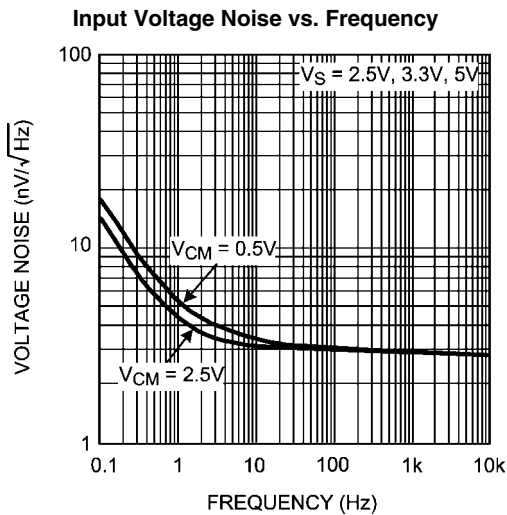
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
Inputs pins only	2000V
All other pins	2000V
Machine Model	200V
Charge Device Model	1000V
V_{IN} Differential	±2V
Supply Voltage ($V_S = V^+ - V^-$)	6.0V

Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 3)	+150°C max
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range	−40°C to 125°C
Supply Voltage ($V_S = V^+ - V^-$)	1.8V to 5.5V
Package Thermal Resistance (θ_{JA})	
5-Pin SOT-23	265°C/W
8-Pin SOIC	190°C/W

2.5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V+ = 2.5V, V− = 0V, V_{CM} = V+/2, R_L >10 kΩ to V+/2. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage (Note 7)	V_{CM} = 2.0V		±9	±500 **±600**	µV
		V_{CM} = 0.5V		±9	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 2.0V		±0.5	±5.5	µV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 2.0V		±1	±30 **±45**	nA
		V_{CM} = 0.5V		±12	±50 **±75**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V		±1	±50 **±75**	nA
		V_{CM} = 0.5V		±11	±60 **±80**	
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 2.0V		0.0474		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V	101	120		dB
		0.23V ≤ V_{CM} ≤ 0.7V	**89**			
		1.5V ≤ V_{CM} ≤ 2.35V	105	129		
		1.5V ≤ V_{CM} ≤ 2.27V	**99**			
PSRR	Power Supply Rejection Ratio	2.5V ≤ V+ ≤ 5V	111 **105**	129		dB
		1.8V ≤ V+ ≤ 5.5V		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		2.5	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V+/2 V_{OUT} = 0.5V to 2.0V	112 **104**	130		dB
		R_L = 2 kΩ to V+/2 V_{OUT} = 0.5V to 2.0V	109 **90**	119		

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V+/2		4	50 **75**	mV from either rail
		R_L = 2 kΩ to V+/2		13	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V+/2		6	50 **75**	
		R_L = 2 kΩ to V+/2		9	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V+/2 V_{IN} (diff) = 100 mV	22 **12**	31		mA
		Sinking, V_{OUT} = V+/2 V_{IN} (diff) = −100 mV	15 **10**	44		
I_S	Supply Current (Per Channel)	V_{CM} = 2.0V		2.0	2.7 **3.4**	mA
		V_{CM} = 0.5V		2.3	3.1 **3.9**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V+/2, V_O = 2 V_{PP}		2.4		V/µs
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V+/2		21		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		14		dB
$Φ_M$	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		60		deg
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
THD+N	Total Harmonic Distortion + Noise	A_V = 1, f = 1 kHz, Amplitude = 1V		0.002		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 2.0V		3		nV/$\sqrt{Hz}$
		f = 1 kHz, V_{CM} = 0.5V		3		
	Input Voltage Noise	0.1 Hz to 10 Hz		75		nV$_{PP}$
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 2.0V		1.1		pA/$\sqrt{Hz}$
		f = 1 kHz, V_{CM} = 0.5V		2.3		

3.3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V+ = 3.3V, V− = 0V, V_{CM} = V+/2, R_L > 10 kΩ to V+/2. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage (Note 7)	V_{CM} = 2.5V		±6	±500 **±600**	µV
		V_{CM} = 0.5V		±6	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 2.5V		±0.5	±5.5	µV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 2.5V		±1.5	±30 **±45**	nA
		V_{CM} = 0.5V		±13	±50 **±77**	
I_{OS}	Input Offset Current	V_{CM} = 2.5V		±1	±50 **±70**	nA
		V_{CM} = 0.5V		±11	±60 **±80**	

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 2.5V		0.048		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V 0.23V ≤ V_{CM} ≤ 0.7V	101 **89**	120		dB
		1.5V ≤ V_{CM} ≤ 3.15V 1.5V ≤ V_{CM} ≤ 3.07V	105 **99**	130		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V+ ≤ 5.0V	111 **105**	129		dB
		1.8V ≤ V+ ≤ 5.5V		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		3.3	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V+/2 V_{OUT} = 0.5V to 2.8V	112 **104**	130		dB
		R_L = 2 kΩ to V+/2 V_{OUT} = 0.5V to 2.8V	110 **92**	119		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V+/2		5	50 **75**	mV from either rail
		R_L = 2 kΩ to V+/2		14	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V+/2		9	50 **75**	
		R_L = 2 kΩ to V+/2		13	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V+/2 V_{IN} (diff) = 100 mV	28 **22**	45		mA
		Sinking, V_{OUT} = V+/2 V_{IN} (diff) = -100 mV	25 **20**	48		
I_S	Supply Current (Per Channel)	V_{CM} = 2.5V		2.1	2.8 **3.5**	mA
		V_{CM} = 0.5V		2.4	3.2 **4.0**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V+/2, V_{OUT} = 2 V_{PP}		2.4		V/µs
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V+/2		22		MHz
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		14		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		62		deg
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
THD+N	Total Harmonic Distortion + Noise	A_V = 1, f = 1 kHz, Amplitude = 1V,		0.002		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 2.5V		2.9		nV/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		65		nV_{PP}
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 2.5V		1.1		pA/√Hz
		f = 1 kHz, V_{CM} = 0.5V		2.1		

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V+/2, R_L > 10 kΩ to V+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage (Note 7)	V_{CM} = 4.5V		±6	±500 **±600**	µV
		V_{CM} = 0.5V		±6	±500 **±600**	
TCV_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 4.5V		±0.5	±5.5	µV/°C
		V_{CM} = 0.5V		±0.2	±5.5	
I_B	Input Bias Current	V_{CM} = 4.5V		±1.5	±30 **±50**	nA
		V_{CM} = 0.5V		±14	±50 **±85**	
I_{OS}	Input Offset Current	V_{CM} = 4.5V		±1	±50 **±70**	nA
		V_{CM} = 0.5V		±11	±65 **±80**	
TCI_{OS}	Input Offset Current Drift	V_{CM} = 0.5V and V_{CM} = 4.5V		0.0482		nA/°C
CMRR	Common Mode Rejection Ratio	0.15V ≤ V_{CM} ≤ 0.7V / 0.23V ≤ V_{CM} ≤ 0.7V	101 **89**	120		dB
		1.5V ≤ V_{CM} ≤ 4.85V / 1.5V ≤ V_{CM} ≤ 4.77V	105 **99**	130		
PSRR	Power Supply Rejection Ratio	2.5V ≤ V+ ≤ 5V	111 **105**	129		dB
		1.8V ≤ V+ ≤ 5.5V		117		
CMVR	Common Mode Voltage Range	Large Signal CMRR ≥ 80 dB	0		5	V
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ to V+/2 V_{OUT} = 0.5V to 4.5V	112 **104**	130		dB
		R_L = 2 kΩ to V+/2 V_{OUT} = 0.5V to 4.5V	110 **94**	119		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to V+/2		8	50 **75**	mV from either rail
		R_L = 2 kΩ to V+/2		24	50 **75**	
	Output Voltage Swing Low	R_L = 10 kΩ to V+/2		9	50 **75**	
		R_L = 2 kΩ to V+/2		23	50 **75**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = V+/2 V_{IN} (diff) = 100 mV	33 **27**	47		mA
		Sinking, V_{OUT} = V+/2 V_{IN} (diff) = -100 mV	30 **25**	49		
I_S	Supply Current (Per Channel)	V_{CM} = 4.5V		2.2	3.0 **3.7**	mA
		V_{CM} = 0.5V		2.5	3.4 **4.2**	
SR	Slew Rate	A_V = +1, C_L = 10 pF, R_L = 10 kΩ to V+/2, V_{OUT} = 2 V_{PP}		2.4		V/µs
GBW	Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ to V+/2		22		MHz

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
G_M	Gain Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		12		dB
Φ_M	Phase Margin	C_L = 20 pF, R_L = 10 kΩ to V+/2		65		deg
R_{IN}	Input Resistance	Differential Mode		38		kΩ
		Common Mode		151		MΩ
THD+N	Total Harmonic Distortion + Noise	A_V = 1, f = 1 kHz, Amplitude = 1V		0.001		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz, V_{CM} = 4.5V		2.9		nV/$\sqrt{\text{Hz}}$
		f = 1 kHz, V_{CM} = 0.5V		2.9		
	Input Voltage Noise	0.1 Hz to 10 Hz		78		nV_{PP}
i_n	Input Referred Current Noise Density	f = 1 kHz, V_{CM} = 4.5V		1.1		pA/$\sqrt{\text{Hz}}$
		f = 1 kHz, V_{CM} = 0.5V		2.2		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute maximum Ratings indicate junction temperature limits beyond which the device maybe permanently degraded, either mechanically or electrically.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: All limits are guaranteed by testing, statistical analysis or design.

Note 7: Ambient production test is performed at 25°C with a variance of ±3°C.

Connection Diagrams

5-Pin SOT-23

OUT 1   5 V+
V− 2
+IN 3   4 -IN

20175202

Top View

8-Pin SOIC

N/C 1   8 N/C
-IN 2   7 V+
+IN 3   6 OUT
V− 4   5 N/C

20175203

Top View
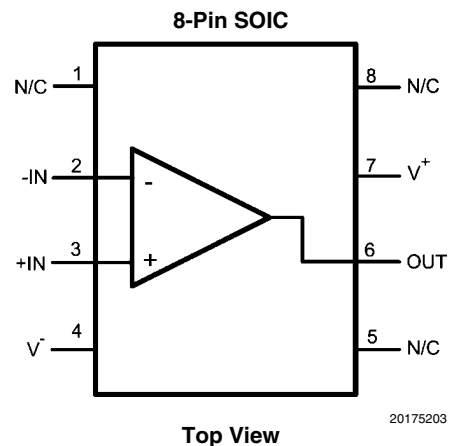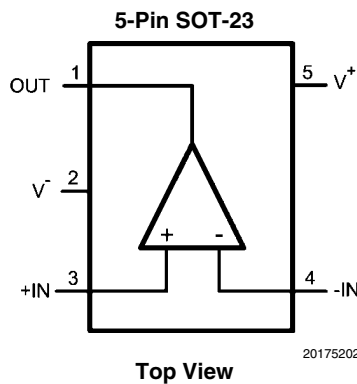
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LMP7731MF	AY3A	1k Units Tape and Reel	MF05A
	LMP7731MFE		250 Units Tape an Reel	
	LMP7731MFX		3k Units Tape and Reel	
8-Pin SOIC	LMP7731MA	LMP7731MA	95 Units/Rail	M08A
	LMP7731MAX		2.5k Tape and Reel	

Typical Performance Characteristics
Unless otherwise noted: $T_A = 25°C$, $R_L > 10\ k\Omega$, $V_{CM} = V_S/2$.

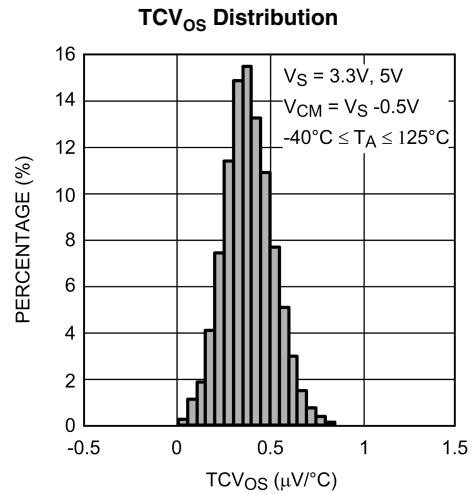**Offset Voltage Distribution**
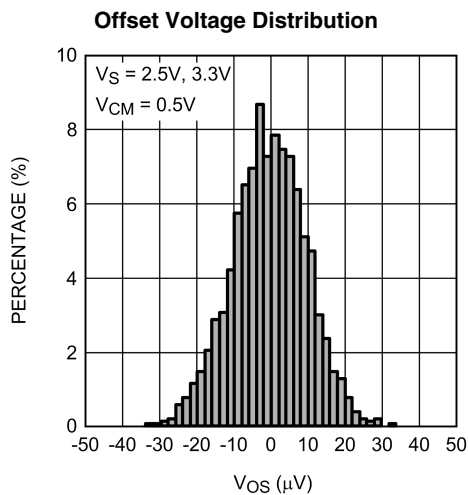

$V_S = 2.5V$
$V_{CM} = 2V$

20175238

TCV$_{OS}$ Distribution

$V_S = 2.5V$
$V_{CM} = 2V$
$-40°C \leq T_A \leq 125°C$

20175234

Offset Voltage Distribution

$V_S = 3.3V, 5V$
$V_{CM} = V_S -0.5V$

20175239

TCV$_{OS}$ Distribution

$V_S = 3.3V, 5V$
$V_{CM} = V_S -0.5V$
$-40°C \leq T_A \leq 125°C$

20175236

Offset Voltage Distribution

$V_S = 2.5V, 3.3V$
$V_{CM} = 0.5V$

20175240

TCV$_{OS}$ Distribution

$V_S = 2.5V$
$V_{CM} = 0.5V$
$-40°C \leq T_A \leq 125°C$
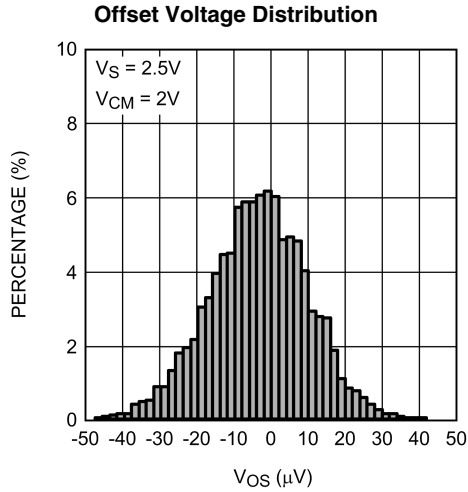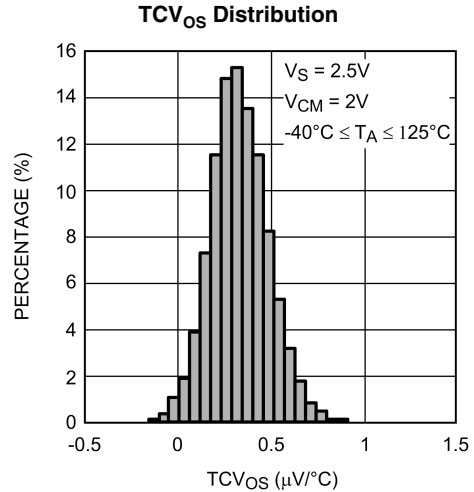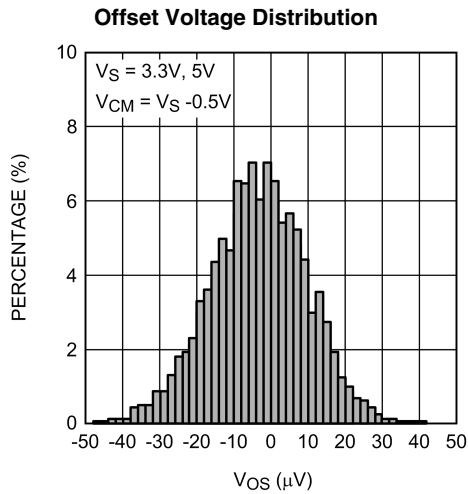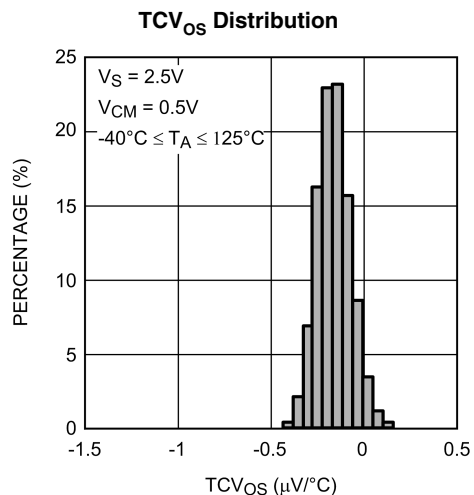
20175235

Offset Voltage Distribution
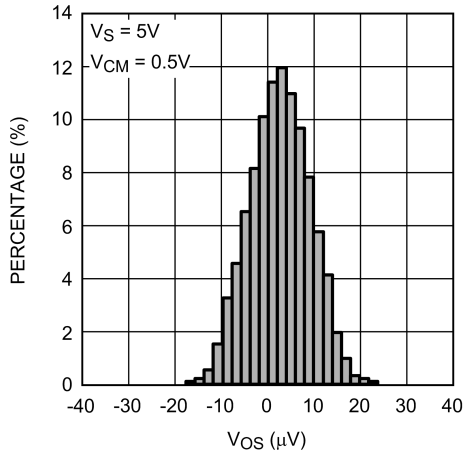
20175241

TCV$_{OS}$ Distribution
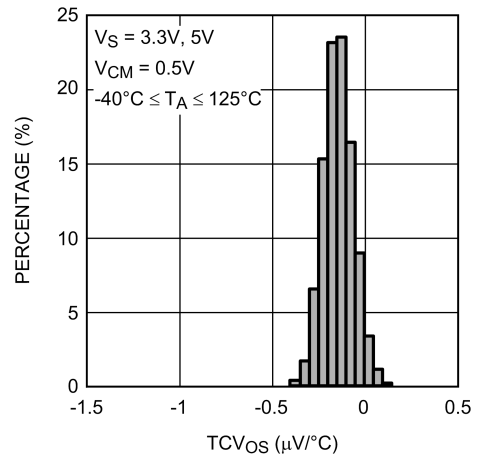
20175237

Offset Voltage vs. Temperature
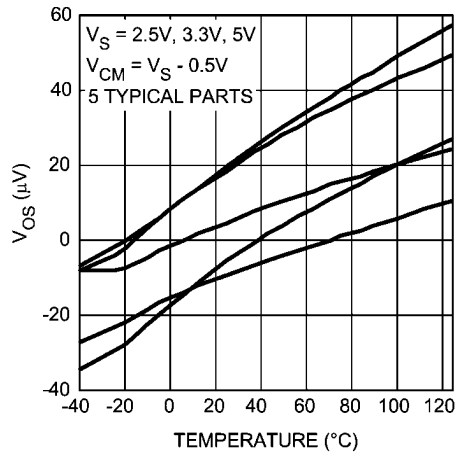
20175251

Offset Voltage vs. Temperature
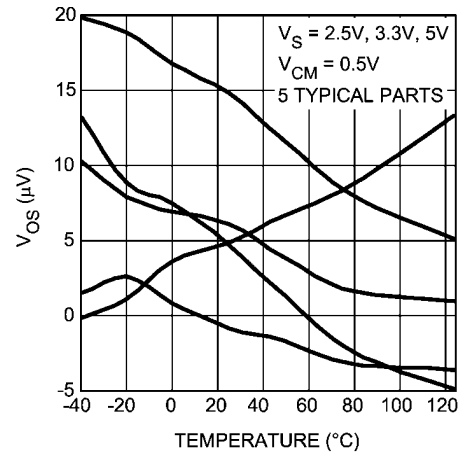
20175252

PSRR vs. Frequency
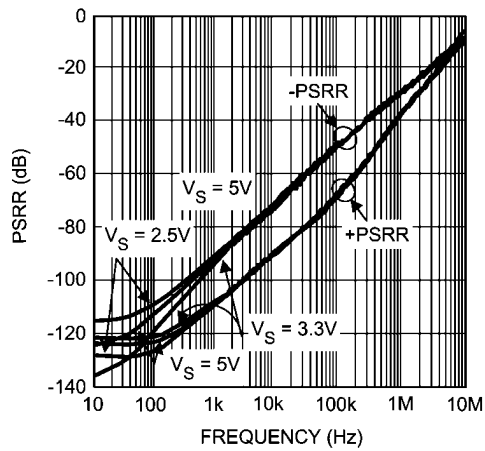
20175229

CMRR vs. Frequency
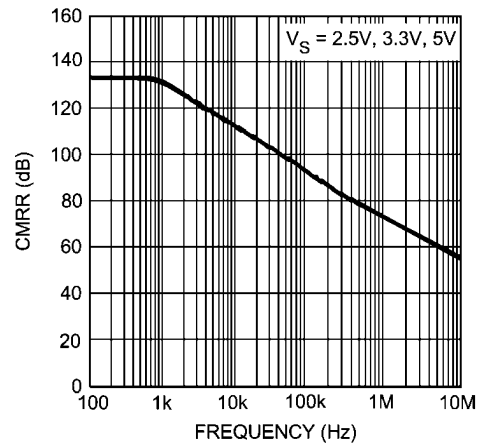
20175256

Offset Voltage vs. Supply Voltage
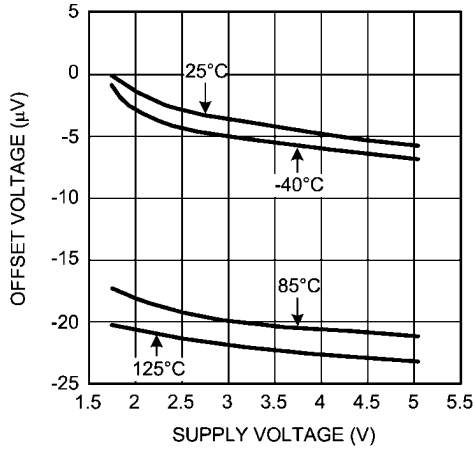
20175242

Offset Voltage vs. V$_{CM}$
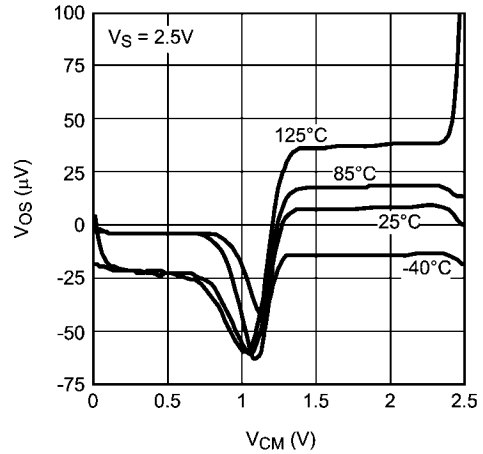
20175243

Offset Voltage vs. V$_{CM}$
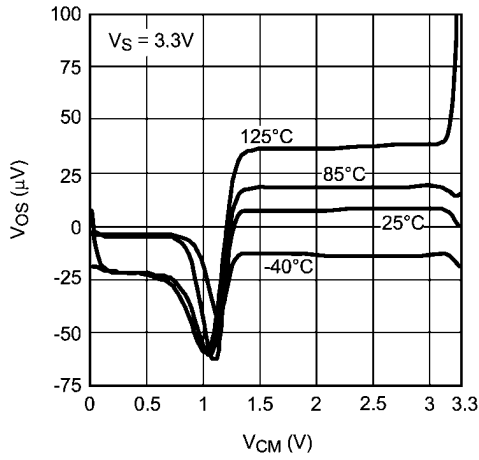
20175244

Offset Voltage vs. V$_{CM}$
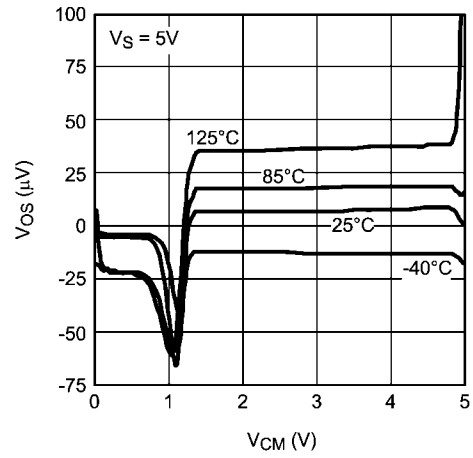
20175245

Input Offset Voltage Time Drift
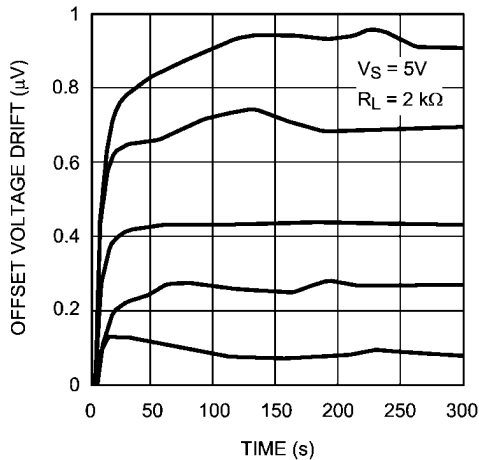
20175230

Slew Rate vs. Supply Voltage
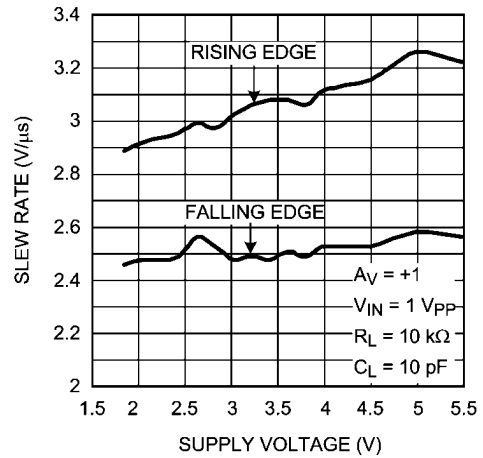
20175220

Time Domain Voltage Noise
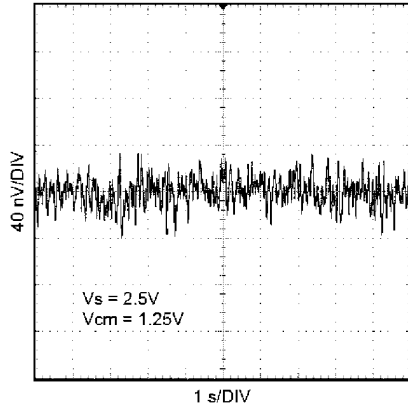
20175269

Time Domain Voltage Noise
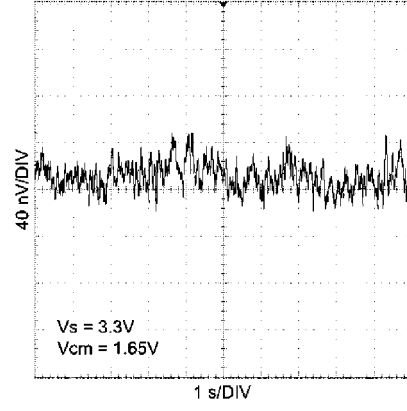
20175267

Time Domain Voltage Noise
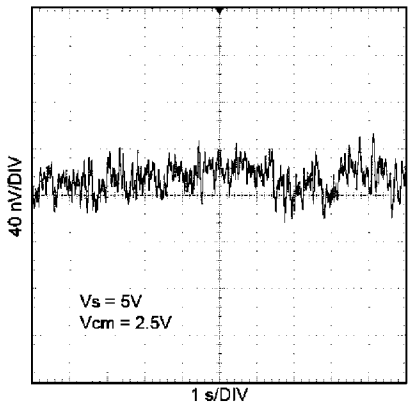
20175268

Output Voltage vs. Output Current
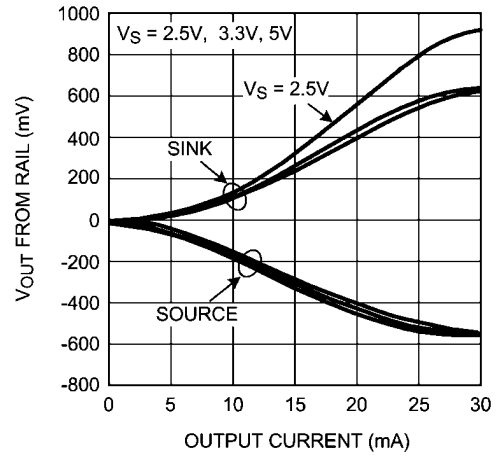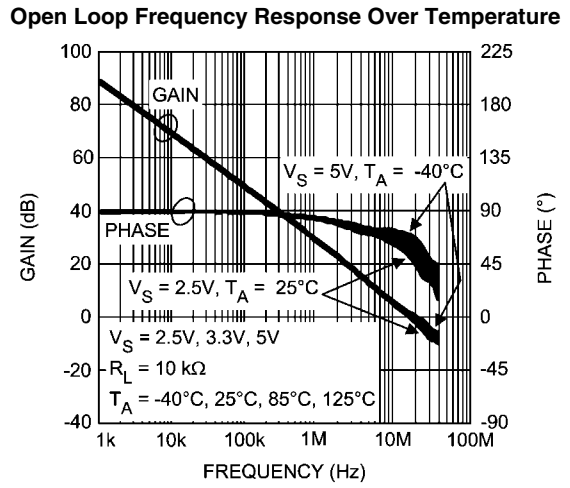

20175259

Input Bias Current vs. V_{CM}
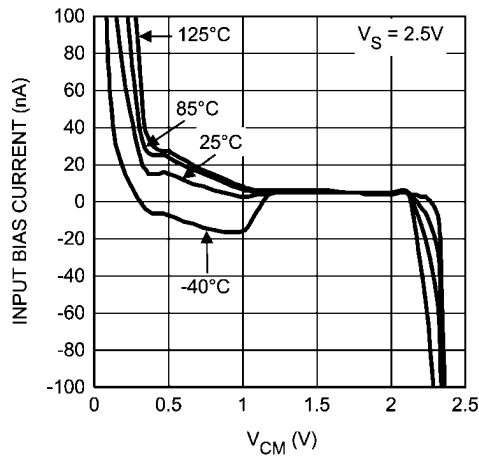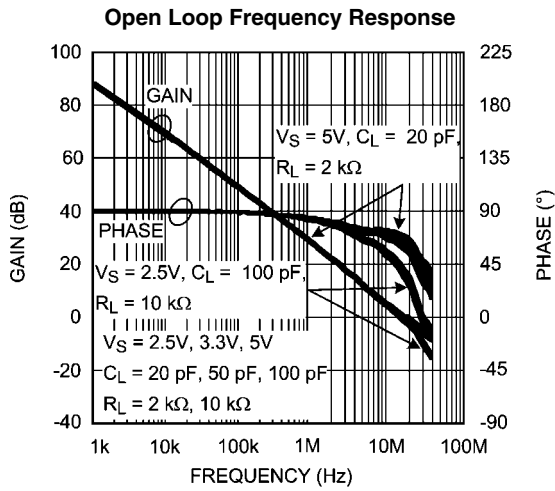

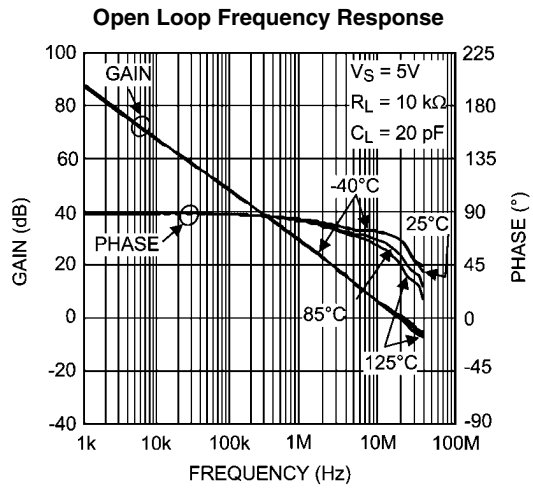20175225

Input Bias Current vs. V_{CM}

20175226

Input Bias Current vs. V$_{CM}$

20175227

Open Loop Frequency Response Over Temperature

20175218

Open Loop Frequency Response

20175219

Open Loop Frequency Response

20175228

THD+N vs. Frequency

20175257

THD+N vs. Output Voltage
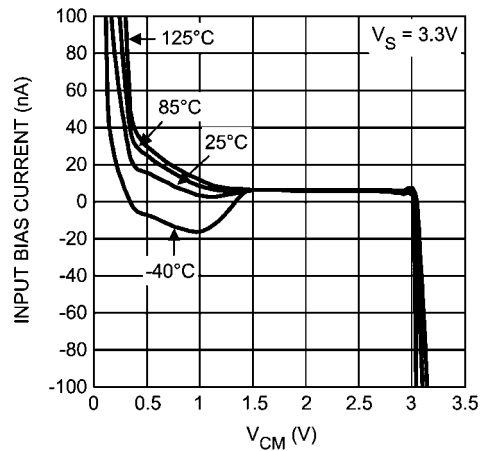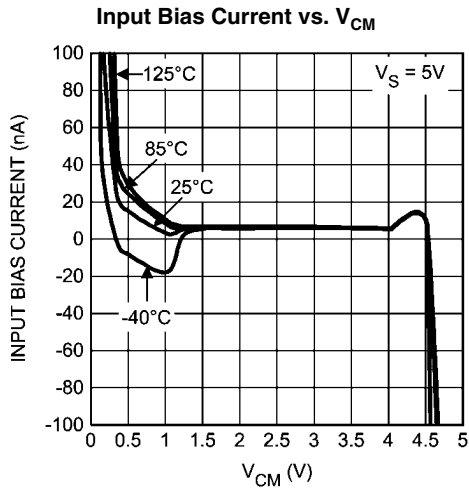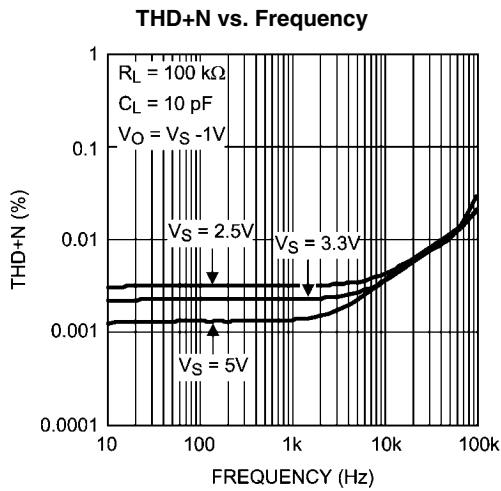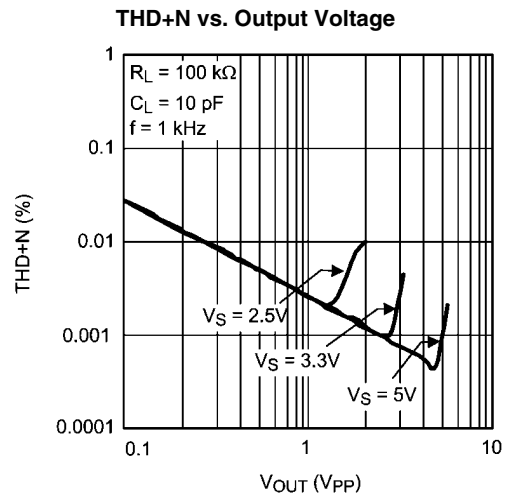
20175258

Large Signal Step Response

$V_S = 5V$
$V_{IN} = 2\ V_{PP}$
$f = 10\ kHz$
$A_V = +1$
$R_L = 10\ k\Omega$
$C_L = 10\ pF$

500 mV/DIV

10 µs/DIV
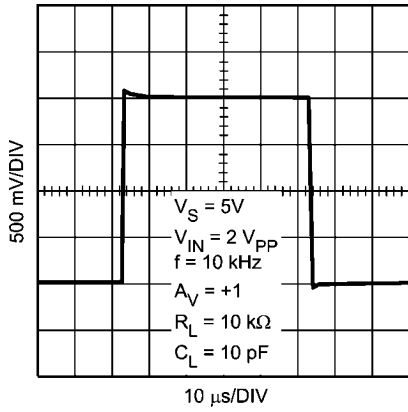
20175222

Small Signal Step Response

$V_S = 5V$
$V_{IN} = 100\ mV_{PP}$
$f = 10\ kHz$
$A_V = +1$
$R_L = 10\ k\Omega$
$C_L = 10\ pF$

20 mV/DIV

10 µs/DIV
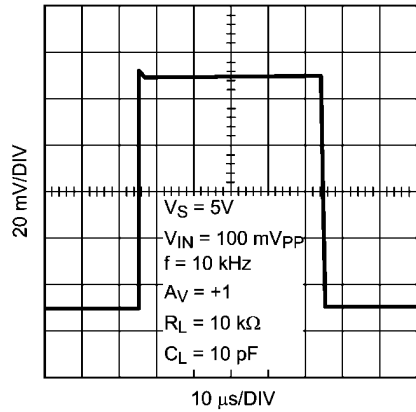
20175221

Large Signal Step Response

$V_S = 5V$
$V_{IN} = 400\ mV_{PP}$
$f = 10\ kHz$
$A_V = +10$
$R_L = 10\ k\Omega$
$C_L = 10\ pF$

1 V/DIV

10 µs/DIV
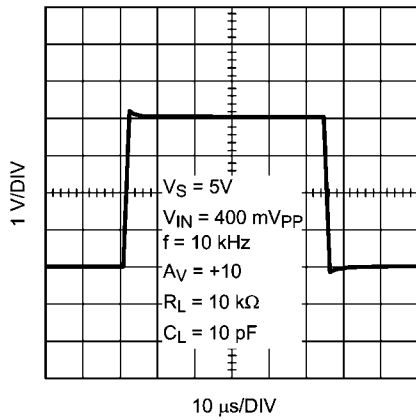
20175224

Small Signal Step Response

$V_S = 5V$
$V_{IN} = 100\ mV_{PP}$
$f = 10\ kHz$
$A_V = +10$
$R_L = 10\ k\Omega$
$C_L = 10\ pF$

200 mV/DIV

10 µs/DIV
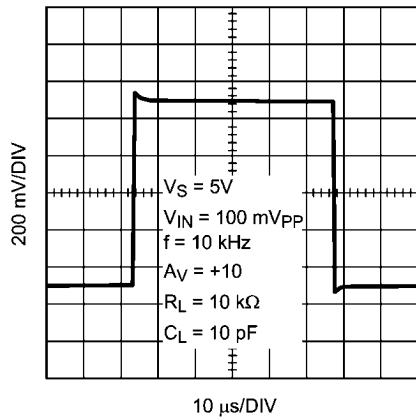
20175223

Supply Current vs. Supply Voltage

SUPPLY CURRENT (mA)

125°C
85°C
25°C
-40°C
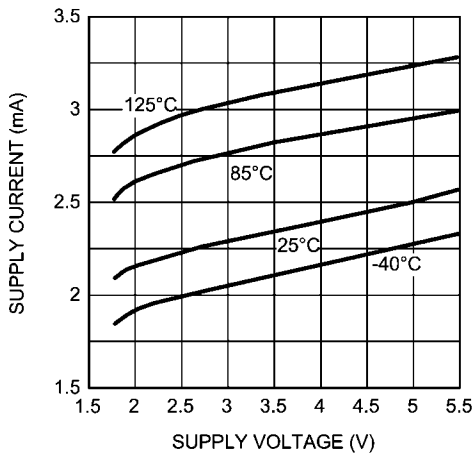
SUPPLY VOLTAGE (V)

20175246

Output Swing High vs. Supply Voltage

$R_L = 2\ k\Omega$

V_{OUT} FROM RAIL (mV)

125°C
85°C
-40°C
25°C
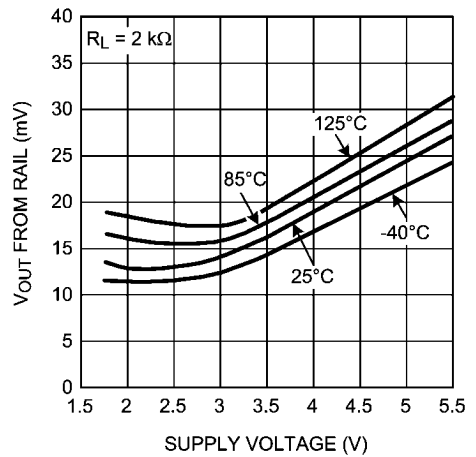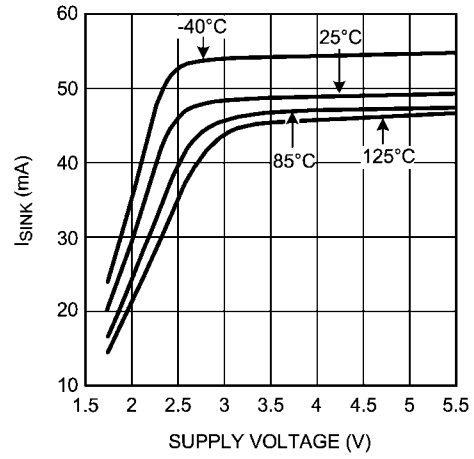
SUPPLY VOLTAGE (V)

20175250

Output Swing Low vs. Supply Voltage
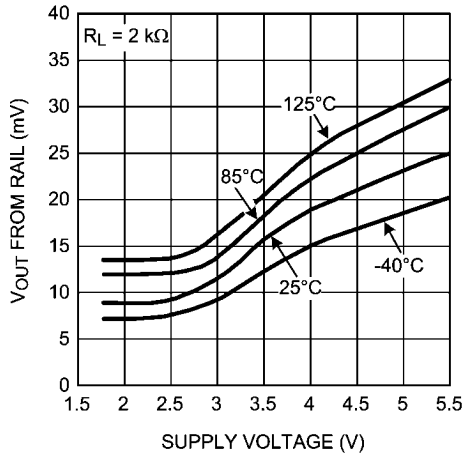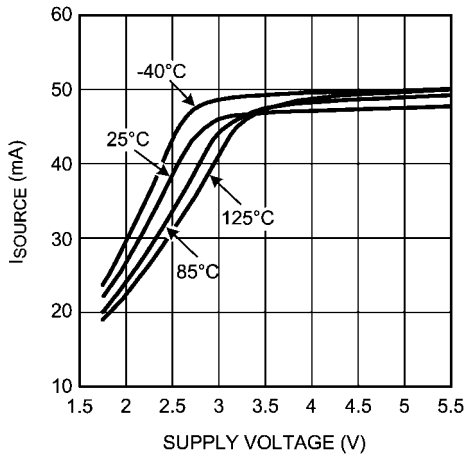

20175249

Sinking Current vs, Supply Voltage

20175247

Sourcing Current vs. Supply Voltage

20175248

Application Information

LMP7731

The LMP7731 is a single, low noise, rail-to-rail input and output, and low voltage amplifier.

The low input voltage noise of only 2.9 nV/√Hz with a 1/f corner at 3 Hz makes the LMP7731 ideal for sensor applications where DC accuracy is of importance.

The LMP7731 has a high gain bandwidth of 22 MHz. This wide bandwidth enables use of the amplifier at higher gain settings while retaining usable bandwidth for the application. This is particularly beneficial when system designers need to use sensors with very limited output voltage range as it allows larger gains in one stage which in turn increases the signal to noise ratio.

The LMP7731 has proprietary input bias cancellation circuitry on the input stages. This allows the LMP7731 to have only about 1.5 nA bias current with a bipolar input stage. This low input bias current, paired with the inherent lower input voltage noise of bipolar input stages makes the LMP7731 an excellent choice for precision applications. The combination of low input bias current, and low input voltage noise enables the user to achieve unprecedented accuracy and higher signal integrity.

National Semiconductor is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data are available for sensitive applications or applications with a constrained error budget.

The LMP7731 is offered in the space saving 5-Pin SOT-23 and 8-Pin SOIC packages. These small packages are ideal solutions for area constrained PC boards and portable electronics.

INPUT BIAS CURRENT CANCELLATION

The LMP7731 has proprietary input bias current cancellation circuitry on their input stages.

The LMP7731 has rail-to-rail input. This is achieved by having two input stages in parallel. *Figure 1* shows only one of the input stages as the circuitry is symmetrical for both stages.

Figure 1 shows that as the common mode voltage gets closer to one of the extreme ends, current I_1 significantly increases. This increased current shows as an increase in voltage drop across resistor R_1 equal to $I_1 * R_1$ on IN+ of the amplifier. This voltage contributes to the offset voltage of the amplifier. When common mode voltage is in the mid-range, the transistors are operating in the linear region and I_1 is significantly small. The voltage drop due to I_1 across R_1 can be ignored as it is orders of magnitude smaller than the amplifier's input offset voltage.

As the common mode voltage gets closer to one of the rails, the offset voltage generated due to I_1 increases and becomes comparable to the amplifiers offset voltage.
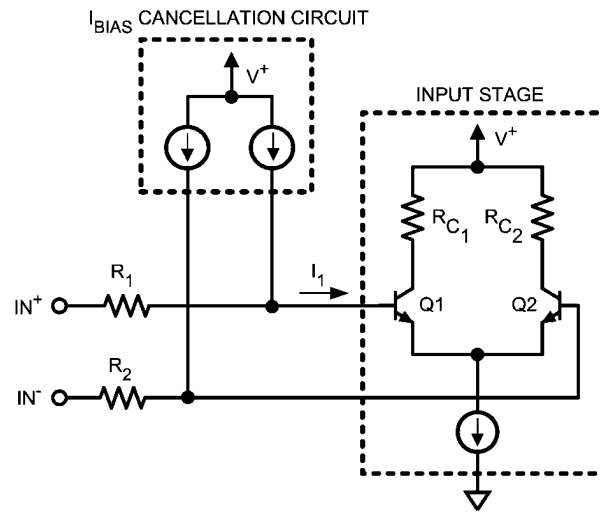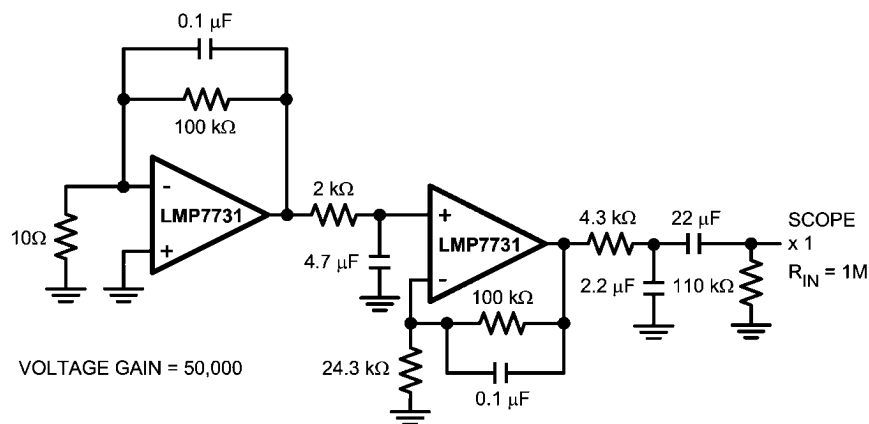

FIGURE 1. Input Bias Current Cancellation

INPUT VOLTAGE NOISE MEASUREMENT

The LMP7731 has very low input voltage noise. The peak-to-peak input voltage noise of the LMP7731 can be measured using the test circuit shown in *Figure 2*


FIGURE 2. 0.1 Hz to 10 Hz Noise Test Circuit

The frequency response of this noise test circuit at the 0.1 Hz corner is defined by only one zero. The test time for the 0.1 Hz to 10 Hz noise measurement using this configuration should not exceed 10 seconds, as this time limit acts as an additional zero to reduce or eliminate the noise contributions of noise from frequencies below 0.1 Hz.

Figure 3 shows typical peak-to-peak noise for the LMP7731 measured with the circuit in *Figure 2* for the LMP7731.
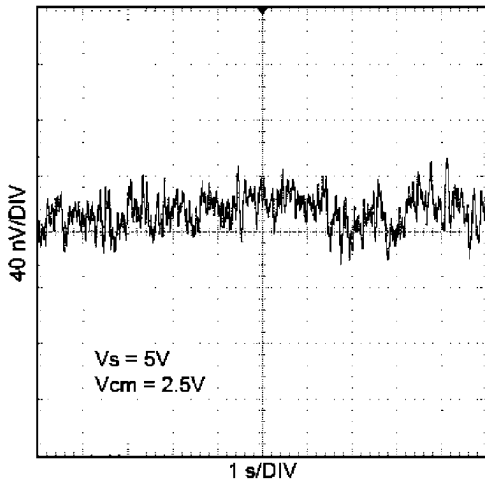
FIGURE 3. 0.1 Hz to 10 Hz Input Voltage Noise

Measuring the very low peak-to-peak noise performance of the LMP7731, requires special testing attention. In order to achieve accurate results, the device should be warmed up for at least five minutes. This is so that the input offset voltage of the op amp settles to a value. During this warm up period, the offset can typically change by a few µV because the chip temperature increases by about 30°C. If the 10 seconds of the measurement is selected to include this warm up time, some of this temperature change might show up as the measured noise. *Figure 4* shows the start-up drift of five typical LMP7731 units.
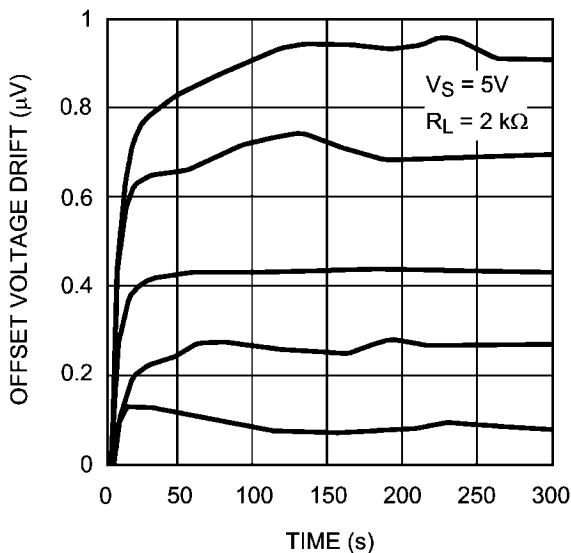

FIGURE 4. Start-Up Input Offset Voltage Drift

During the peak-to-peak noise measurement, the LMP7731 must be shielded. This prevents offset variations due to airflow. Offset can vary by a few nV due to this airflow and that can invalidate measurements of input voltage noise with a magnitude which is in the same range. For similar reasons, sudden motions must also be restricted in the vicinity of the test area. The feed-through which results from this motion could increase the observed noise value which in turn would invalidate the measurement.

DIODES BETWEEN THE INPUTS

The LMP7731 has a set of anti-parallel diodes between the input pins as shown in *Figure 5*. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than the voltage needed to turn on the diodes might cause damage to the diodes. The differential voltage between the input pins should be limited to ±3 diode drops or the input current needs to be limited to ±20 mA.
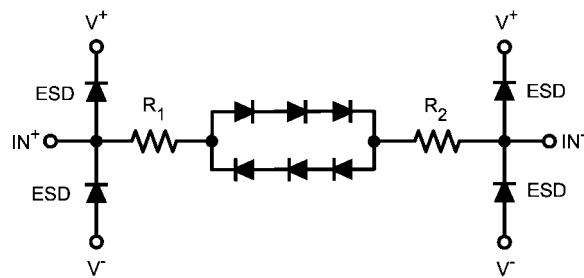

FIGURE 5. Anti-Parallel Diodes between Inputs

DRIVING AN ADC

Analog to Digital Converters, ADCs, usually have a sampling capacitor on their input. When the ADC's input is directly connected to the output of the amplifier a charging current flows from the amplifier to the ADC. This charging current causes a momentary glitch that can take some time to settle. There are different ways to minimize this effect. One way is to slow down the sampling rate. This method gives the amplifier sufficient time to stabilize its output. Another way to minimize the glitch caused by the switch capacitor is to have an external capacitor connected to the input of the ADC. This capacitor is chosen so that its value is much larger than the internal switching capacitor and it will hence provide the voltage needed to quickly and smoothly charge the ADC's sampling capacitor. Since this large capacitor will be loading the output of the amplifier as well, an isolation resistor is needed between the output of the amplifier and this capacitor. The isolation resistor, R_{ISO}, separates the additional load capacitance from the output of the amplifier and will also form a low-pass filter and can be designed to provide noise reduction as well as anti-aliasing. The drawback to having R_{ISO} is that it reduces signal swing since there is some voltage drop across it.
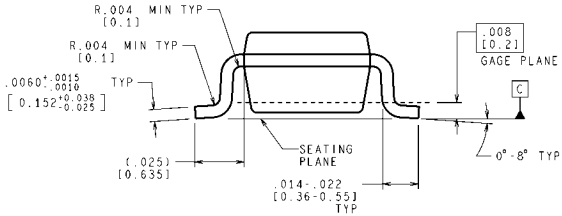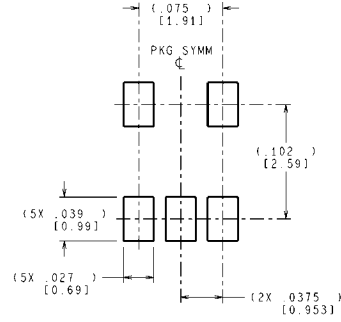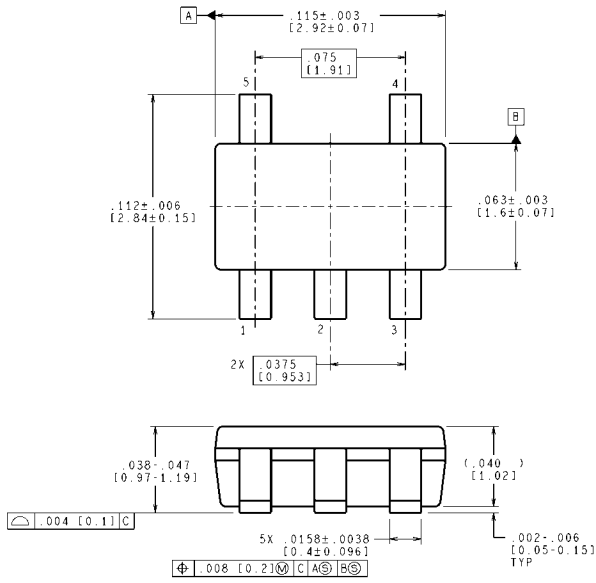
Figure 6 (a) shows the ADC directly connected to the amplifier. To minimize the glitch in this setting, a slower sample rate needs to be used. *Figure 6* (b) shows R_{ISO} and an external capacitor used to minimize the glitch.
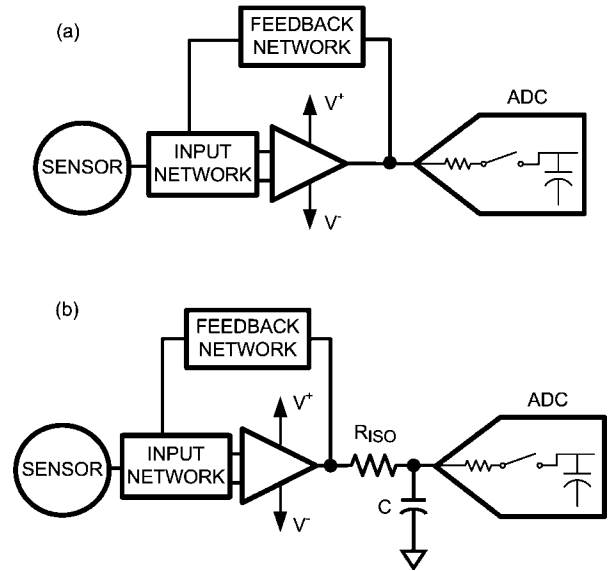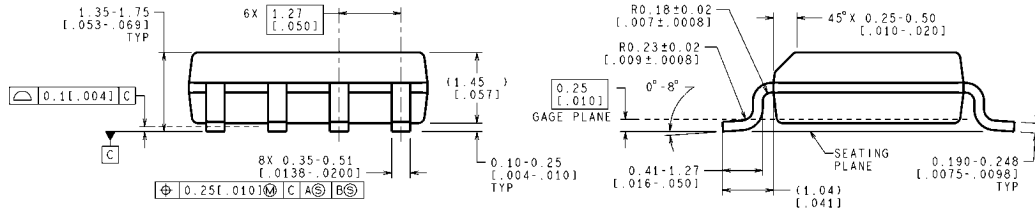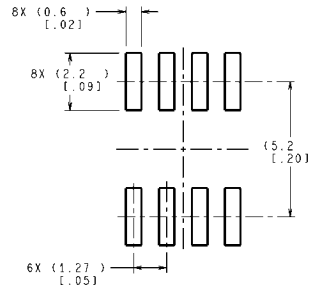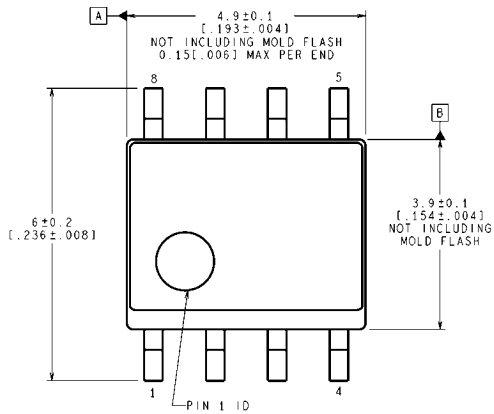

FIGURE 6. Driving an ADC

Physical Dimensions inches (millimeters) unless otherwise noted

.115±.003
[2.92±0.07]

.075
[1.91]

5   4

B

.112±.006
[2.84±0.15]

.063±.003
[1.6±0.07]

1   2   3

2X .0375
[0.953]

(.075)
[1.91]

PKG SYMM
℄

(.102)
[2.59]

(5X .039)
[0.99]

(5X .027)
[0.69]

(2X .0375)
[0.953]

LAND PATTERN RECOMMENDATION

.038-.047
[0.97-1.19]

(.040)
[1.02]

.004 [0.1] C

5X .0158±.0038
[0.4±0.096]

.002-.006
[0.05-0.15]
TYP

.008 [0.2] M C A S B S

R.004 MIN TYP
[0.1]

R.004 MIN TYP
[0.1]

.0060+.0015
-.0010
[0.152+0.038]
    -0.025
TYP

(.025)
[0.635]

.014-.022
[0.36-0.55]
TYP

SEATING
PLANE

.008
[0.2]
GAGE PLANE

C

0°-8° TYP

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MF05A (Rev D)

5-Pin SOT-23
NS Package Number MF05A

4.9±0.1
[.193±.004]
NOT INCLUDING MOLD FLASH
0.15[.006] MAX PER END

8   5

B

6±0.2
[.236±.008]

3.9±0.1
[.154±.004]
NOT INCLUDING
MOLD FLASH

1   4

PIN 1 ID

8X (0.6)
[.02]

8X (2.2)
[.09]

(5.2)
[.20]

6X (1.27)
[.05]

RECOMMENDED LAND PATTERN

1.35-1.75
[.053-.069]
TYP

6X 1.27
[.050]

0.1[.004] C

C

8X 0.35-0.51
[.0138-.0200]

(1.45)
[.057]

0.10-0.25
[.004-.010]
TYP

0.25 [.010] M C A S B S

R0.18±0.02
[.007±.0008]

R0.23±0.02
[.009±.0008]

0.25
[.010]
GAGE PLANE

0°-8°

0.41-1.27
[.016-.050]

45°X 0.25-0.50
[.010-.020]

SEATING
PLANE

(1.04)
[.041]

0.190-0.248
[.0075-.0098]
TYP

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev L)

8-Pin SOIC
NS Package Number M08A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	PowerWise® Design University	www.national.com/training

| | National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959 | National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com | National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com | National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com |

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		

TI E2E Community Home Page   e2e.ti.com