TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TCA62746AFG, TCA62746AFNG, TCA62746AFNAG, TCA62746BFNAG

16-Output Constant Current LED Driver with Output Open/Short Detection

The TCA62746 series are LED drivers with sink type constant circuit output, making them ideal for controlling LED modules and displays.

The current value of the 16-output is configurable using one external resistor.

In addition, these drivers are equipped with a function for detecting the output voltage when the output load LEDs open or short, and which then outputs the result as serial data.

These drivers consist of a 16-constant current output block, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate.

Features

- 16-output built-in
- Output open detection (OOD) function
  : When in detection mode, outputs the detection results via SOUT.
- Output short detection (OSD) function
  : When in detection mode, outputs the detection results via SOUT.
- Output current setting range
  : 2 to 50 mA × 16-constant current output
- Current accuracy (@ R_{EXT} = 1.56 kΩ, V_O = 1.0 V, V_{DD} = 5.0 V)
  : Between outputs: ± 1% (typ.)
    Between devices: ± 3% (max) @I_O=15mA
- Control data format: serial-in, parallel-out
- I/O logic: TTL level (Schmitt trigger input)
- Data transfer frequency: f_{SCK} = 25 MHz (max)
- Power supply voltage: V_{DD} = 4.5 to 5.5 V
- Operation temperature range: T_{opr} = −40 to 85°C
- Constant current output voltage: V_O = 17V (max)
- Output delay circuit built-in
- Internal data reset circuit for power-on resetting (POR)
- Backward compatible to TB62706B and TB62726A series drivers
- Package: AFG type: SSOP24-P-300-1.00B
          AFNG type: SSOP24-P-300-0.65A
          AFNAG/BFNAG: SSOP24-P-300-0.64

TCA62746AFG

SSOP24-P-300-1.00B

TCA62746AFNG

SSOP24-P-300-0.65A

TCA62746AFNAG/BFNAG

QSOP24-P-150-0.64

Weight
SSOP24-P-300-1.00B : 0.32 g (typ.)
SSOP24-P-300-0.65A : 0.14 g (typ.)
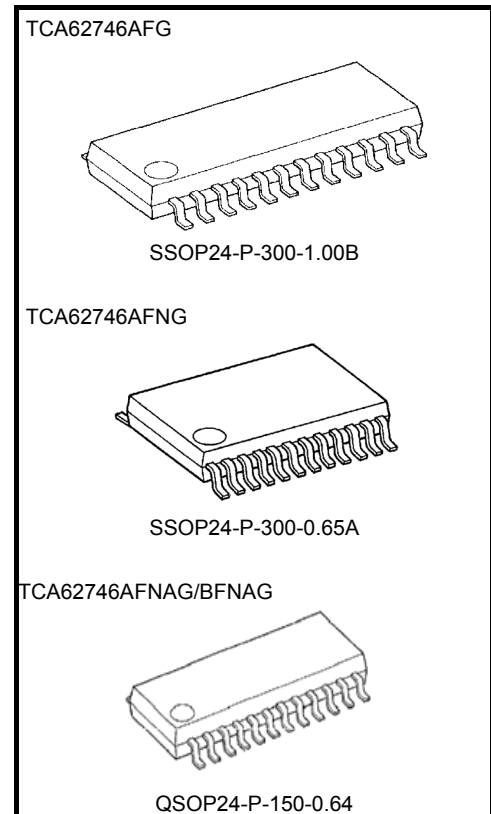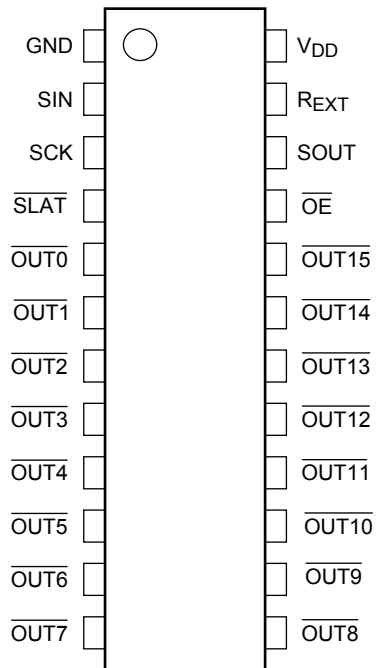SSOP24-P-150-0.64: 0.14 g (typ.)

Caution

This device is sensitive to electrostatic discharge. Please handle with care.
The terminals which are marginal to electro static discharge are shown in the following table.
(Please refer to page 22 for details.)

ESD test MM Model Marginal terminals (MM Model Internal Standard ±200V)
5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20

* ESD test HBM Model Internal Standard (±2000V) is OK

Pin Assignment (top view)

TCA62746AFG/AFNG/AFNAG

GND	V_{DD}
SIN	R_{EXT}
SCK	SOUT
$\overline{SLAT}$	$\overline{OE}$
$\overline{OUT0}$	$\overline{OUT15}$
$\overline{OUT1}$	$\overline{OUT14}$
$\overline{OUT2}$	$\overline{OUT13}$
$\overline{OUT3}$	$\overline{OUT12}$
$\overline{OUT4}$	$\overline{OUT11}$
$\overline{OUT5}$	$\overline{OUT10}$
$\overline{OUT6}$	$\overline{OUT9}$
$\overline{OUT7}$	$\overline{OUT8}$

TCA62746BFNAG

|	
$\overline{OUT14}$	$\overline{OUT13}$
$\overline{OUT15}$	$\overline{OUT12}$
$\overline{OE}$	$\overline{OUT11}$
SOUT	$\overline{OUT10}$
R_{EXT}	$\overline{OUT9}$
V_{DD}	$\overline{OUT8}$
GND	$\overline{OUT7}$
SIN	$\overline{OUT6}$
SCK	$\overline{OUT5}$
$\overline{SLAT}$	$\overline{OUT4}$
$\overline{OUT0}$	$\overline{OUT3}$
$\overline{OUT1}$	$\overline{OUT2}$
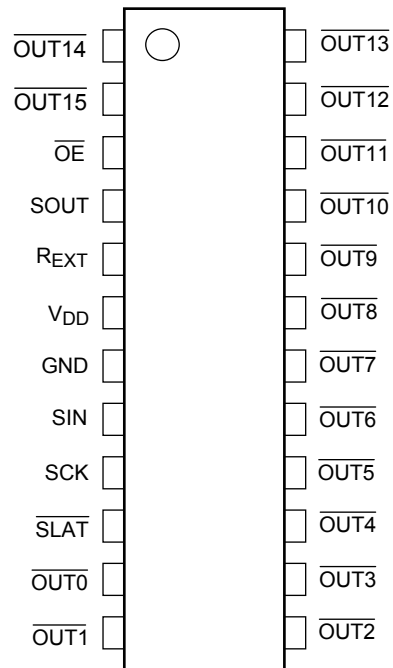
Note1: Short circuiting an output pin to a power supply pin (V_{DD} or $V_{LED}*$), or short-circuiting the R_{EXT} pin to the GND pin will likely exceed the rating, which in turn may result in smoldering and/or permanent damage. Please keep this in mind when determining the wiring layout for the power supply and GND pins.
*V_{LED}: LED power supply

Block Diagram
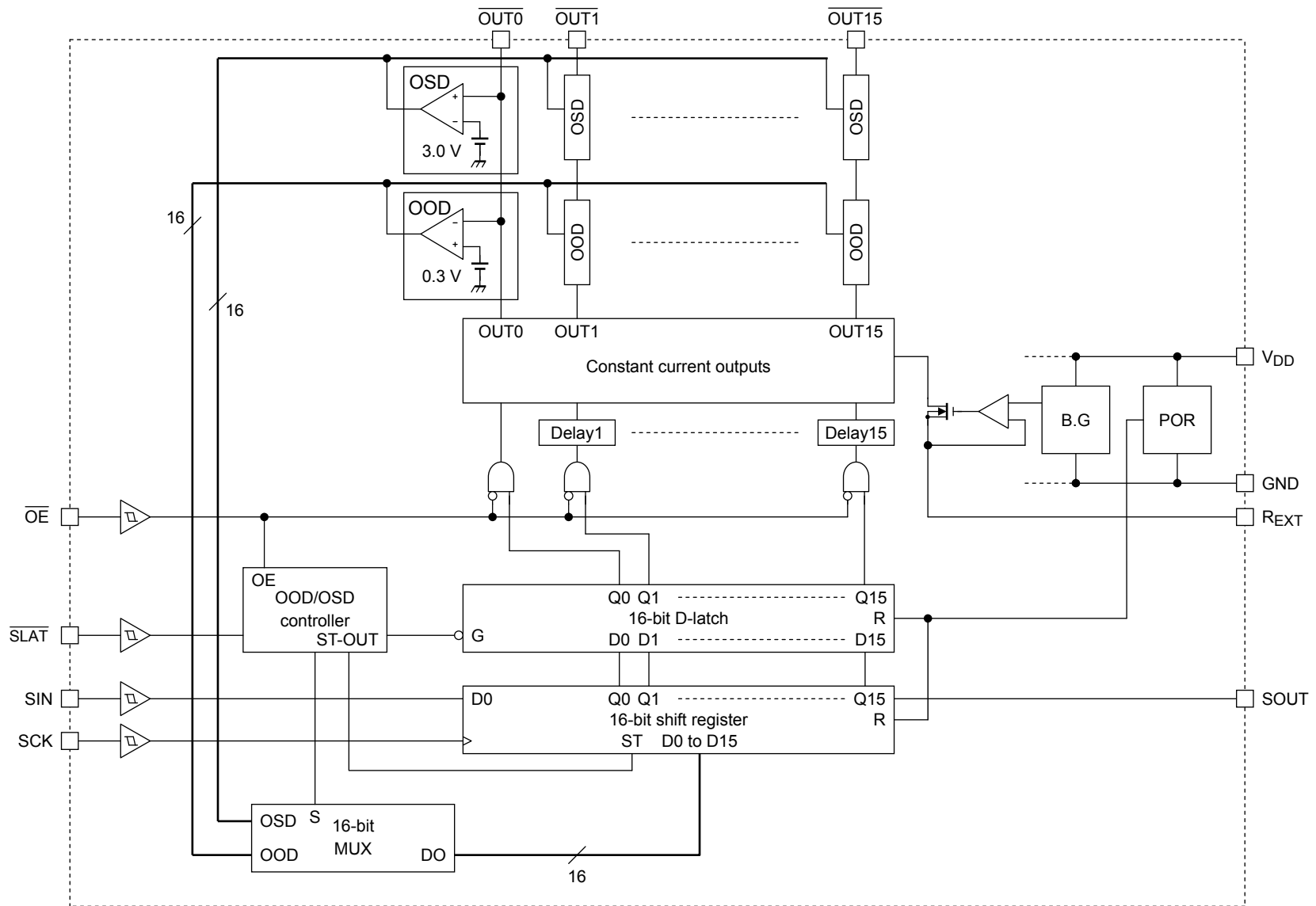
Truth Table

SCK	$\overline{\text{SLAT}}$	$\overline{\text{OE}}$	SIN	$\overline{\text{OUT0}} \cdots \overline{\text{OUT7}} \cdots \overline{\text{OUT15}}$ *1	SOUT
⤴	H	L	Dn	Dn ⋯ Dn − 7 ⋯ Dn − 15	Dn − 15
⤴	L	L	Dn + 1	No Change	Dn − 14
⤴	H	L	Dn + 2	Dn + 2 ⋯ Dn − 5 ⋯ Dn − 13	Dn − 13
⤵	- *2	L	Dn + 3	Dn + 2 ⋯ Dn − 5 ⋯ Dn − 13	Dn − 13
⤵	- *2	H	Dn + 3	OFF	Dn − 13

Note1: When $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ output pins are set to "H" the respective output will be ON and when set to "L" the respective output will be OFF.

Note2: "-" is irrelevant to the truth table.

Timing Chart
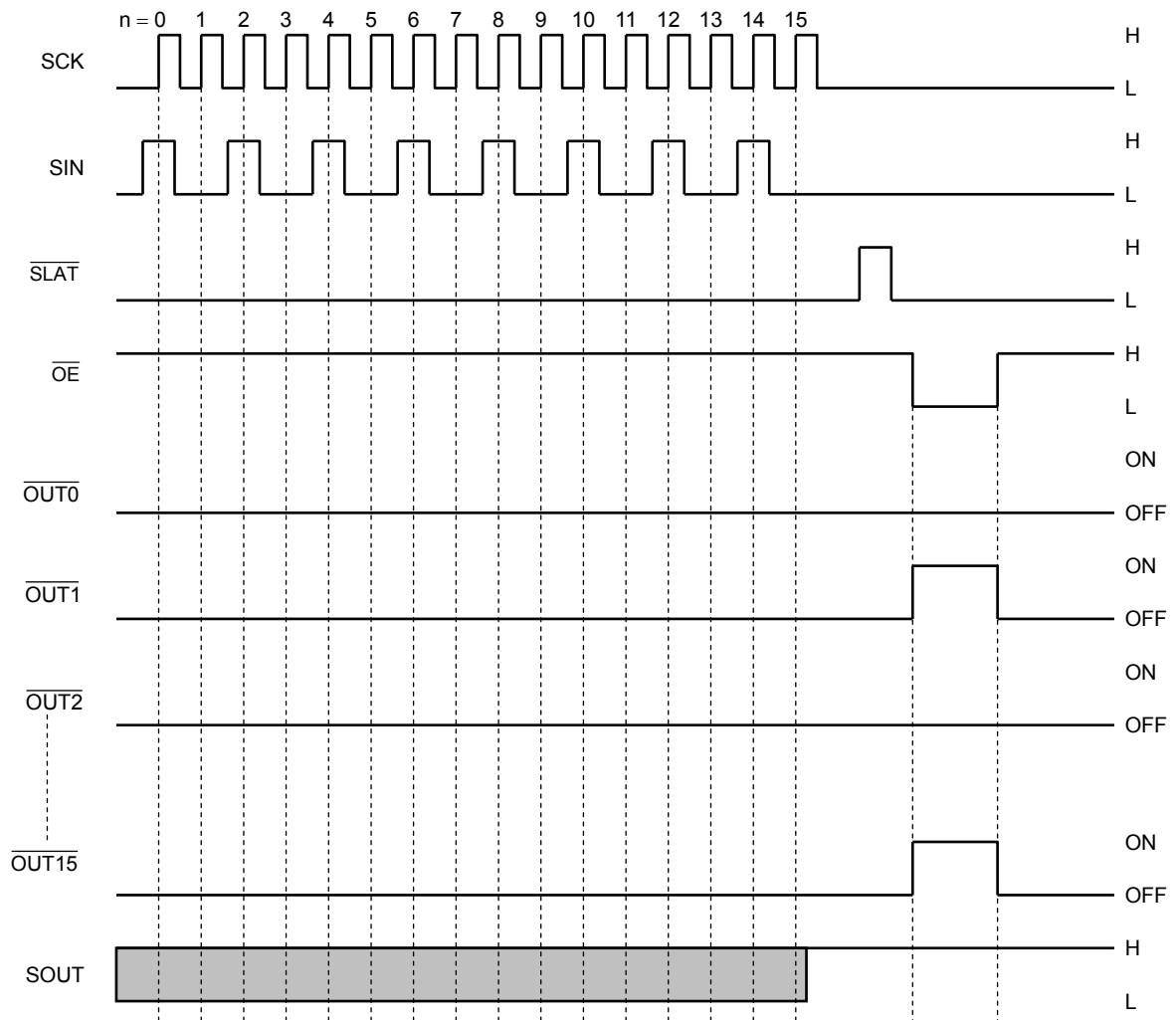
Note 1: The latch circuit is a leveled-latch circuit. Please exercise precaution as it is not triggered-latch circuit.

Note 2: Keep the $\overline{\text{SLAT}}$ pin is set to "L" to enable the latch circuit to hold data. In addition, when the $\overline{\text{SLAT}}$ pin is set to "H" the latch circuit does not hold data. The data will instead pass onto output.
When the $\overline{\text{OE}}$ pin is set to "L" the $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ output pins will go ON and OFF in response to the data. In addition, when the $\overline{\text{OE}}$ pin is set to "H" all the output pins will be forced OFF regardless of the data.

Pin Functions

Pin No	Pin Name	I/O	Function
1	GND	—	The ground pin.
2	SIN	I	The serial data input pin.
3	SCK	I	The serial data transfer clock input pin. The serial data is shifted by the rising edge of the clock. Also used for OOD/OSD mode settings.
4	$\overline{SLAT}$	I	The latch signal input pin. Data is saved at L level. Also used for OOD/OSD mode settings.
5	$\overline{OUT0}$	O	A sink type constant current output pin.
6	$\overline{OUT1}$	O	A sink type constant current output pin.
7	$\overline{OUT2}$	O	A sink type constant current output pin.
8	$\overline{OUT3}$	O	A sink type constant current output pin.
9	$\overline{OUT4}$	O	A sink type constant current output pin.
10	$\overline{OUT5}$	O	A sink type constant current output pin.
11	$\overline{OUT6}$	O	A sink type constant current output pin.
12	$\overline{OUT7}$	O	A sink type constant current output pin.
13	$\overline{OUT8}$	O	A sink type constant current output pin.
14	$\overline{OUT9}$	O	A sink type constant current output pin.
15	$\overline{OUT10}$	O	A sink type constant current output pin.
16	$\overline{OUT11}$	O	A sink type constant current output pin.
17	$\overline{OUT12}$	O	A sink type constant current output pin.
18	$\overline{OUT13}$	O	A sink type constant current output pin.
19	$\overline{OUT14}$	O	A sink type constant current output pin.
20	$\overline{OUT15}$	O	A sink type constant current output pin.
21	$\overline{OE}$	I	The constant current output enable signal input pin. During the "H" level, the output will be forced off. Also used for OOD/OSD mode settings.
22	SOUT	O	The serial data output pin. This pin outputs the OD/OSD detection result data.
23	R_{EXT}	—	The constant current value setting resistor connection pin. Resistance is connected with this terminal between GND. All output current is set as the same value.
24	V_{DD}	—	The power supply input pin.

Absolute Maximum Ratings ($T_a = 25°C$)

Characteristics	Symbol	Rating *1	Unit
Power supply voltage	V_{DD}	−0.4 to 6.0	V
Output current	I_O	55	mA
Logic input voltage	V_{IN}	−0.3 to V_{DD} + 0.3 *2	V
Output voltage	V_O	−0.3 to 17	V
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C
Thermal resistance	$R_{th(j-a)}$	94(AFG type When mounted PCB)/120(AFNG type When mounted PCB) *3 80.07(AFNAG/BFNAG type When mounted PCB)	°C/W
Power dissipation	P_D	1.32(AFG type When mounted PCB)/1.04(AFNG type When mounted PCB) *3,4 1.56(AFNAG/BFNAG type When mounted PCB)	W

Note1: Voltage is ground referenced.
Note2: However, do not exceed 6 V.
Note3: PCB condition 76.2 mm x 114.3 mm x 1.6 mm, Cu 30% (SEMI conforming)
Note4: The power dissipation decreases the reciprocal of the saturated thermal resistance (1/ Rth(j-a)) for each
degree (1°C) that the ambient temperature is exceeded (Ta = 25°C).

Operating Conditions

DC Items (Unless otherwise specified, $T_a = -40°C$ to 85°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	—	5.5	V
Output voltage when OFF	$V_{O (OFF)}$	Measuring pin is $\overline{OUTn}$	—	—	16	V
Output voltage when ON	$V_{O (ON)}$	Measuring pin is $\overline{OUTn}$	0.7	—	2.7	V
High level logic input voltage	V_{IH}	—	2.0	—	V_{DD}	V
Low level logic input voltage	V_{IL}	—	GND	—	0.8	V
High level SOUT output current	I_{OH}	V_{DD} = 5 V	—	—	−1	mA
Low level SOUT output current	I_{OL}	V_{DD} = 5 V	—	—	1	mA
Constant current output	I_O	Measuring pin is $\overline{OUTn}$	2	—	50	mA

AC Items (Unless otherwise specified, V_{DD} = 4.5 to 5.5 V, $T_a = -40°C$ to 85°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Serial data transfer frequency	f_{SCK}	7	—	—	—	25	MHz
Clock pulse width	t_{wSCK}	7	SCK = "H" or "L"	20	—	—	ns
Latch pulse width	t_{wSLAT}	7	$\overline{SLAT}$ = "H"	20	—	—	ns
Enable pulse width	t_{wOE1}	7	$\overline{OE}$ = "H" or "L" ,R_{EXT} = 500 Ω	100	—	—	ns
	t_{wOE2}	—	When error is detected *1	2	—	—	μs
Hold time	t_{HOLD1}	7	—	5	—	—	ns
	t_{HOLD2}	7	—	5	—	—	ns
	t_{HOLD3}	7	—	10	—	—	ns
	t_{HOLD4}	7	—	10	—	—	ns
Setup time	t_{SETUP1}	7	—	5	—	—	ns
	t_{SETUP2}	7	—	5	—	—	ns
	t_{SETUP3}	7	—	10	—	—	ns
	t_{SETUP4}	7	—	10	—	—	ns
Maximum clock rise time	t_r	7	*2	—	—	500	ns
Maximum clock fall time	t_f	7	*2	—	—	500	ns

Note1: Please refer to page 16 for details of the error detection.
Note2: If the device is connected in a cascade and the tr/tf of the clock waveform increases due to deceleration of the clock waveform,
it may not be possible to achieve the timing required for data transfer. Please keep these timing conditions in mind when
designing your application.

2010-06-25

Electrical Characteristics (Unless otherwise specified, V_{DD} = 4.5 to 5.5 V and T_a = 25°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH} = −1 mA, Measuring pin is SOUT	V_{DD} − 0.4	—	—	V
Low level logic output voltage	V_{OL}	1	I_{OH} = +1 mA, Measuring pin is SOUT	—	—	0.4	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD} Measuring pin is $\overline{OE}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND Measuring pin is $\overline{SLAT}$, SIN, SCK	—	—	−1	μA
Power supply current	I_{DD1}	4	V_O = 16 V, No R_{EXT} SCK = "L", $\overline{OE}$ = "H"	—	0.1	0.5	mA
	I_{DD2}	4	R_{EXT} = 1.56 kΩ, All output OFF	—	—	7.0	mA
	I_{DD3}	4	R_{EXT} = 500 Ω, All output OFF	—	—	14.0	mA
	I_{DD4}	4	R_{EXT} = 1.2 kΩ, All output ON	—	—	7.0	mA
	I_{DD5}	4	R_{EXT} = 500 Ω, All output ON	—	—	14.0	mA
Constant current output	I_{O1}*1	5	V_{DD} = 5.0V, V_O = 1.0 V, R_{EXT} = 1.56 kΩ	14.55	15	15.45	mA
	I_{O2}	5	V_{DD} = 5.0V, V_O = 1.0 V, R_{EXT} = 500 Ω	44.2	47	49.8	mA
Output OFF leak current	I_{OK}	5	V_O = 16 V, R_{EXT} = 1.56 kΩ, All output OFF	—	—	0.5	μA
Constant current error	ΔI_O	5	V_{DD} = 5.0V, V_O = 1.0 V R_{EXT} = 1.56 kΩ Measuring pin is $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±3	%
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD} = 4.5 to 5.5V, V_O = 1.0 V R_{EXT} = 1.56 kΩ Measuring pin is $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±4	%/V
Constant current output voltage regulation	$\%V_O$	5	V_{DD} = 5.0V, V_O = 1.0 to 3.0 V R_{EXT} = 1.56 kΩ Measuring pin is $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±4	%/V
Pull-up resistor	R_{UP}	3	Measuring pin is $\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	Measuring pin is $\overline{SLAT}$	250	500	800	kΩ

Note 1: TCA62746AFG is guaranteed by this specification manufactured after the week 47 of 2007 (Weekly code 747).
TCA62746AFNG is guaranteed by this specification.

Electrical Characteristics during OOD/OSD Mode
(Unless otherwise specified, V_{DD} = 4.5 to 5.5 V and T_a = 25°C)

| Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
OOD voltage	V_{OOD}	6	R_{EXT} = 464 Ω to 11.5 kΩ	—	0.30	0.40	V
OSD voltage	V_{OSD}	6	R_{EXT} = 464 Ω to 11.5 kΩ	2.85	3.0	—	V

## Switching Characteristics (Unless otherwise specified, $T_a = 25°C$ and $V_{DD} = 5.0$ V)

Characteristics		Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Propagation delay time	SCK- $\overline{OUT0}$	t_{pLH1}	7	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	20	100	ns
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pLH2}	7	$\overline{OE}$ = "L"	—	20	100	
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	7	$\overline{SLAT}$ = "H"	—	20	100	
	SCK-SOUT	t_{pLH}	7	—	5	10	—	
	SCK- $\overline{OUT0}$	t_{pHL1}	7	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	50	100	
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pHL2}	7	$\overline{OE}$ = "L"	—	50	100	
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}	7	$\overline{SLAT}$ = "H"	—	50	100	
	SCK-SOUT	t_{pHL}	7	—	15	20	—	
Output rise time		t_{or}	7	10 to 90% of voltage waveform	—	30	150	ns
Output fall time		t_{of}	7	90 to 10% of voltage waveform	—	70	150	ns
Output delay time		$t_{DLY (ON)}$	7	$\overline{OUTn}$ - $\overline{OUT(n+1)}$ between adjacent outputs	—	20	—	ns
Output delay time		$t_{DLY (OFF)}$	7	$\overline{OUTn}$ - $\overline{OUT(n+1)}$ between adjacent outputs	—	20	—	ns

I/O Equivalent Circuits

1. SCK, SIN
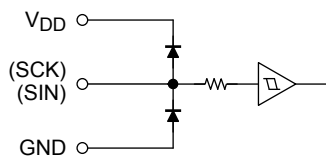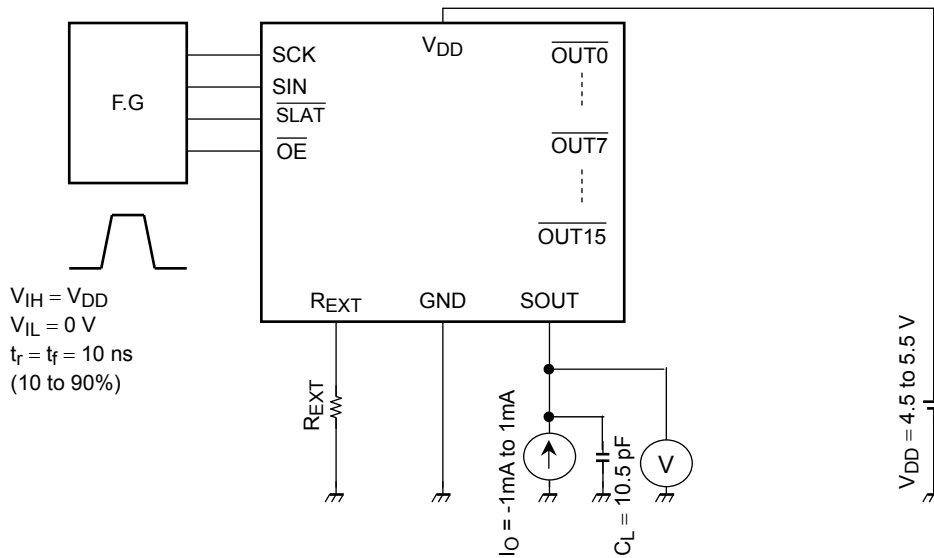
2. $\overline{OE}$
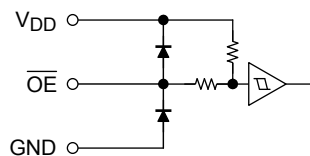
3. $\overline{SLAT}$
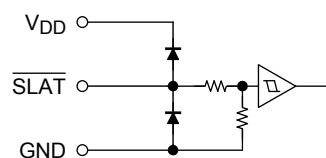
4. SOUT
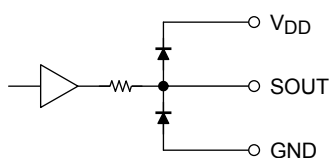
5. $\overline{OUT0}$ to $\overline{OUT15}$
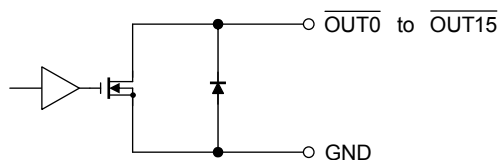
Test Circuits

Test Circuit 1: High level logic input voltage / Low level logic input voltage
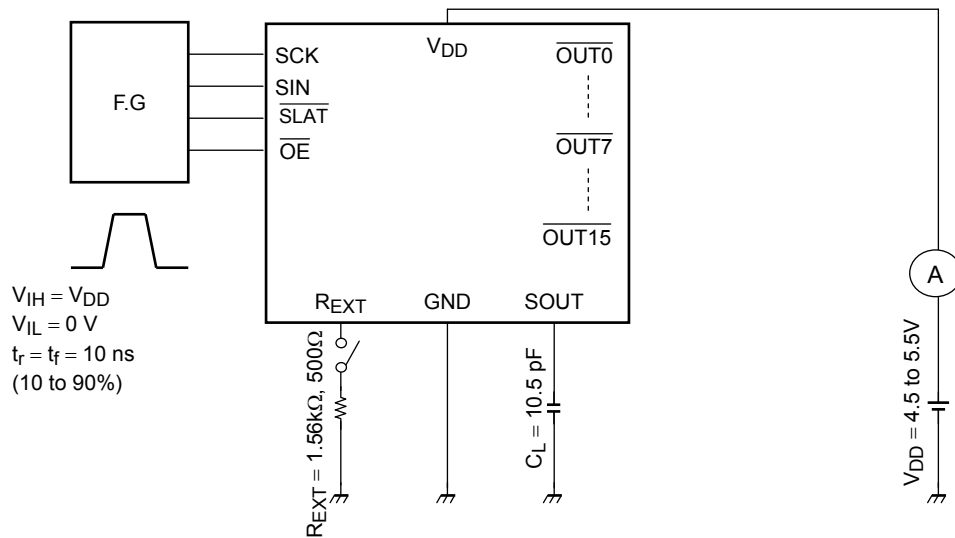

$V_{IH} = V_{DD}$
$V_{IL} = 0\ V$
$t_r = t_f = 10\ ns$
(10 to 90%)

Test Circuit 2: High level logic input current / Pull-down resistor
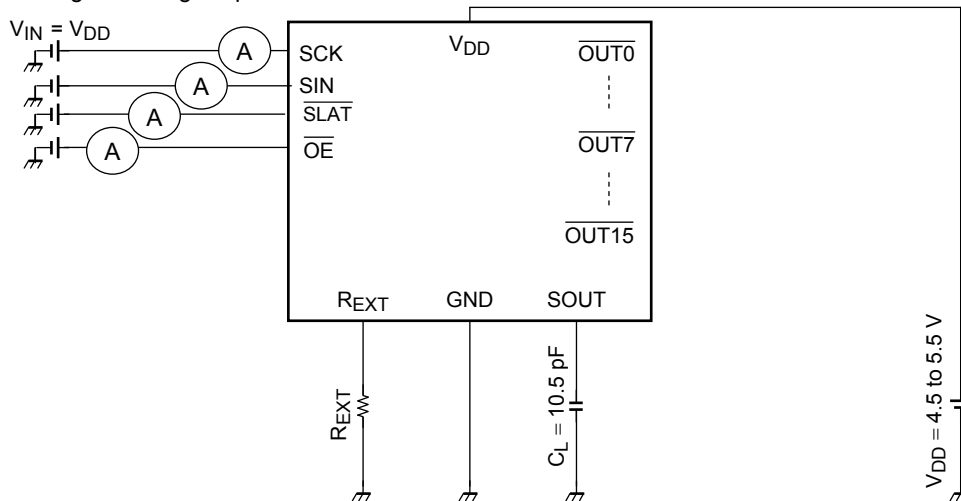
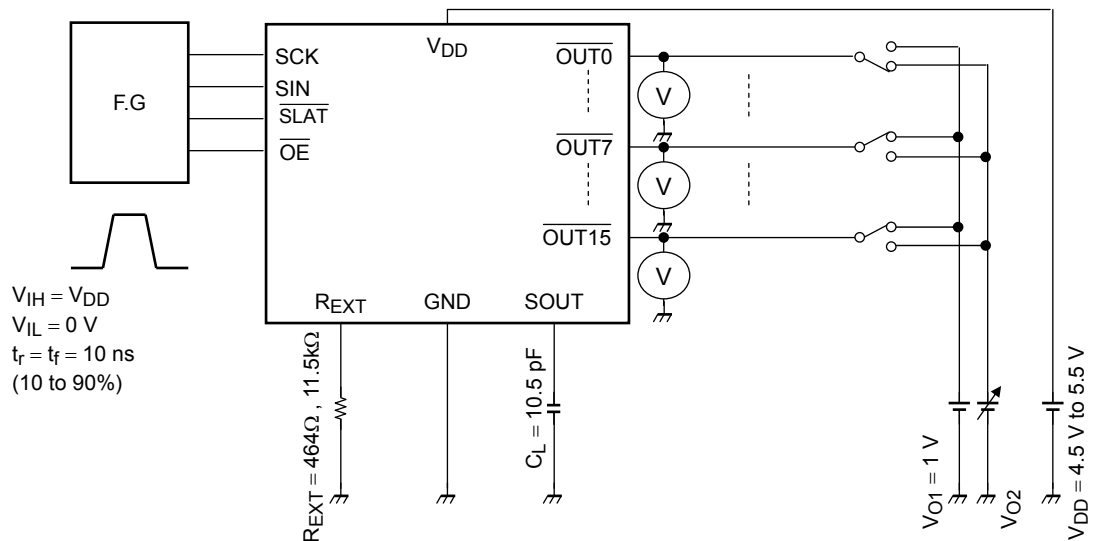Test Circuit 3: Low level logic input current / Pull-up resistor

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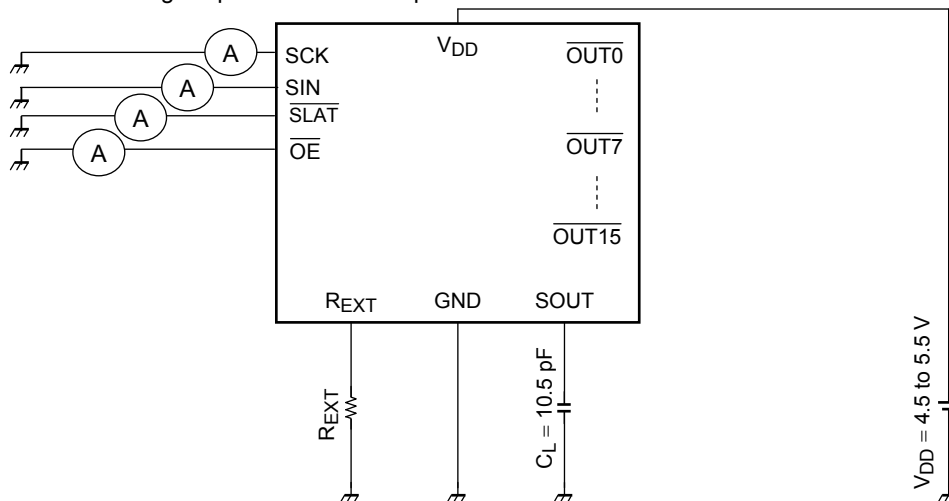
Test Circuit 4: Power supply current

Test Circuit 5: Constant current output / Output OFF leak current / Constant current error
Constant current power supply voltage regulation / Constant current output voltage regulation
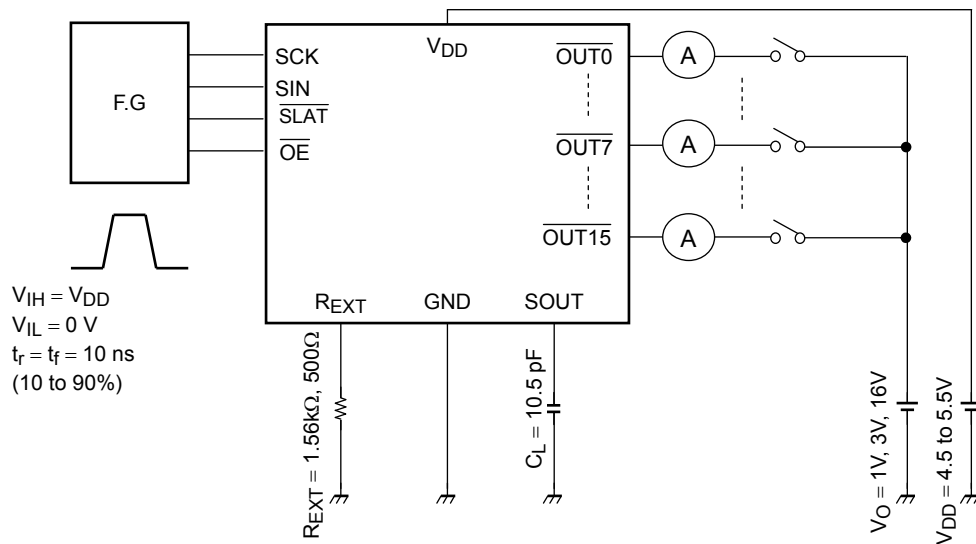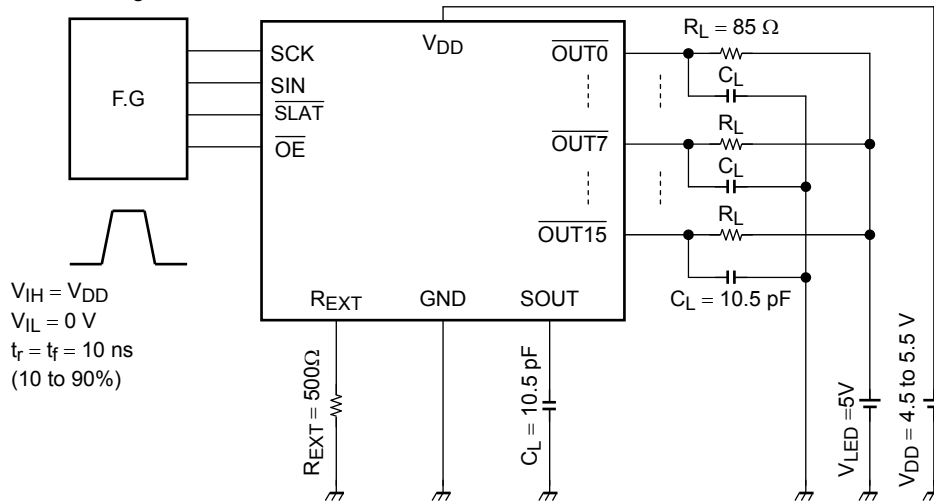

Test Circuit 6: OOD voltage / OSD voltage

All output terminals is set to turning on, only one output terminal is connected with the V_{O2} power supply, and V_{O2} is changed. V_{OOD}/V_{OSD} is confirmed by the error detection result from SOUT.

Test Circuit 7: Switching Characteristics

$V_{IH} = V_{DD}$
$V_{IL} = 0$ V
$t_r = t_f = 10$ ns
(10 to 90%)

Output Delay Circuit

This is designed for high speed switching between outputs and is intended to have the effect of reducing switching noise by reducing the di/dt when all outputs are ON or OFF at the same time. There is a switching time lag (20 ns typ.) between adjacent outputs.

The equivalent circuit chart of the delay circuit is shown in the following.
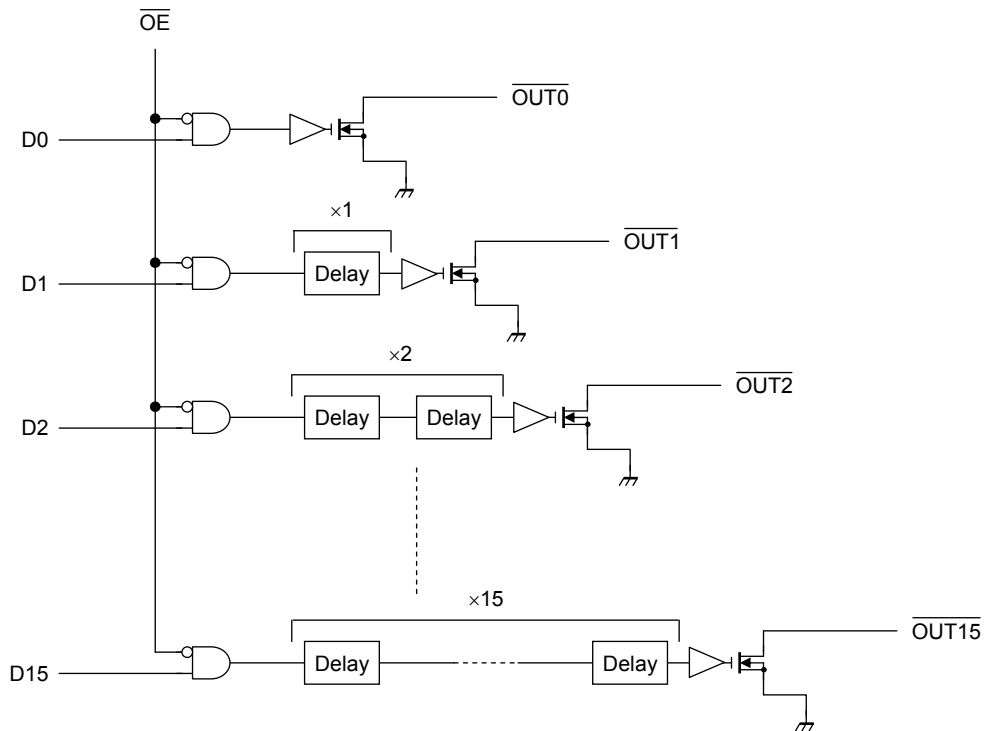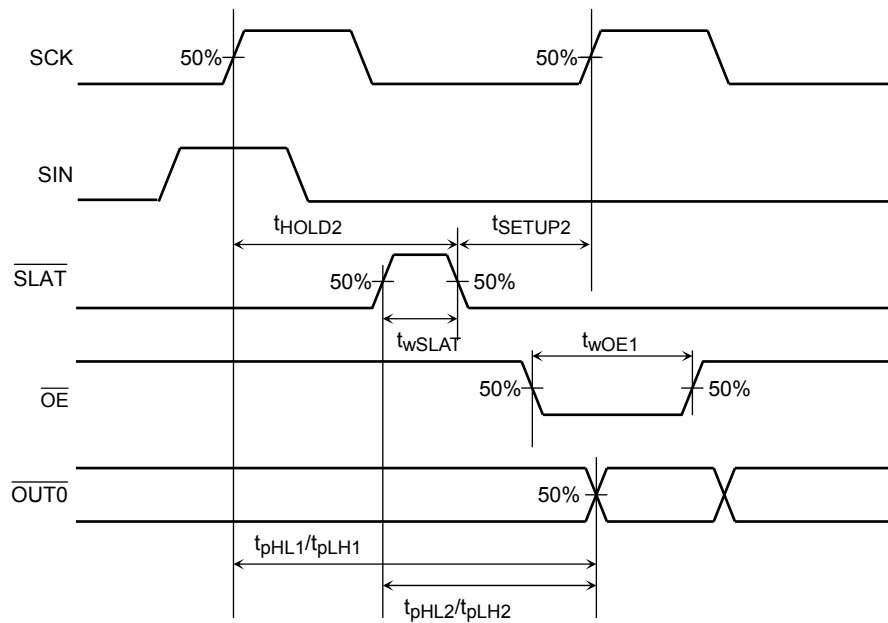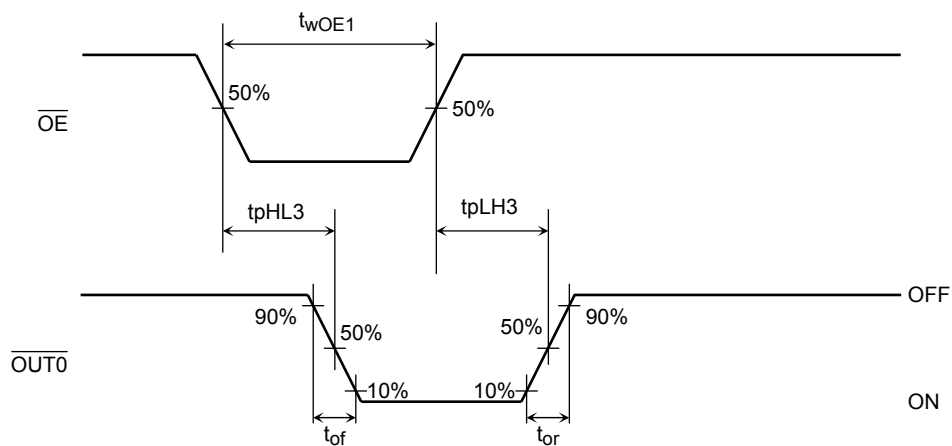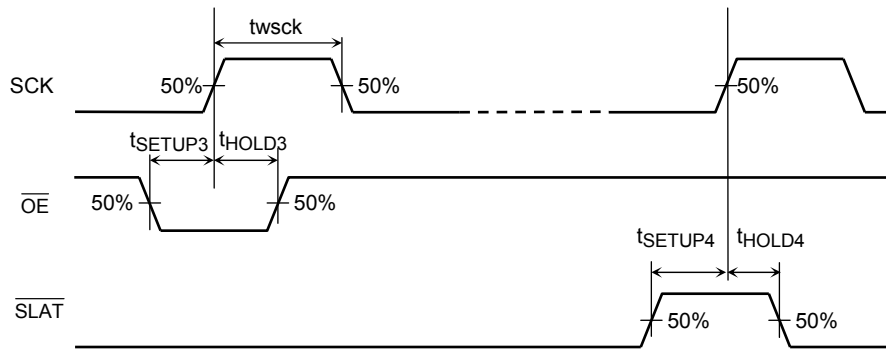
Timing Waveforms

1. SCK, SIN, SOUT
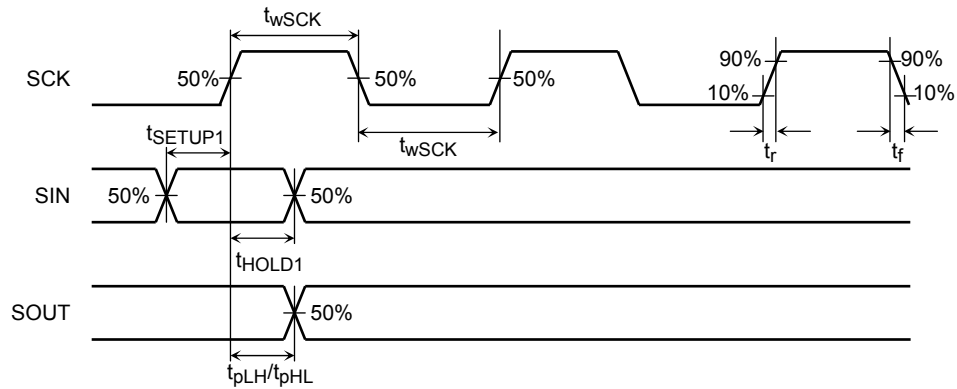
2. SCK, SIN, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$, $\overline{\text{OUT0}}$
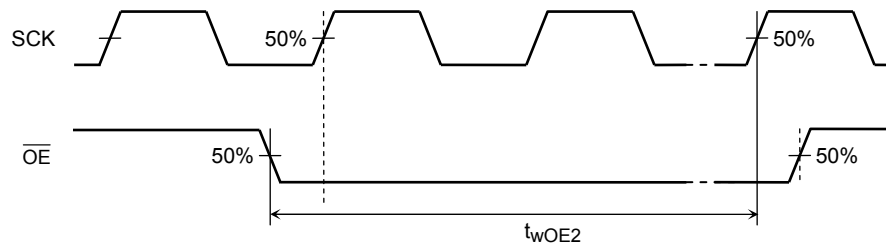

3. $\overline{\text{OUT0}}$

4. OOD Mode/OSD Mode
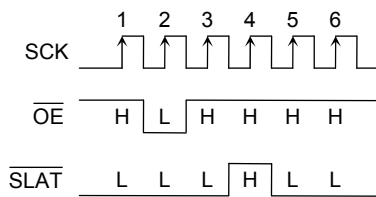

5. OOD/OSD Read Mode

PWM grayscale control

   This IC is possible to PWM grayscale control by the input of the PWM signal to the EN terminal.

When PWM grayscale control is done, we recommend the LED power-supply voltage to be set to become the

satiety region of the constant current characteristic. When using this IC outside the saturation area, PWM grayscale

control cannot be normally done.

Switching to Open Circuit Detection (OOD) and Short Circuit Detection (OSD) Modes
Switching to OSD mode

```
            1   2   3   4   5   6
 SCK    ___|↑|_|↑|_|↑|_|↑|_|↑|_|↑|___

  ___
  OE      H | L | H   H   H   H

  ____
  SLAT      L   L   L | H | L   L
```

   The signal sequence set to be in the OSD mode. Here, the $\overline{SLAT}$ active pulse would not latch any data.

Switching to OOD mode

```
            1   2   3   4   5   6
 SCK    __|↑|_|↑|_|↑|_|↑|_|↑|_|↑|___

  ___
  OE      H | L | H   H   H   H

  ____
  SLAT      L   L   L   L   L | H |
```
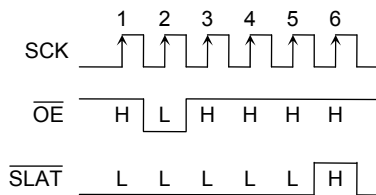
   The signal sequence set to be in the OOD mode. Here, the $\overline{SLAT}$ active pulse would not latch any data.

Reading Error Status Code

```
                    n ≥ 3
              1    2    3
   SCK       ↑    ↑    ↑        ↑ ↑ ↑ ↑ ↑
           MIN 2 μs
   OE    H   L    L    L        H H H H H

   SOUT  [        ]            Error status code
                               Bit    Bit Bit Bit Bit Bit
                               15     14  13  12  11  10
```
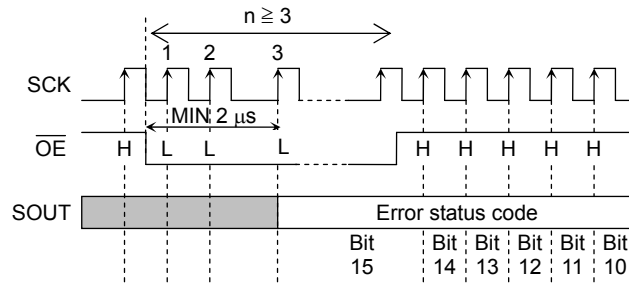
When the above signal sequence is set in the OOD and OSD modes, the error state code can be read through the terminal SOUT.

Error state code of OOD detection mode

	Error state code	State of output terminal
$V_{OOD} \geq V_O$	0	Open circuit
$V_{OOD} < V_O$	1	Normal

Error state code of OSD detection mode

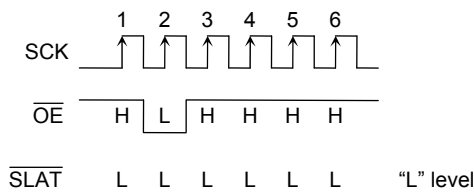|	Error state code	State of output terminal
$V_{OSD} \leq V_O$	0	Short circuit
$V_{OSD} > V_O$	1	Normal

Description

In the OOD and OSD modes, the state of $\overline{OE}$ must be switched from "H" to "L". And, then, This IC would execute Open-/Short-circuit Detection as well as enabling output ports to drive current.

At least three clock must be inputs at the "L" state of $\overline{OE}$ and the third clock should be at least 2 μs after the falling edge of $\overline{OE}$. the detected error status into the built-in shift register is done by rising edge of this third clock.

When $\overline{OE}$ is "L", the serial data cannot be input from the terminal SIN.
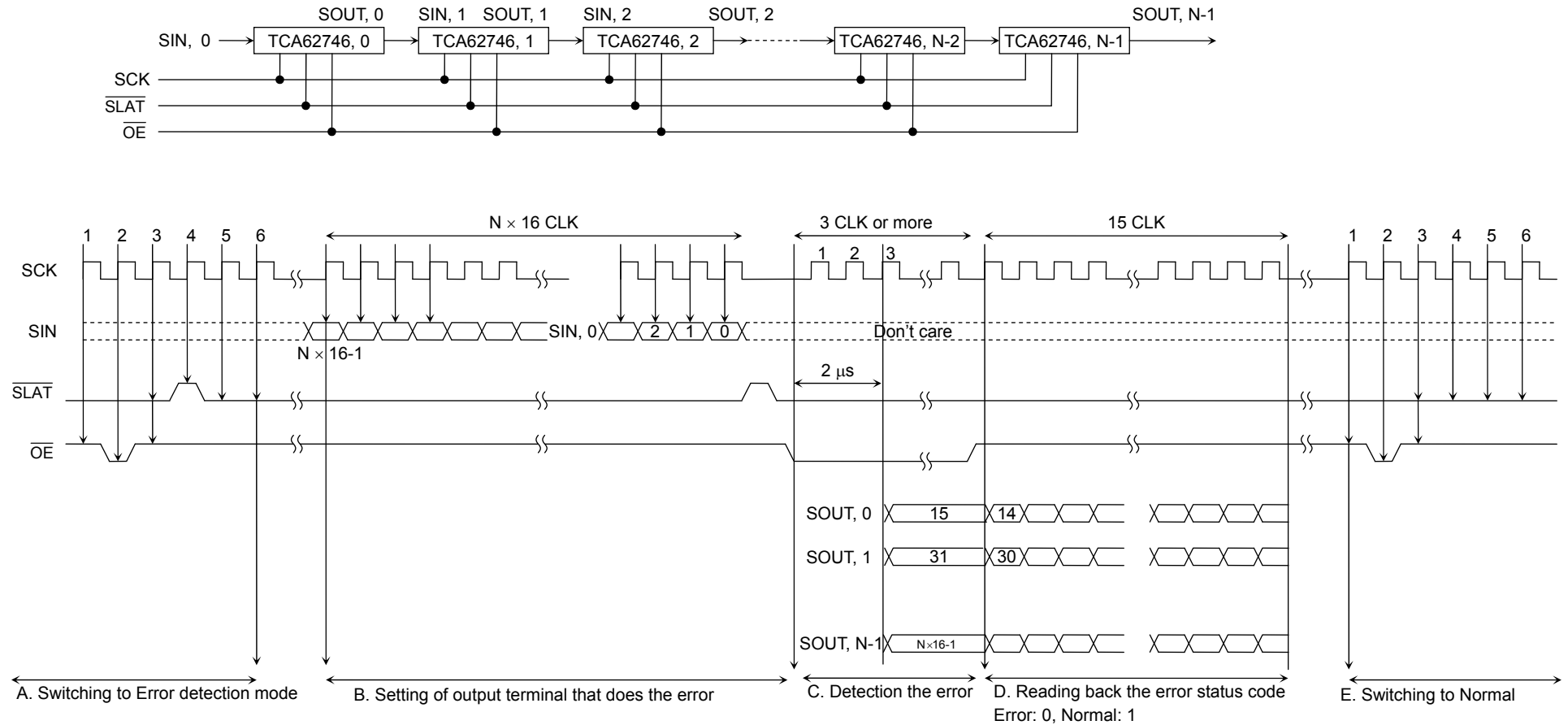
When $\overline{OE}$ is changed from "L" to "H", the error state code is output from the terminal SOUT synchronizing with the clock.

Switching to Normal Mode

```
          1   2   3   4   5   6
   SCK      ↑   ↑   ↑   ↑   ↑   ↑

   OE     H  L  H   H   H   H

   SLAT   L   L   L   L   L   L    "L" level
```

The signal sequence set to be in the Normal mode.

Timing chart of error detection mode (OSD mode)

A. Switching to Error detection mode
B. Setting of output terminal that does the error
C. Detection the error
D. Reading back the error status code Error: 0, Normal: 1
E. Switching to Normal

Reference data

*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

Set output current – Duty cycle graph
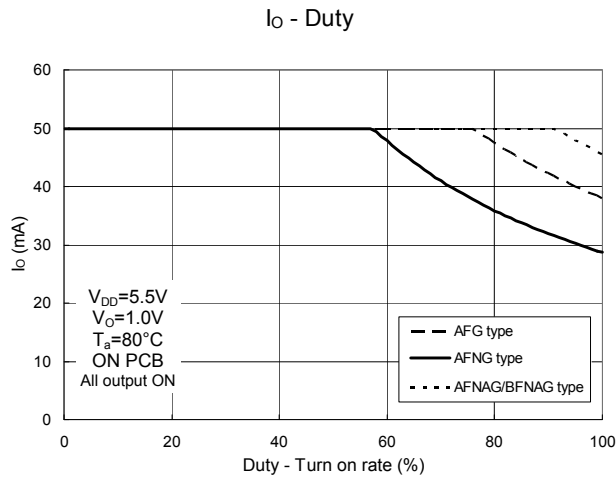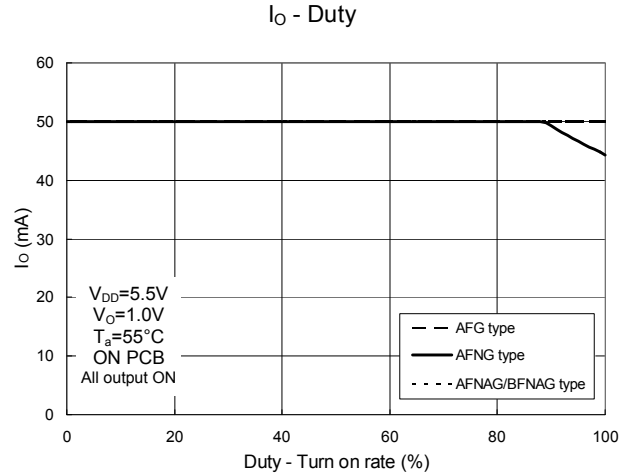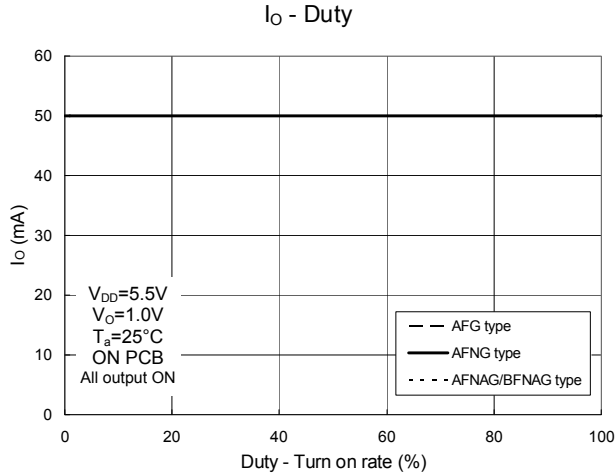
I_O - Duty

V_{DD}=5.5V
V_O=1.0V
T_a=25°C
ON PCB
All output ON

– – – AFG type
——— AFNG type
· · · · · AFNAG/BFNAG type

I_O - Duty

V_{DD}=5.5V
V_O=1.0V
T_a=55°C
ON PCB
All output ON

– – – AFG type
——— AFNG type
· · · · · AFNAG/BFNAG type

I_O - Duty

V_{DD}=5.5V
V_O=1.0V
T_a=80°C
ON PCB
All output ON

– – – AFG type
——— AFNG type
· · · · · AFNAG/BFNAG type

Power dissipation – Ta

P_D - Ta

ON PCB

– – – AFG type
——— AFNG type
· · · · · AFNAG/BFNAG type
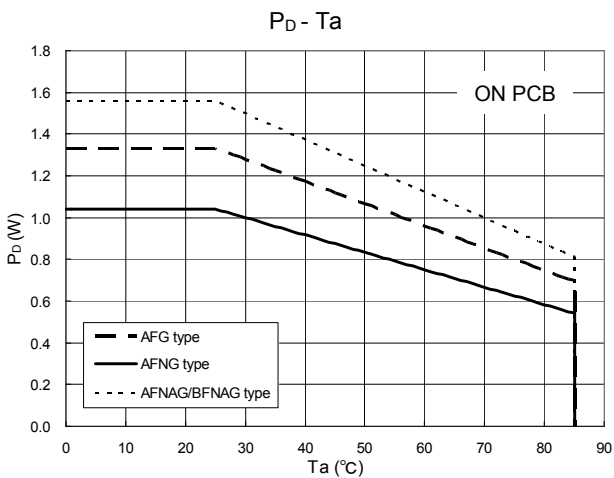
Reference data

*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

Output Current – R_{EXT} Resistor

I_O - R_{EXT}

Theoretical value
$$I_O (A) = (1.23(V) \div R_{EXT} (\Omega)) \times 19$$

V_{DD}=5.0V
V_O=1.0V
T_a=25°C

Io (mA) vs R_{EXT} (kΩ)

Constant current characteristic

I_O - V_O

V_{DD}=5.0V
V_O=1.0V
T_a=25°C

Io (mA) vs V_O (V)
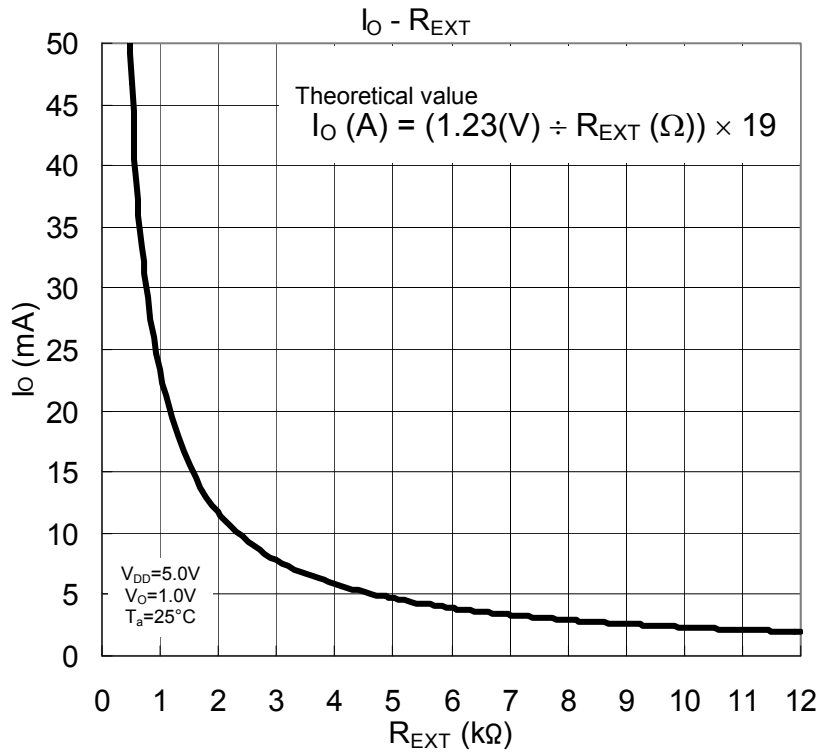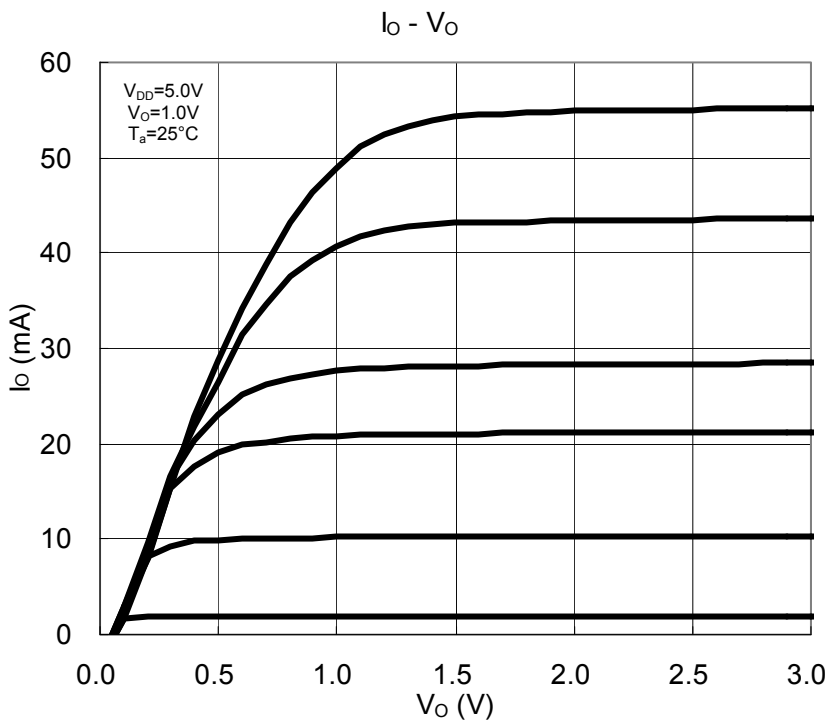
Package Dimensions

SSOP24-P-300-1.00B

Unit : mm
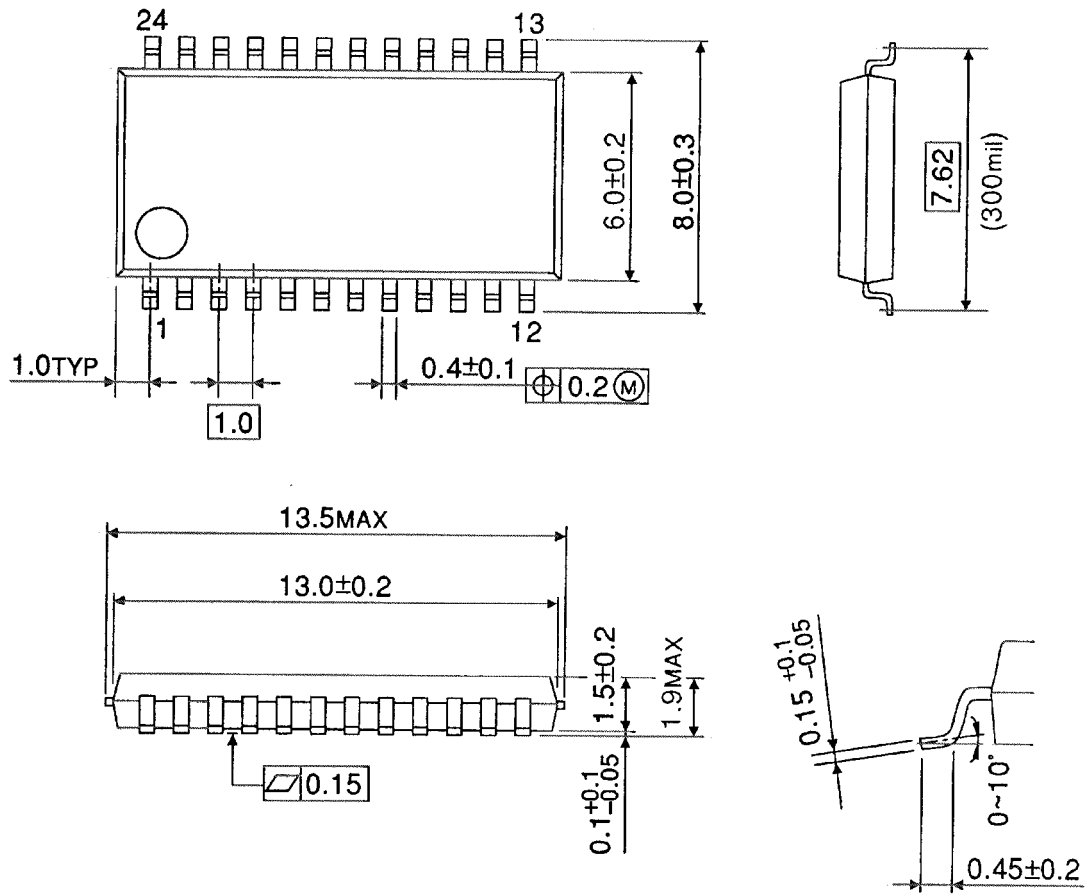
Weight: 0.32 g (typ.)

Package Dimensions

SSOP24-P-300-0.65A   Unit: mm
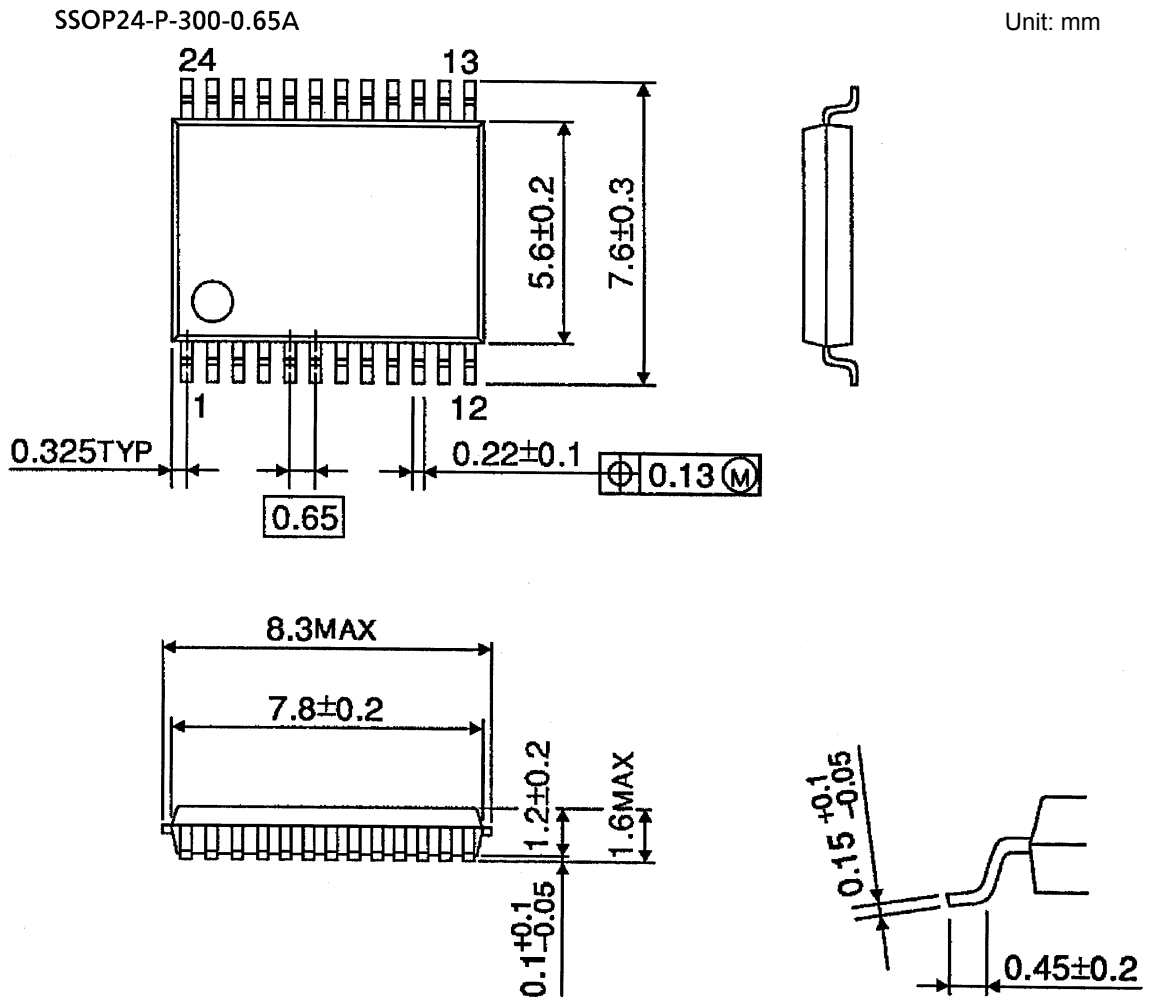
Weight: 0.14 g (typ.)

Package Dimensions

SSOP24-P-150-0.64

Unit: Inch

0.337 to 0.344

0.0325(REF)

0.150 to 0.157

0.229 to 0.244

0.025

0.008 to 0.012

0.054 to 0.068

0.004 to 0.098

0.010(TYP)

0.016 to 0.034
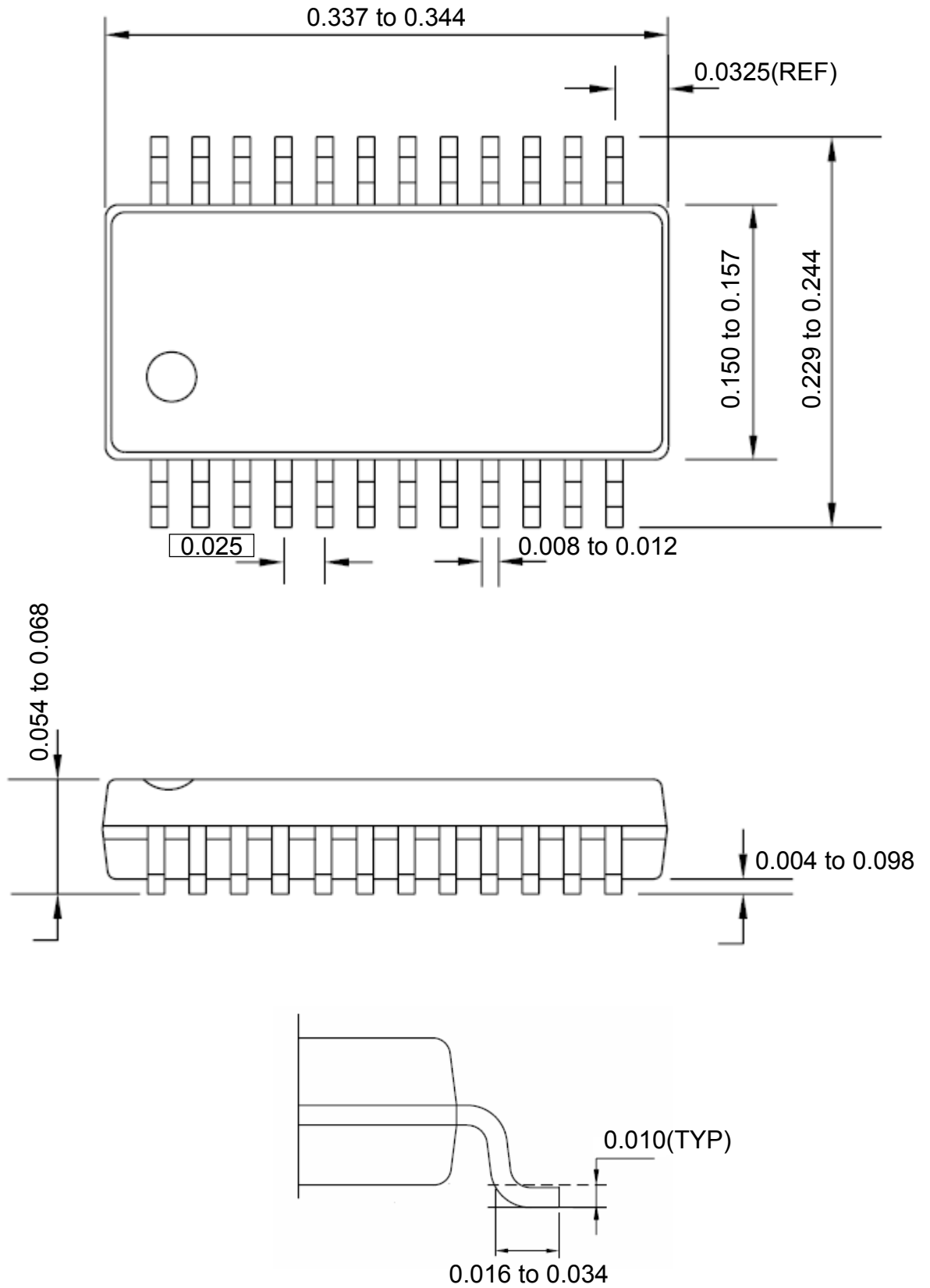
Weight: 0.14 g (typ.)

Serge resisting

The terminals which are weak to electro static discharge are shown in the following table.

pin	MM Model ESD test Result (Internal Standard ±200V)			
	- Serge		+ Serge	
	Standard	TEST Result	Standard	TEST Result
1	V_{DD}	200V	V_{DD}	200V
2	V_{DD},GND	200V	V_{DD},GND	200V
3	V_{DD},GND	200V	V_{DD},GND	200V
4	V_{DD},GND	200V	V_{DD},GND	200V
5	V_{DD},GND	200V	V_{DD},GND	**160V**
6	V_{DD},GND	200V	V_{DD},GND	**160V**
7	V_{DD},GND	200V	V_{DD},GND	**160V**
8	V_{DD},GND	200V	V_{DD},GND	**160V**
9	V_{DD},GND	200V	V_{DD},GND	**160V**
10	V_{DD},GND	200V	V_{DD},GND	**160V**
11	V_{DD},GND	200V	V_{DD},GND	**160V**
12	V_{DD},GND	200V	V_{DD},GND	**160V**
13	V_{DD},GND	200V	V_{DD},GND	**160V**
14	V_{DD},GND	200V	V_{DD},GND	**160V**
15	V_{DD},GND	200V	V_{DD},GND	**160V**
16	V_{DD},GND	200V	V_{DD},GND	**160V**
17	V_{DD},GND	200V	V_{DD},GND	**160V**
18	V_{DD},GND	200V	V_{DD},GND	**160V**
19	V_{DD},GND	200V	V_{DD},GND	**160V**
20	V_{DD},GND	200V	V_{DD},GND	**160V**
21	V_{DD},GND	200V	V_{DD},GND	200V
22	V_{DD},GND	200V	V_{DD},GND	200V
23	V_{DD},GND	200V	V_{DD},GND	200V
24	GND	200V	GND	200V

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

About solderability, following conditions were confirmed

Solderability

(1) **Use of Sn-37Pb solder Bath**
·   **solder bath temperature: 230°C**
·   **dipping time: 5 seconds**
·   **the number of times: once**
·   **use of R-type flux**

(2) **Use of Sn-3.0Ag-0.5Cu solder Bath**
·   **solder bath temperature: 245°C**
·   **dipping time: 5 seconds**
·   **the number of times: once**
·   **use of R-type flux**

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