Am54S/74S174•Am54S/74S175

Hex/Quadruple D-Type Flip Flops With Clear

Distinctive Characteristics

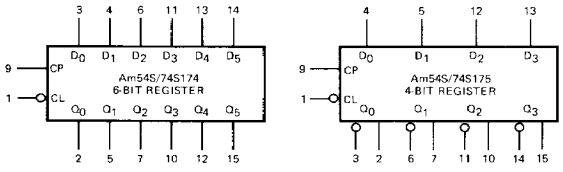
- 4-Bit and 6-Bit high-speed parallel registers.
- Common clock and common clear.
- Positive edge-triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am54S/74S174 is a six-bit, high-speed register and the Am54S/74S175 is a four-bit, high-speed register built using advanced Schottky technology. The registers consist of D-type flip-flops with a buffered common clock and an asynchronous active LOW buffered clear.

When the clear is LOW, the Q outputs are LOW independent of the other inputs. Information meeting the set-up requirements of the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

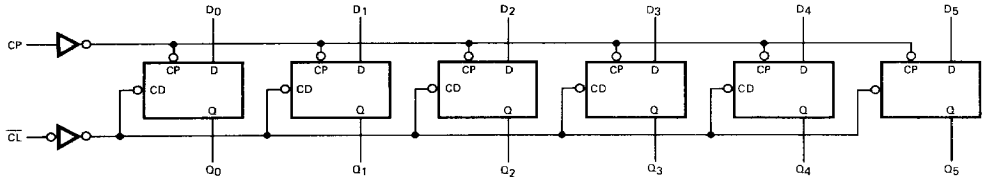
LOGIC SYMBOLS



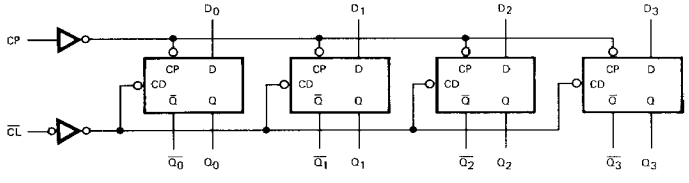
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S174



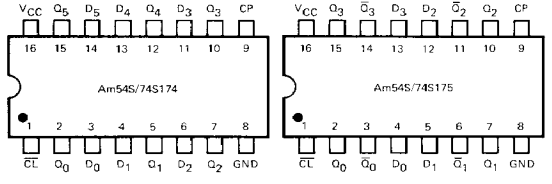
Am54S/74S175



ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S174 Order Number	Am54S/74S175 Order Number
Molded DIP	0°C to +70°C	SN74S174N	SN74S175N
Hermetic DIP	0°C to +70°C	SN74S174J	SN74S175J
Dice	0°C to +70°C	SN74S174X	SN74S175X
Hermetic DIP	−55°C to +125°C	SN54S174J	SN54S175J
Hermetic Flat Pak	−55°C to +125°C	SN54S174W	SN54S175W
Dice	−55°C to +125°C	SN54S174X	SN54S175X

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S174, Am74S175 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am54S174, Am54S175 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA, V_{IN} = V_{IH} or V_{IL}	74S	2.7	3.4		Volts
			54S	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S174		90	144	mA
			S175		60	96	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open and 4.5 V applied to the data and clear inputs. Measured after a momentary ground, then 4.5 V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output		V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω		8	12	ns
t_{PHL}					11.5	17	
t_{PLH}	Clear to Output				10	15	ns
t_{PHL}					13	22	
t_{pw}	Pulse Width	Clock		7			ns
		Clear		10			
t_s	Data Set-up Time			5			ns
t_s	Set-up Time. Clear Recovery (in-active) to Clock			5			ns
t_h	Data Hold Time			3			ns
f_{MAX}	Maximum Clock Frequency			75	110		MHz

Am54S/74S174 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{CL}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

Am54S/74S175 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{CL}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

FUNCTION TABLE

INPUTS			OUTPUTS	
Clear	Clock	D_i	Q_i	$\overline{Q}_i$
L	X	X	L	H
H	L	X	NC	NC
H	H	X	NC	NC
H	↑	L	L	H
H	↑	H	H	L

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH Transition
Note: $\overline{Q}_i$ on Am54S/74S175 only

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

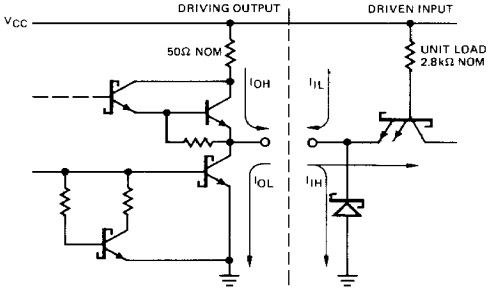
CL Clear. When the clear is LOW, the Qi outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

CP Clock pulse for the register. Enters data on the positive transition.

Q_i The TRUE register outputs.

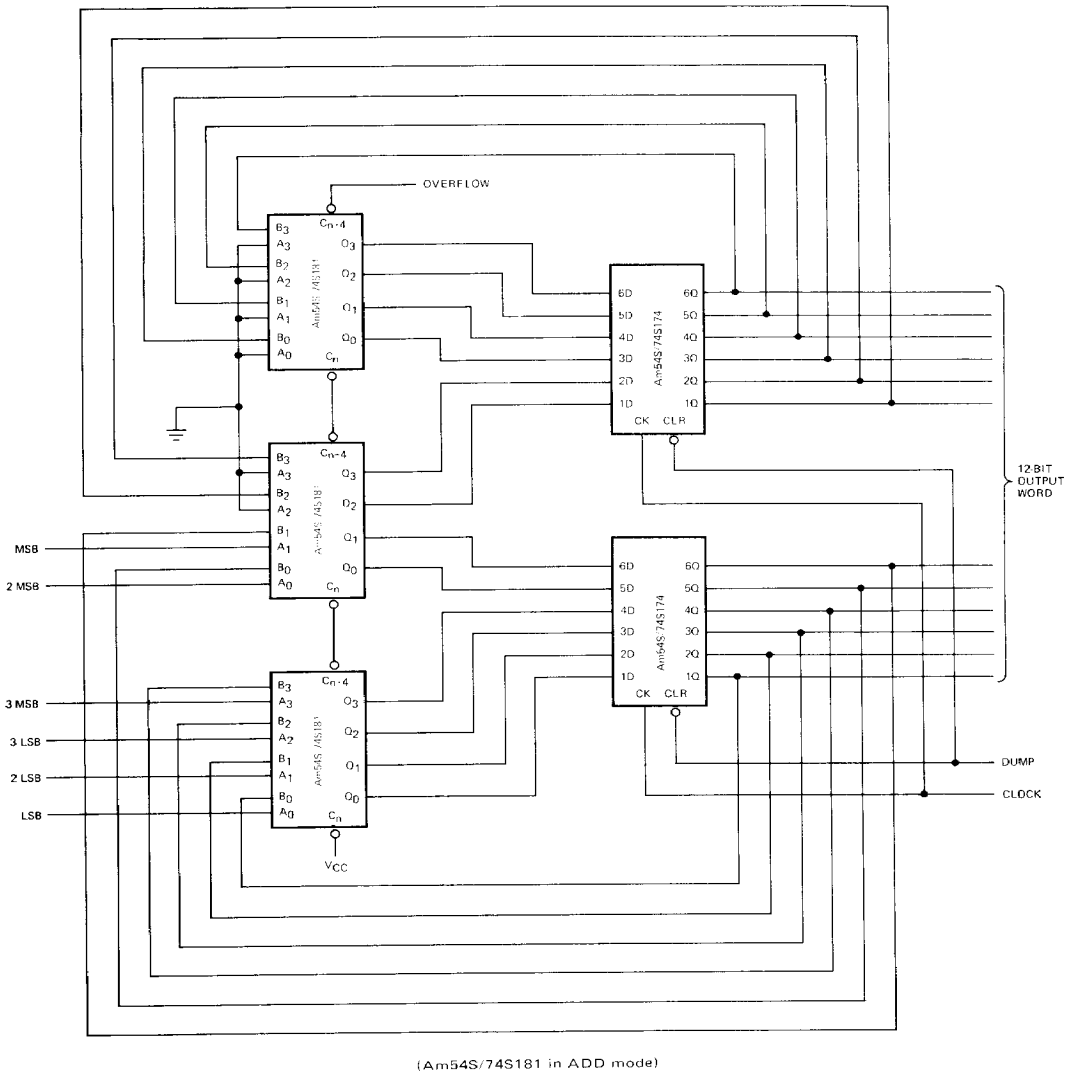
$\overline{Q}_i$ The complement register outputs.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATION

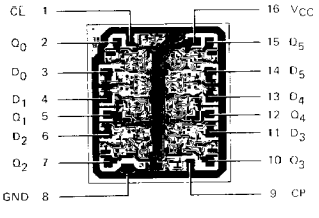


(Am54S/74S181 in ADD mode)

6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)

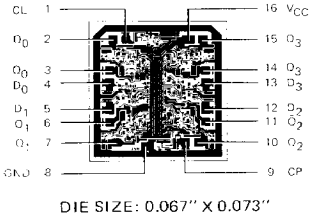
Metallization and Pad Layouts

Am54S/74S174



DIE SIZE: 0.070" X 0.083"

Am54S/74S175



DIE SIZE: 0.067" X 0.073"