Integrated Device Technology, Inc.

3.3V CMOS STATIC RAM 1 MEG (256K x 4-BIT) REVOLUTIONARY PINOUT

PRELIMINARY
IDT71V128

FEATURES:

- 256K x 4 advanced high-speed CMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise.
- Equal access and cycle times
  - — Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in a 32-pin 400 mil Plastic SOJ

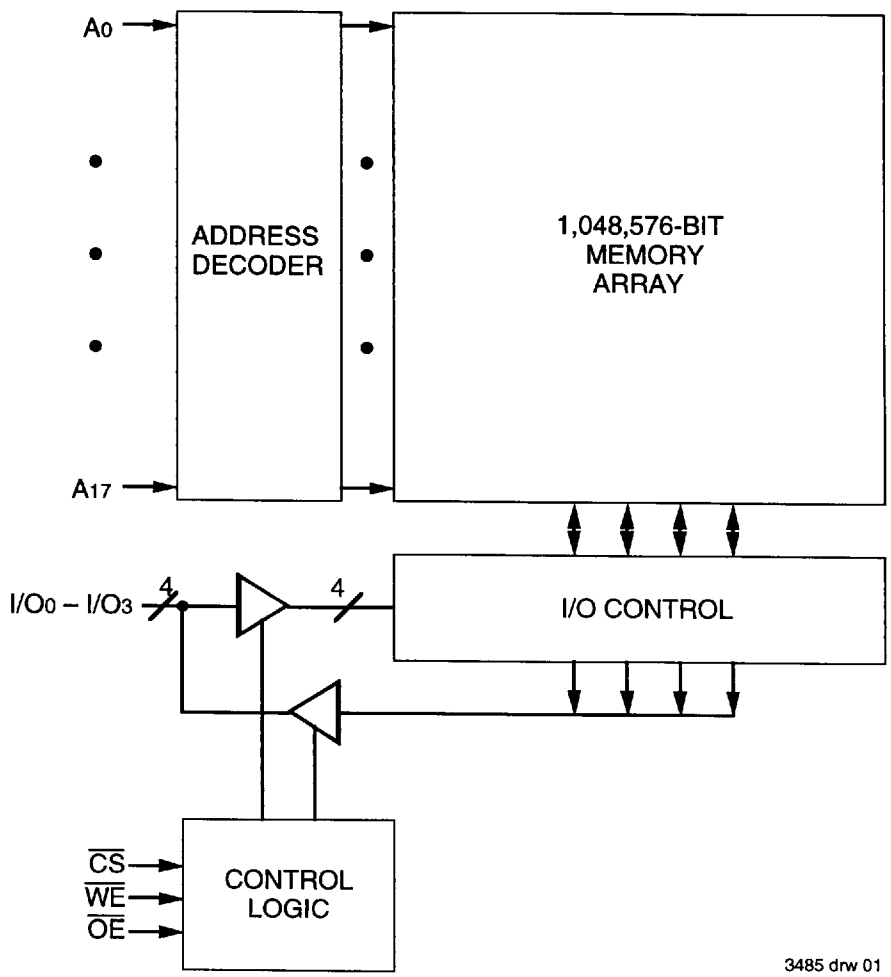
DESCRIPTION:

The IDT71V128 is a 1,048,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

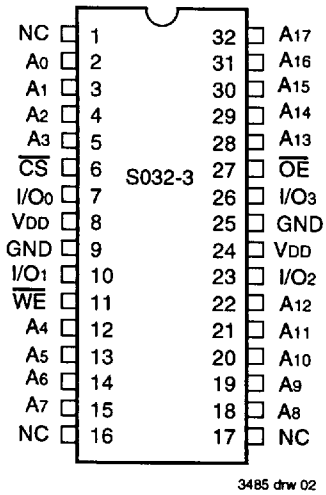
The IDT71V128 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71V128 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71V128 is packaged in a 32-pin 400 mil Plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



3485 drw 02

SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.1(2)	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

NOTES:
3485 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{TERM} must not exceed VDD + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES:
3485 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{DD} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE:
3485 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	VDD+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTE:
3485 tbl 04

1. V_{IL} (min.) = –1V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V ± 10%

Symbol	Parameter	Test Condition	IDT71V128		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = GND to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{DD}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8mA, V_{DD} = Min.	2.4	—	V

3483 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{DD} = 3.3V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter	71V128S12[3]		71V128S15		71V128S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current and $\overline{CS} \leq V_{IL}$, Outputs Open, V_{DD} = Max., f = f_{MAX}[2]	100	—	95	—	90	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{DD} = Max., f = f_{MAX}[2]	20	—	20	—	20	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{DD} = Max., f = 0[2], $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	5	—	5	—	5	—	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. 12ns specification is preliminary.

3484 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3485 tbl 07

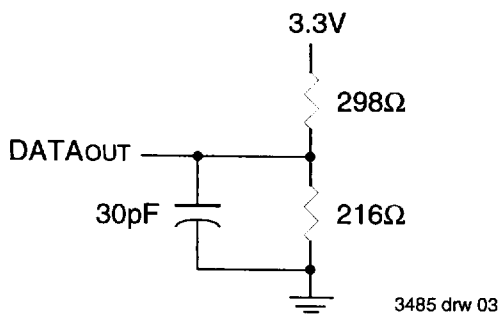
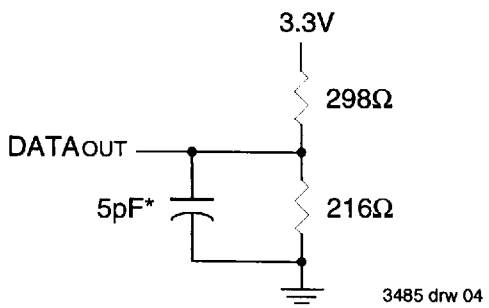


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

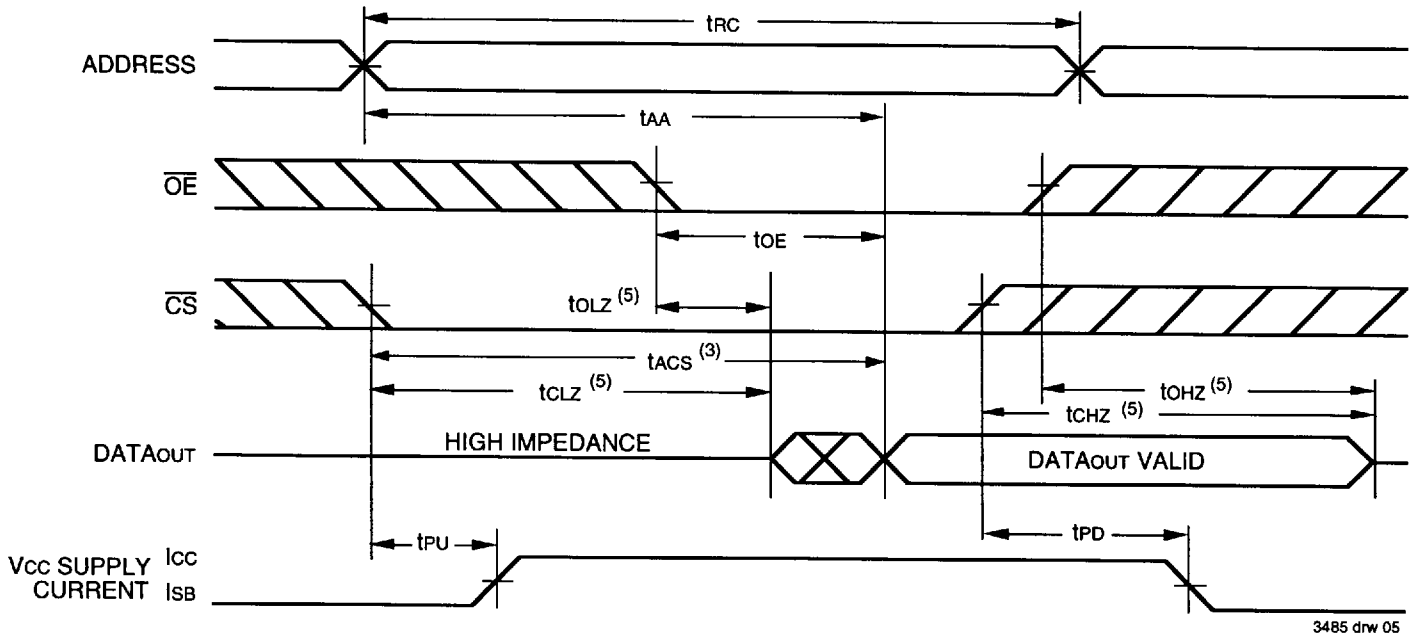
AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 10%, Commercial Range)

Symbol	Parameter	71V128S12[3]		71V128S15		71V128S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}[2]	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}[2]	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}[2]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[2]	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	12	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[2]	Output Active from End-of-Write	3	—	3	—	4	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

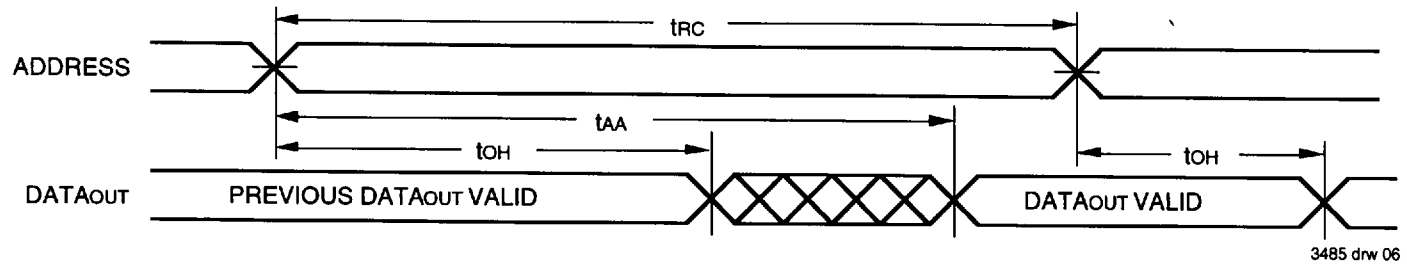
NOTES:
1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
3. 12ns specification is preliminary.

3484 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

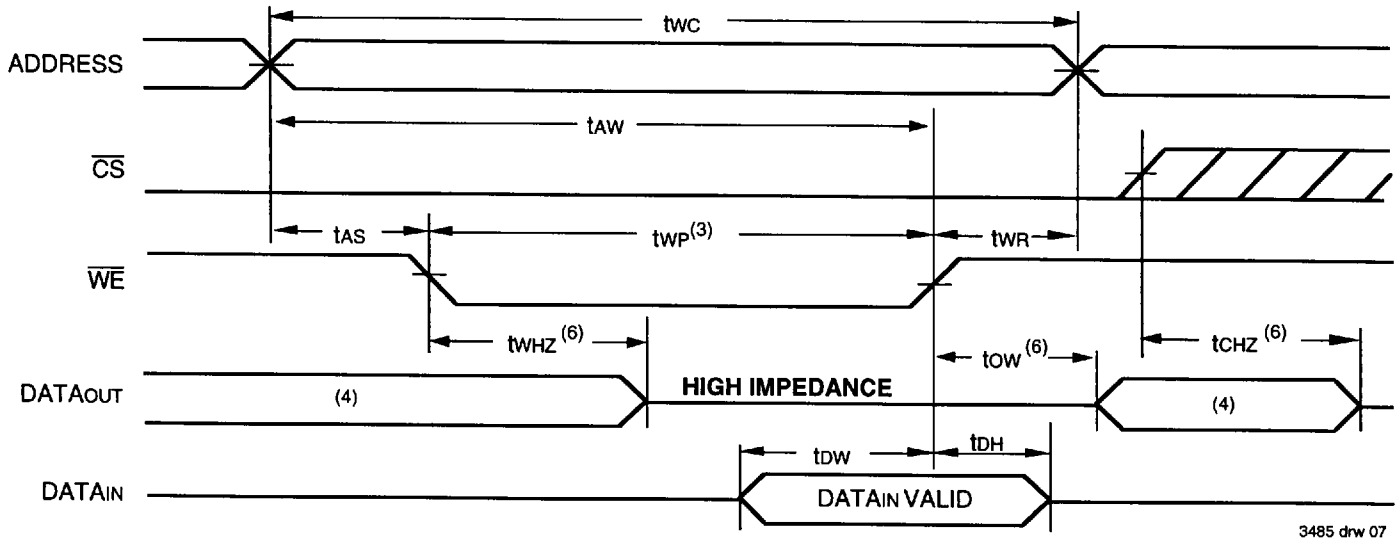


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

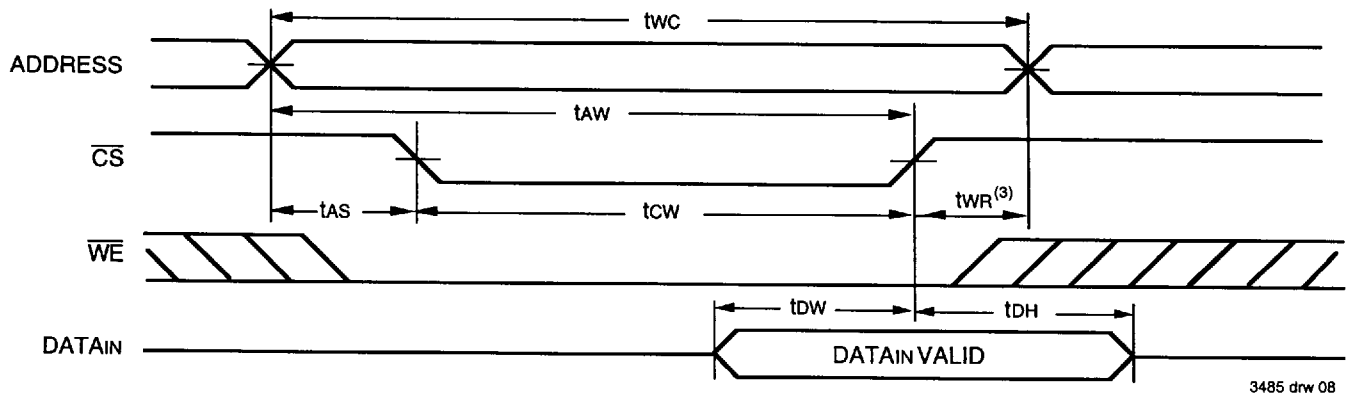


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)

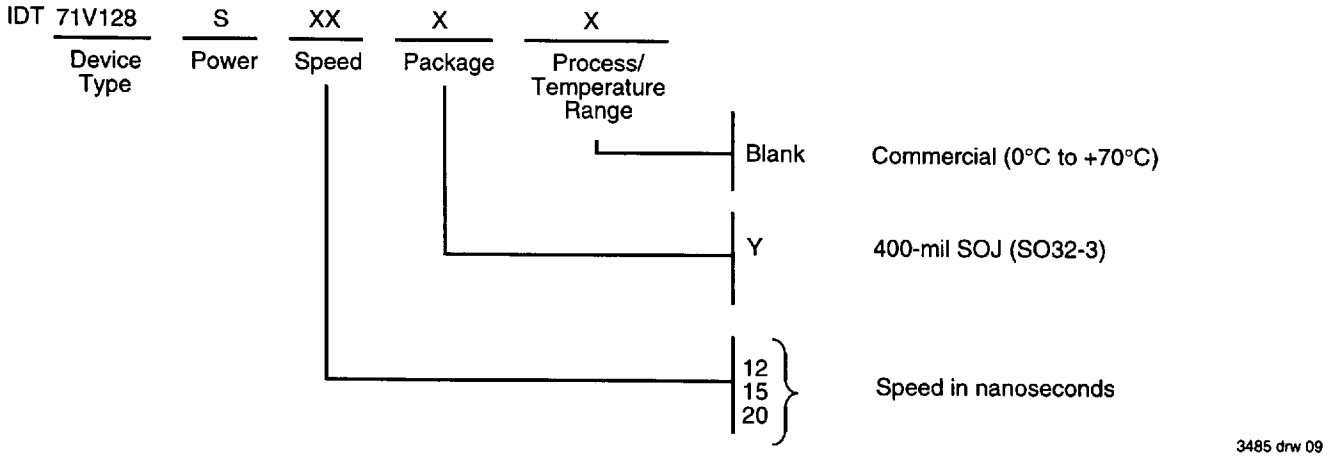


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the tCW write period.
6. Transition is measured ±200mV from steady state.

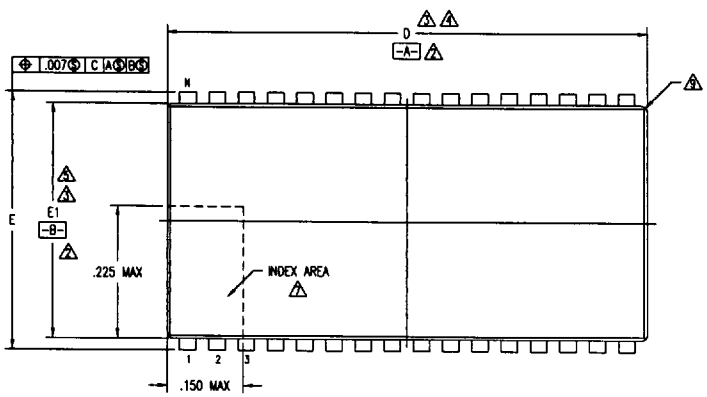
ORDERING INFORMATION

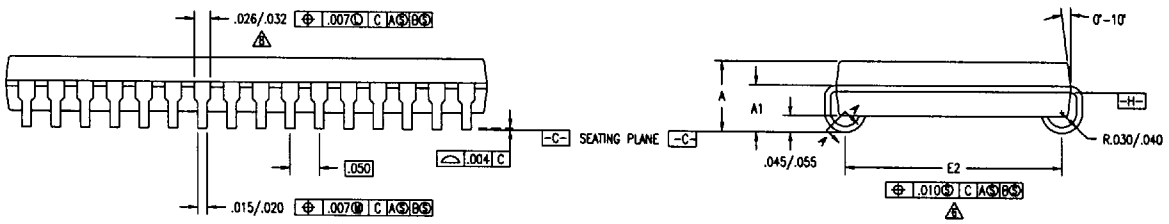


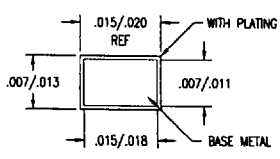
3485 drw 09

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20287	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. VU
27321	02	ADD A2 DIM	11/14/94	T. VU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
27945	04	ADD 44 LD	06/25/95	







SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE	PB PACKAGE OUTLINE .400" BODY WIDTH SOJ .050" PITCH
DRAWN AA	02/15/96		
CHECKED		SIZE C	DRAWING No. PSC-4033 REV 04
		DO NOT SCALE DRAWING	

SOJ (Continued)

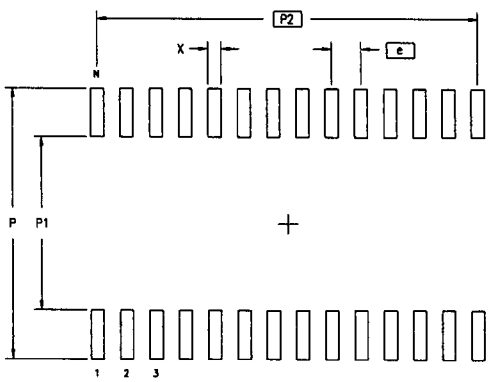
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20287	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. VU
27321	02	ADD A2 DIM	11/14/94	T. VU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
27945	04	ADD 44 LD	08/25/95	

JEDEC #	SO28-6			
SYMBOL	JEDEC VARIATION AA			NOTE
	MIN	NOM	MAX	
A	.131	.138	.145	
A1	.082	–	–	
D	.720	.725	.730	3,4
E	.435	.440	.445	
E1	.395	.400	.405	3,5
E2	.360	.370	.380	6
N	28			

JEDEC #	SO32-3			
	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.131	.138	.145	
A1	.082	–	–	
D	.820	.825	.830	3,4
E	.435	.440	.445	
E1	.395	.400	.405	3,5
E2	.360	.370	.380	6
N	32			

JEDEC #	SO44-1			
	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX	
A	.131	.138	.145	
A1	.082	–	–	
D	1.120	1.125	1.130	3,4
E	.435	.440	.445	
E1	.395	.400	.405	3,5
E2	.360	.370	.380	6
N	44			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	.458	.466	.458	.466	.458	.466
P1	.290	.294	.290	.294	.290	.294
P2	.650 BSC		.750 BSC		1.050 BSC	
X	.018	.026	.018	.026	.018	.026
e	.050 BSC		.050 BSC		.050 BSC	
N	28		32		44	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
6. DIMENSION E2 TO BE DETERMINED AT SEATING PLANE -C- CONTACT POINT
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-061, VARIATION AA, AB & AE

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