



## 128K × 8 CMOS STATIC RAM

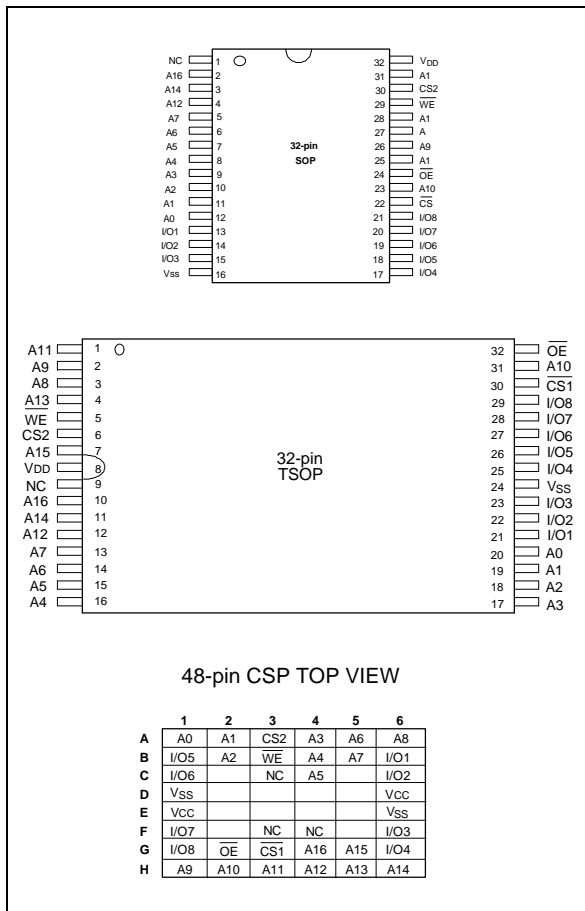
### GENERAL DESCRIPTION

The W24L01 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 2.3V to 3.3V power supply. The W24L01 family, W24L01-LE and W24L01-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

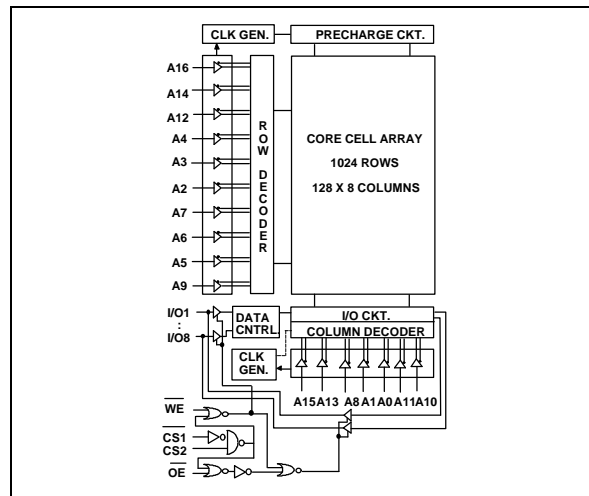
### FEATURES

- Low power consumption:
  - Active: 132 mW (max.)
  - Standby: 13.5 μW (max.) / 2.5V ±0.2V  
16.5 μW (max.) / 3.0V ±0.3V
- Access time: 70 nS / 100 nS (max.)
- 2.3V to 3.3V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Packaged in 32-pin 450 mil SOP, standard type one TSOP (8 mm × 20 mm), small type one TSOP (8 mm × 13.4 mm) and 48-pin CSP

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection



## TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to +4.6	V
Input/Output to Vss Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	LE	-20 to 85
	LI	-40 to 85

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(VDD = 3.0V ±0.3V; VDD = 2.5V ±0.2V, Vss = 0V; TA (°C) = -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	3.0V			2.5V			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Input Low Voltage	VIL	-	-0.2	-	+0.4	-0.2	-	+0.4	V
Input High Voltage	VIH	-	+2.2	-	VDD +0.3	+2.0	-	VDD +0.2	V
Input Leakage Current	ILI	VIN = Vss to VDD	-1	-	+1	-1	-	+1	µA
Output Leakage Current	ILO	VI/O = Vss to VDD, CS1 = VIH (min.) or CS2 = VIL (max.) or OE = VIH (min.) or WE = VIL (max.)	-1	-	+1	-1	-	+1	µA
Output Low Voltage	VOL	IOL = +2.1 mA, VDD = 3.0V IOL = +0.5 mA, VDD = 2.5V	-	-	0.4	-	-	0.4	V
Output Low Voltage	VOH	IOH = -1.0 mA, VDD = 3.0V IOH = -0.5 mA, VDD = 2.5V	2.2	-	-	2.0	-	-	V



Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	3.0V			2.5V			UNIT
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Operating Power Supply Current	I <sub>DD</sub>	$\overline{CS1} = V_{IL} \text{ (max.)}$ and $CS2 = V_{IH} \text{ (min.)}$ , I/O = 0 mA, Cycle = min. Duty = 100%	-	-	45	-	-	25	mA
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS1} = V_{IH} \text{ (min.)}$ or $CS2 = V_{IL} \text{ (max.)}$ , Cycle = min. Duty = 100%	-	-	0.3	-	-	0.3	mA
	I <sub>SB1</sub>	$\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	-	0.5	5	-	0.5	5	μA

Note: Typical parameter is measured under ambient temperature  $T_A = 25^\circ \text{C}$  and  $V_{DD} = 3.0V / 2.5V$

## CAPACITANCE

( $T_A = 25^\circ \text{C}$ ,  $f = 1 \text{ MHz}$ )

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	$V_{IN} = 0V$	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	$V_{OUT} = 0V$	10	pF

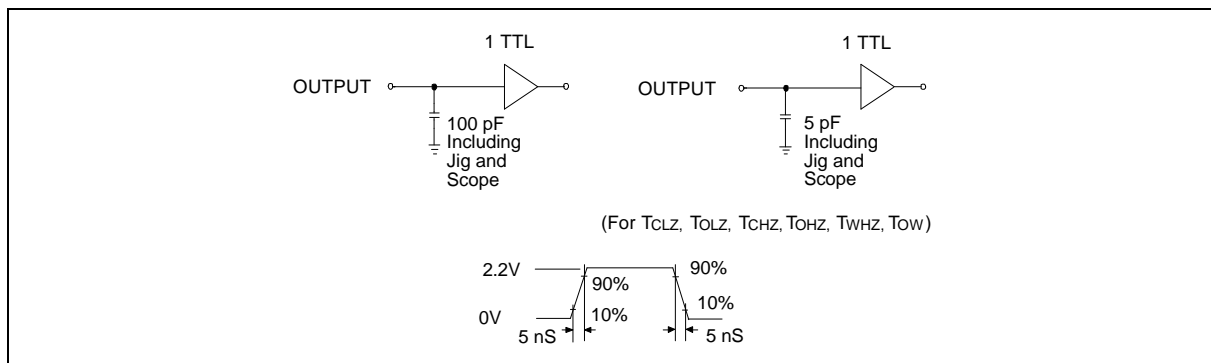
Note: These parameters are sampled but not 100% tested.

## AC CHARACTERISTICS

### AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 2.2V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V, $V_{DD} = 3.0V$
	1.1V, $V_{DD} = 2.5V$
Output Load	See the drawing below

### AC Test Loads and Waveform





AC Characteristics, continued

(V<sub>DD</sub> = 3.0V ±0.3V; V<sub>DD</sub> = 2.5V ±0.2V; V<sub>SS</sub> = 0V; T<sub>A</sub> (°C) = -20 to 85 for LE, -40 to 85 for LI)**Read Cycle**

PARAMETER	SYM.	3.0V		2.5V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	100	-	nS
Address Access Time	TAA	-	70	-	100	nS
Chip Select Access Time	TACS	-	70	-	100	nS
Output Enable to Output Valid	TAOE	-	35	-	50	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	15	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	30	-	35	nS
Output Hold from Address Change	TOH	10	-	15	-	nS

\* These parameters are sampled but not 100% tested

**Write Cycle**

PARAMETER	SYM.	3.0V		2.5V		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	70	-	100	-	nS
Chip Selection to End of Write	TCW	60	-	70	-	nS
Address Valid to End of Write	TAW	60	-	70	-	nS
Address Setup Time	TAS	0	-	0	-	nS
Write Pulse Width	TWP	55	-	70	-	nS
Write Recovery Time	$\overline{CS1}$ , $CS2$ , $\overline{WE}$ TWR	0	-	0	-	nS
Data Valid to End of Write	TDW	30	-	50	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	25	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	35	nS
Output Active from End of Write	TOW	5	-	10	-	nS

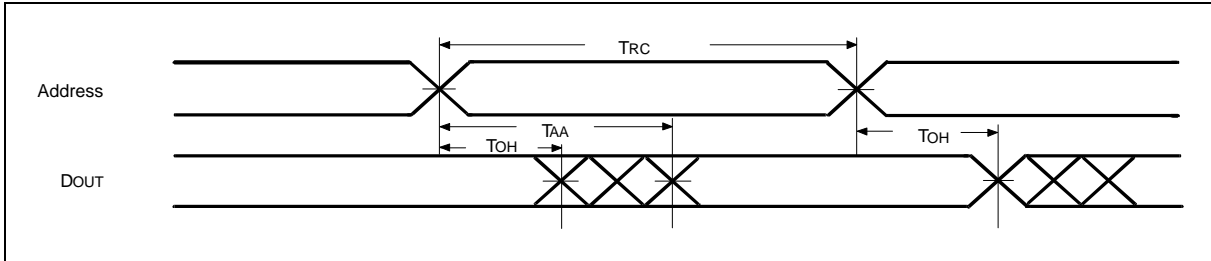
\* These parameters are sampled but not 100% tested



**TIMING WAVEFORMS**

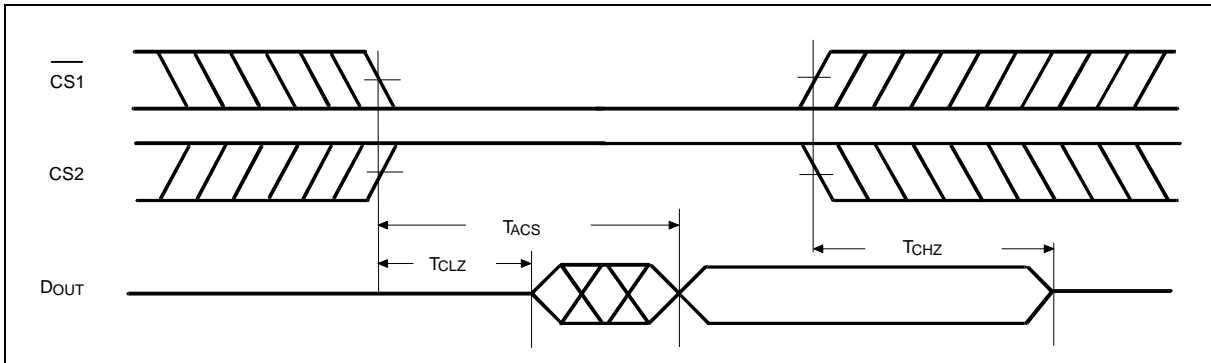
**Read Cycle 1**

(Address Controlled)



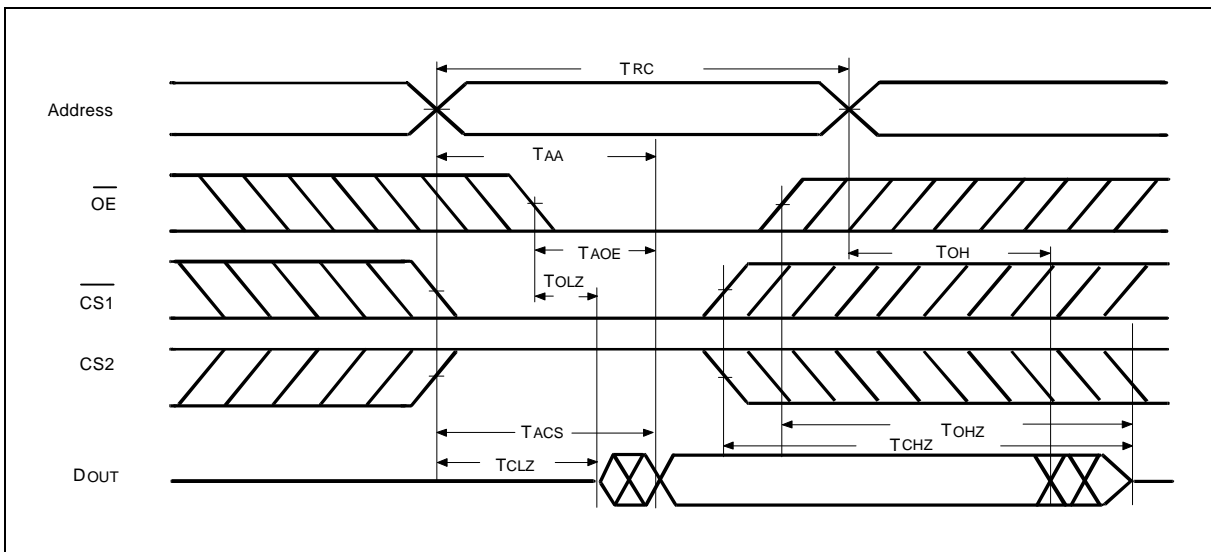
**Read Cycle 2**

(Chip Select Controlled)



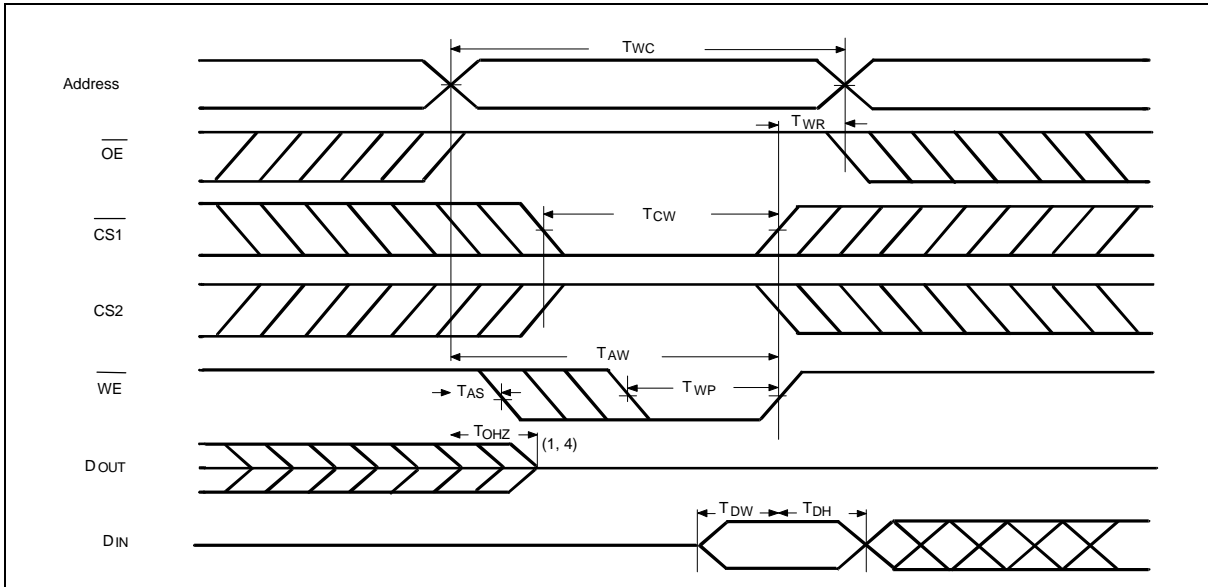
**Read Cycle 3**

(Output Enable Controlled)



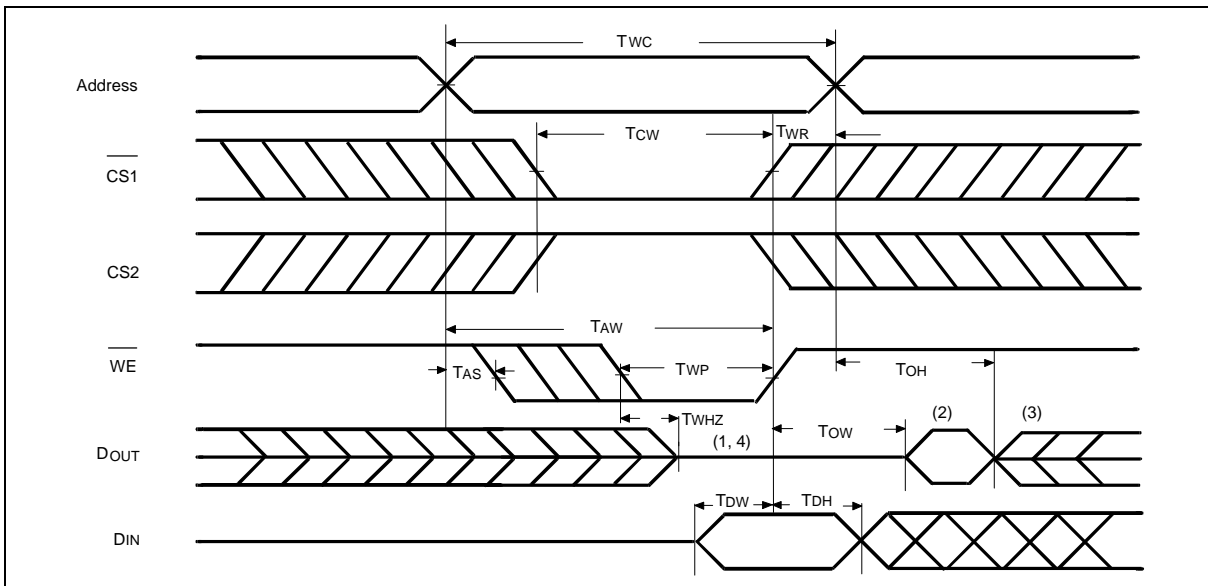
Timing Waveforms, continued

## Write Cycle 1



## Write Cycle 2

( $\overline{OE} = V_{IL}$  Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured  $\pm 500$  mV from steady state with  $C_L = 5$  pF. This parameter is guaranteed but not 100% tested.



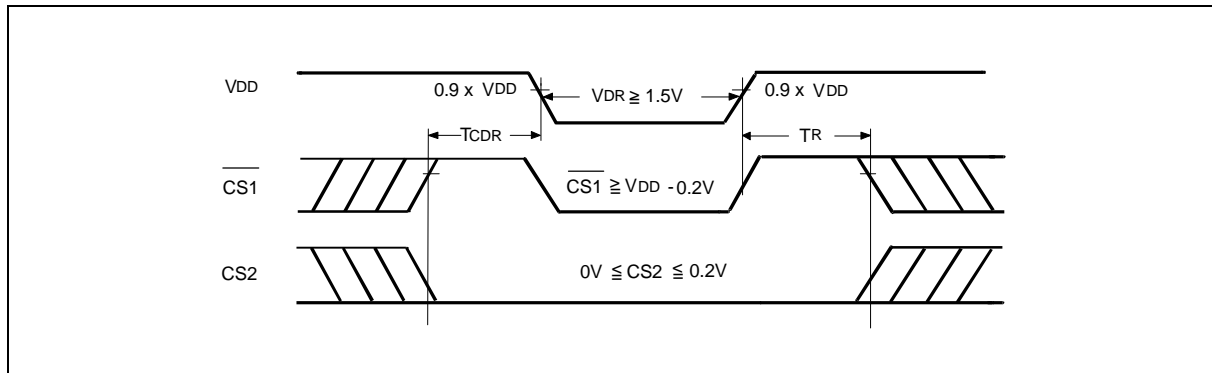
## DATA RETENTION CHARACTERISTICS

(TA (°C) = -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	1.5	-	-	V
Data Retention Current	I <sub>DDDR</sub>	$\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V, V_{DD} = 3V$	-	-	5	μA
Chip Deselect to Data Retention Time	T <sub>CDR</sub>	See data retention waveform	0	-	-	nS
Operation Recovery Time	T <sub>R</sub>		T <sub>RC</sub> *	-	-	nS

\* Read Cycle Time

## DATA RETENTION WAVEFORM





## ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	PACKAGE
W24L01B-70LE	100/70	2.5V/3V	-20 to 85	CSP
W24L01Q-70LE	100/70	2.5V/3V	-20 to 85	Small type one TSOP
W24L01S-70LE	100/70	2.5V/3V	-20 to 85	450 mil SOP
W24L01T-70LE	100/70	2.5V/3V	-20 to 85	Standard type one TSOP
W24L01B-70LI	100/70	2.5V/3V	-40 to 85	CSP
W24L01Q-70LI	100/70	2.5V/3V	-40 to 85	Small type one TSOP
W24L01S-70LI	100/70	2.5V/3V	-40 to 85	450 mil SOP
W24L01T-70LI	100/70	2.5V/3V	-40 to 85	Standard type one TSOP

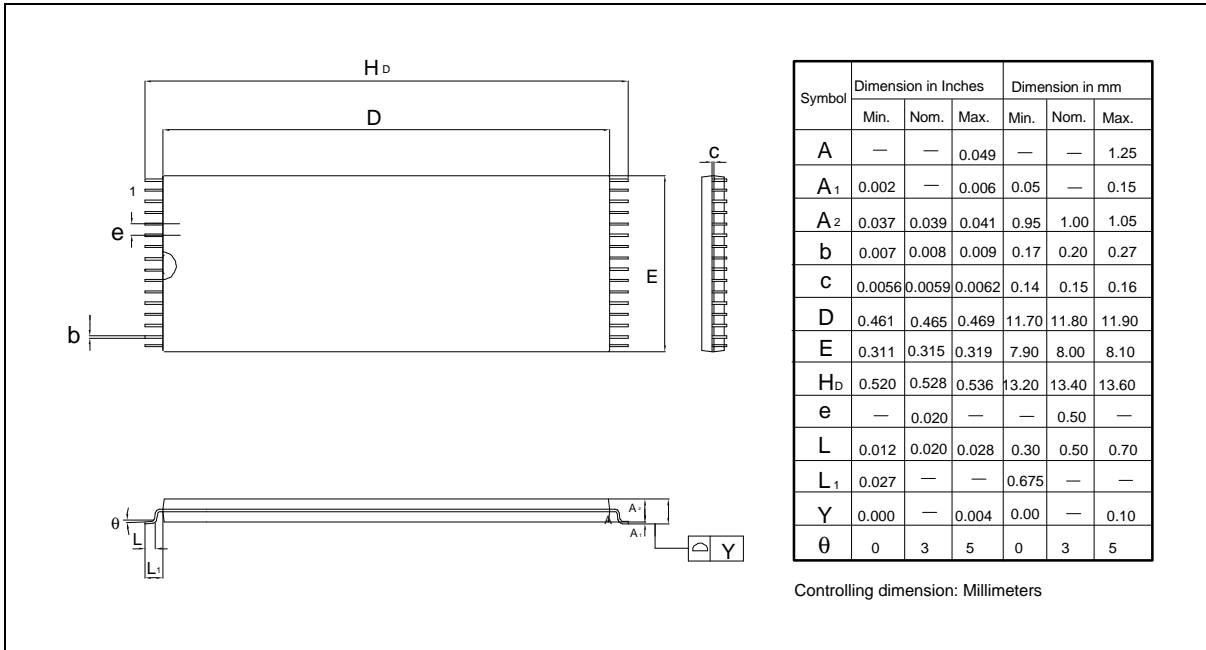
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

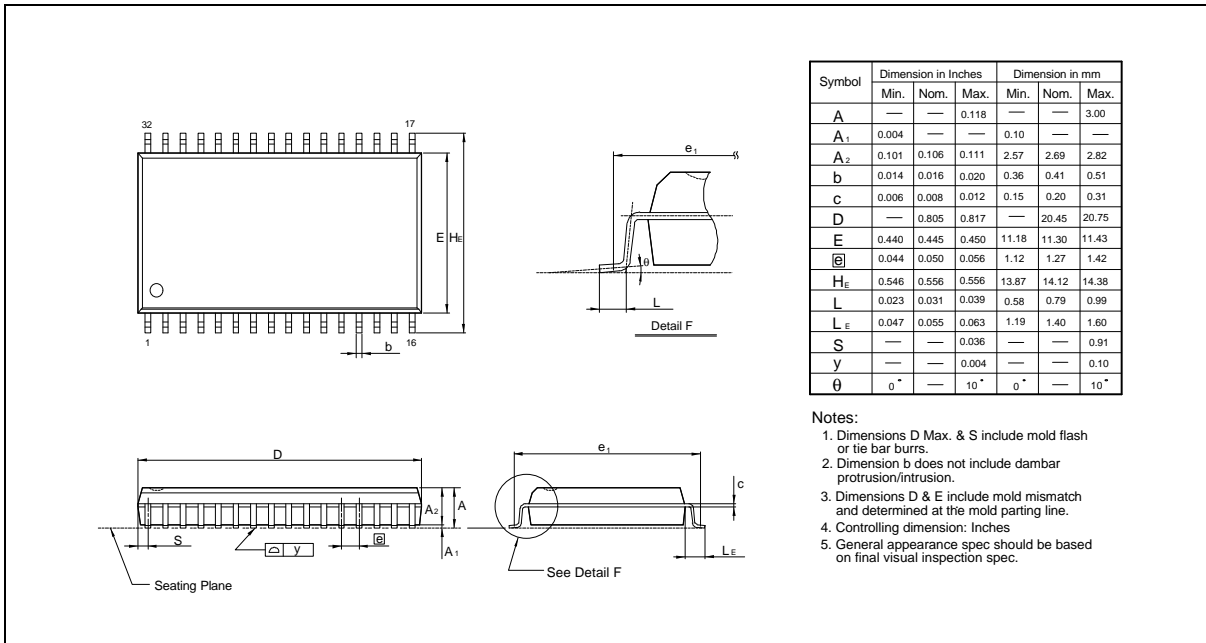


## PACKAGE DIMENSIONS

### 32-pin Small Type One TSOP

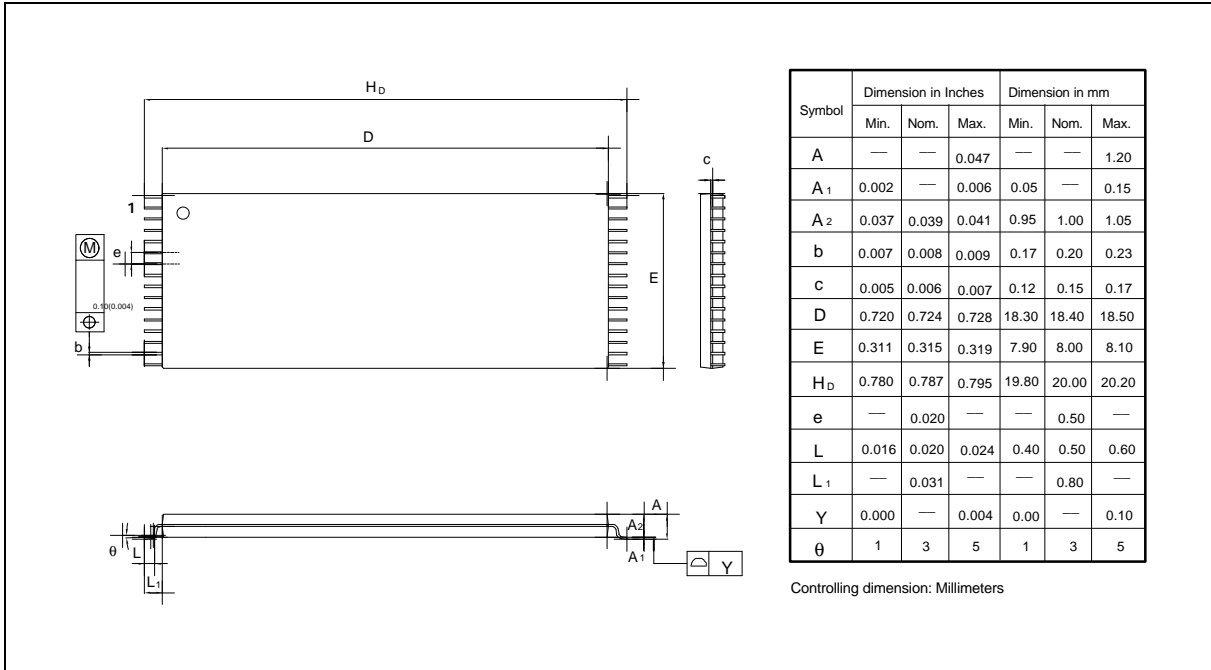


### 32-pin SOP Wide Body



Package Dimensions, continued

## 32-pin Standard Type One TSOP





## VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Feb. 1998		Initial Issued
A2	Apr. 1998	3	Add standby power supply current (ISB1) typical parameter when operation temperature $T_A = 25^\circ \text{C}$
A3	June 1998	1	Change supply voltage range: from (2.7V to 3.6V) to (2.3V to 3.3V) Modify power consumption: - Active : 132 mW (max.) - Standby: 13.5 $\mu\text{W}$ (max.) /2.5V $\pm 0.2$ 16.5 $\mu\text{W}$ (max.) /3.0V $\pm 0.3$
		2, 3	Correct Operating Characteristics: $V_{IL}$ from (-0.5V to +0.6V) to (-0.2V to +0.4V) $V_{IH}$ (max.) from $V_{DD} + 0.5\text{V}$ to $V_{DD} + 0.3\text{V}$ for 3.0V from $V_{DD} + 0.5\text{V}$ to $V_{DD} + 0.2\text{V}$ for 2.5V $I_{DD}$ (max.) from 20 mA to 45 mA for 3.0V from 20 mA to 25 mA for 2.5V $I_{SB}$ (max.) from 1 mA to 0.3 mA Modify $V_{OL}$ , $V_{OH}$ test conditions
		3	Correct Capacitance: $C_{IN}$ (max.) from 6 pF to 8 pF $C_{I/O}$ (max.) from 8 pF to 10 pF Correct AC Characteristics and AC Test Waveform Input Pulse Levels from (0V to 2.4V) to (0V to 2.2V) Input and Output Timing Reference Level from 1.2V to 1.5V for 3.0V form 1.2V to 1.1V for 2.5V
		4	$T_{WHZ}^*$ , $T_{OHZ}^*$ from 30 nS to 35 nS $T_{CW}$ from 50 nS to 60 nS for 3V $T_{AW}$ from 50 nS to 60 nS for 3V $T_{WP}$ from 50 nS to 55 nS for 3V
		7	Correct $V_{DR}$ (min.) from 2.0V to 1.5V
		8	Modify Ordering Information: access time (nS)    operating voltage(V) -70                    2.7V to 3.0V -100                   2.3V to 2.7V W24L01-LI operating temperature( $^\circ\text{C}$ ) from -20-85 to -40-85
A4	Oct. 1998	1, 8, 9	Add SOP package type
A5	Jan. 1999	1	Add SOP package pin configuration



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Note: All data and specifications are subject to change without notice.