DATA SHEET

L 65764

8 K x 8 / 3.3 VOLTS HIGH SPEED CMOS SRAM

FEATURES

- **SINGLE SUPPLY 3.3 V ± 0.3 V**
- **FAST ACCESS TIME**
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 216 mW (typ)
  STANDBY : 120mW (typ)
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

INTRODUCTION

The L 65764 is a high speed CMOS static RAM organized as 8192x8 bits. It is manufactured using MHS high performance CMOS technology.
Access times as fast as 25 ns are available with maximum power consumption of only 450 mW.
The L 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

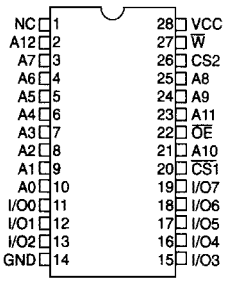
Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
L 65764 provides fast access time with 3 volts power supply, perfectly designed for portable applications. (PC cache memory... etc)
The L 65764 is processed following the test methods of MIL STD 883C.

7

INTERFACE

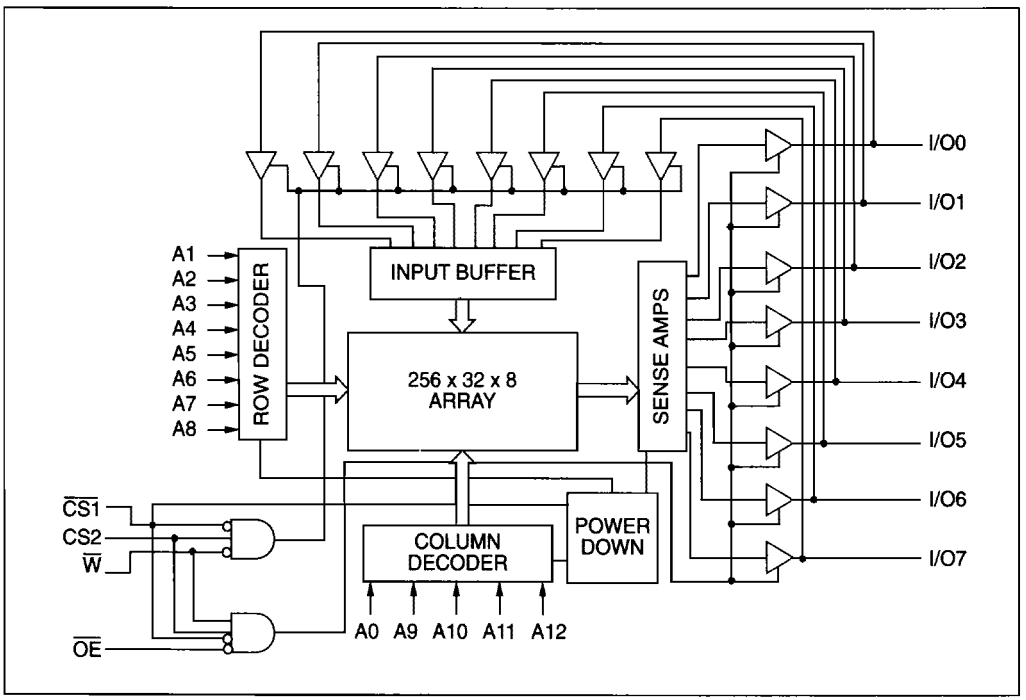
PIN CONFIGURATION

SOIC & SOJ 300 mils, 28 pins, DIL.
SOIC 330 mils, 28 pins
Plastic 300 & 600 mil, 28 pins, DIL
Ceramic 300 mils, 600 mils, 28 pins, DIL

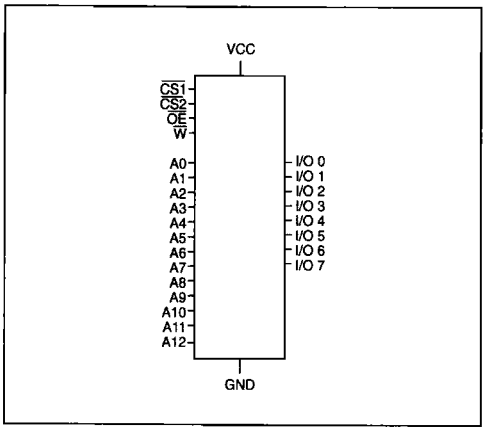


Pinout DIL/SOIC/SOJ 28 pins (top view)

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A13	: Address inputs	$\overline{CS1}$	: Chip-select 1
I/O0-I/O7	: Inputs/Outputs	CS2	: Chip Select 2
VCC	: Power	$\overline{OE}$	: Output enable
GND	: Ground	$\overline{W}$	: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low – H = high – X = H or L – Z = High impedance.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Commercial	3.3 V ± 0.3 %	0°C to + 70°C

7

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

CONSUMPTION FOR COMMERCIAL SPECIFICATION (– 5)

SYMBOL		PARAMETER	L 65764 – 25	L 65764 – 35	L 65764 – 45	L 65764 – 55	UNIT	VALUE
ICCSB	(6)	Standby supply current	30	30	30	30	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	125	125	125	125	mA	max

AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 10 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) + 30 pF

AC TEST LOAD AND WAVEFORMS

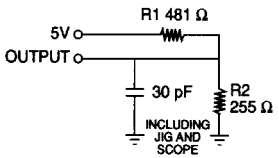


Figure 1 a

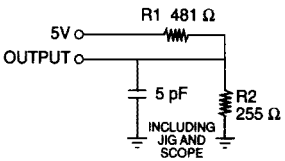


Figure 1 b

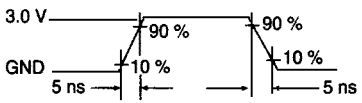
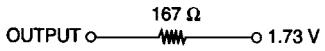


Figure 2

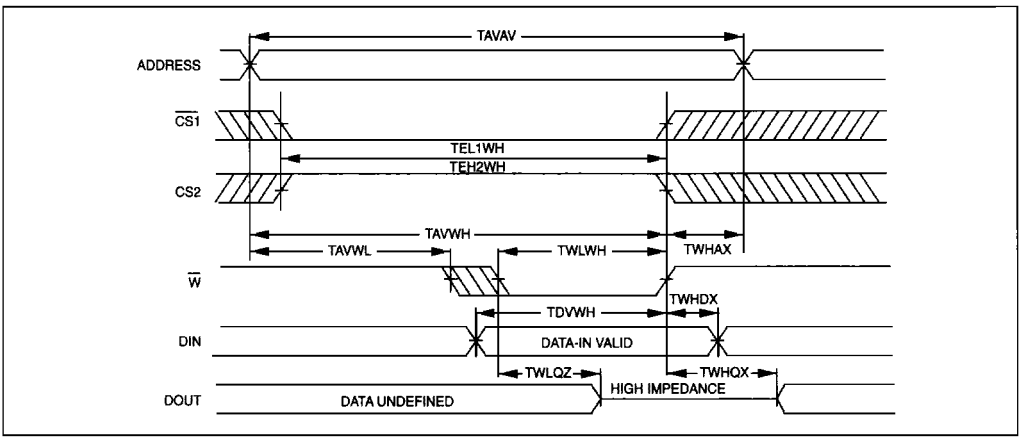
Equivalent to : THEVENIN EQUIVALENT



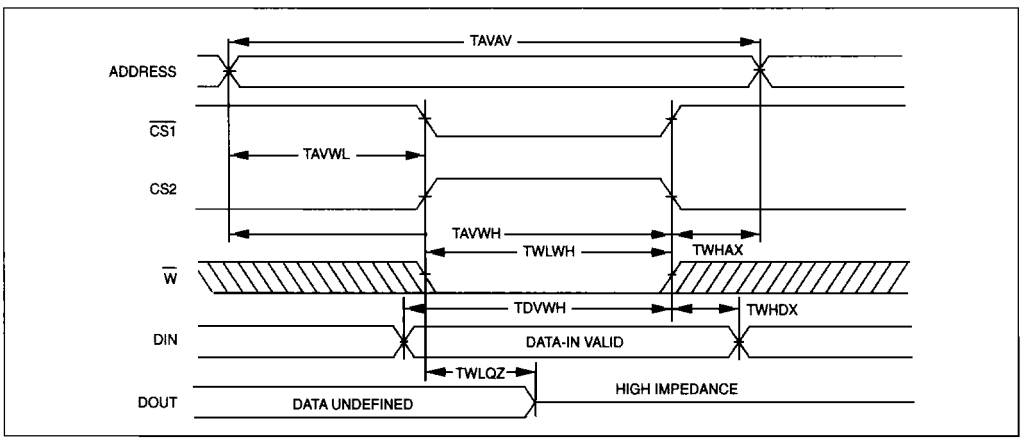
WRITE CYCLE : COMMERCIAL SPECIFICATION

SYMBOL	PARAMETER	L 65764 -25	L 65764 -35	L 65764 -45	L 65764 -55	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end write	20	25	30	40	ns	min
TDVWH	Data set-up time	17	20	20	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	20	25	30	40	ns	min
TEH2WH	CS2 high to write end	20	20	25	30	ns	min
TWLQZ (9)	Write low to high Z	12	12	15	20	ns	max
TWLWH	Write pulse width	15	20	20	25	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	5	5	5	5	ns	min

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 9)



7

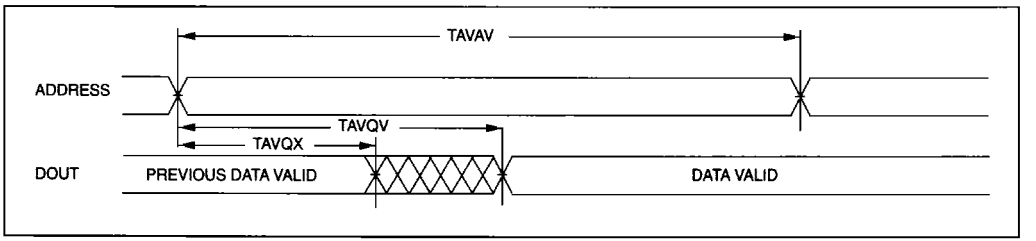
Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE}$ = VIH.

READ CYCLE : COMMERCIAL SPECIFICATION

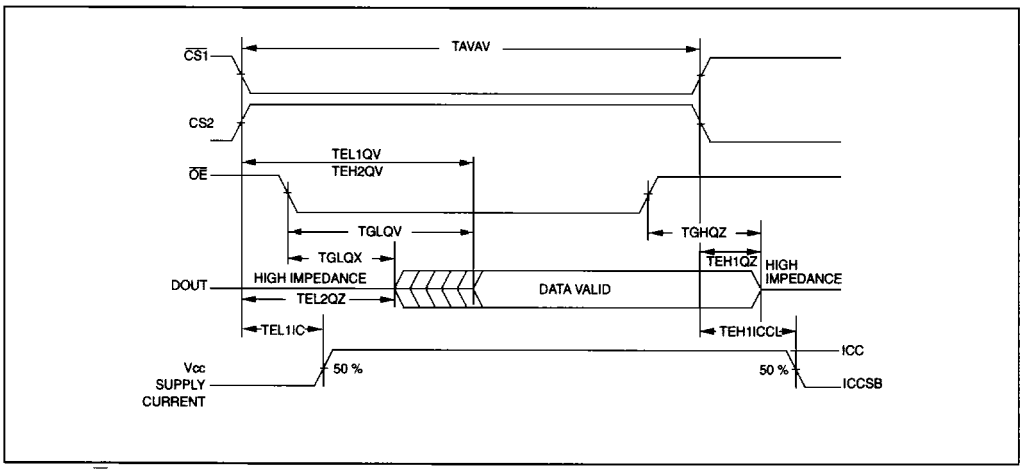
SYMBOL	PARAMETER	L 65764 -25	L 65764 -35	L 65764 -45	L 65764 -55	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	10	15	15	20	ns	max
TEL2QZ (11)	CS2 low to high Z	10	15	15	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEH1ICCL	CS1 high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	20	ns	max

7

READ CYCLE nb 1 (notes 10, 11)



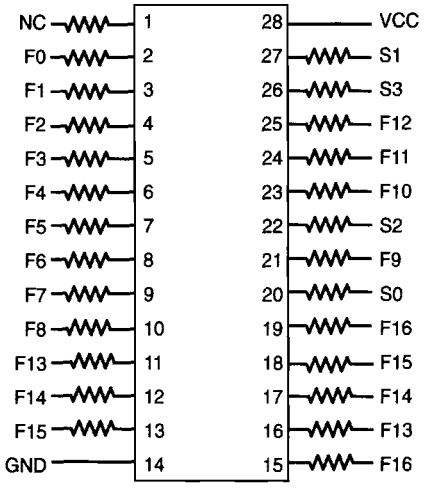
READ CYCLE nb 2 (notes 10, 12)

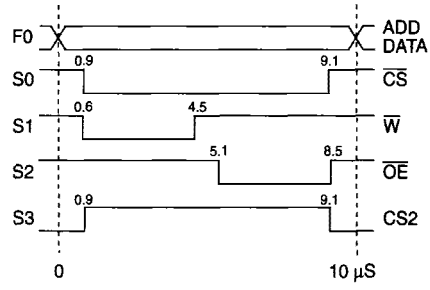


Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{CS_1}$ & $\overline{OE}$ = VIL and CS_2 = VIH.
12. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW.

7

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
FO = 50 KHz ± 20 %

Fn = 1/2 F n-1
S0 to S3 : programmable signals for write / read cycles
NC = Not connected

ORDERING INFORMATION

TEMPERATURE		PACKAGE		DEVICE TYPE	GRADE	FLOW
C	L	UI	–	65764	– 25	: RD

C : Commercial

0 - Chip form
1P - Ceramic 28 pins 300 mils
1E - Ceramic 28 pins 600 mils
3P - Plastic 28 pins 300 mils
3I - Plastic 28 pins 600 mils
TI - SOIC 28 pins 300 mils
TP - SOIC 28 pins 330 mils
UI - SOJ 28 pins

8 k x 8 High speed static RAM

– 25 = 25 ns
– 35 = 35 ns
– 45 = 45 ns
– 55 = 55 ns

: R Tape and Reel
: RD Tape and Reel Dry Pack

7