2SJ451

Silicon P Channel MOS FET

REJ03G0864-0400
Rev.4.00
Sep 07, 2007

Description

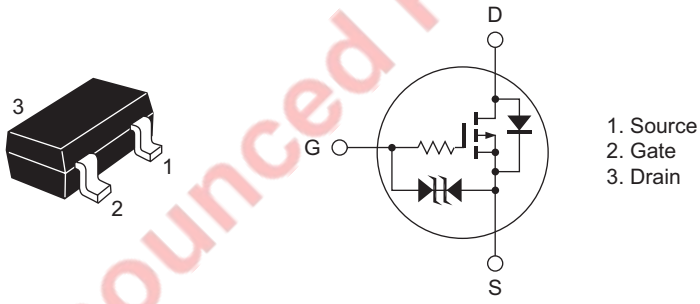
Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5 V gate drive device.
- Small package (MPAK).

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is “ZK–”.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	–0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%

Electrical Characteristics

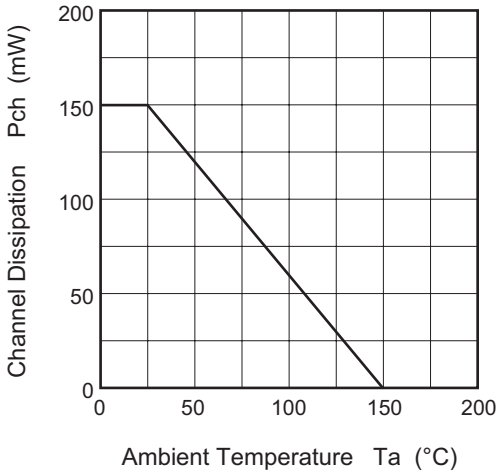
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	–20	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1.0	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	–0.5	—	–1.5	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS\ (on)\ 1}$	—	2.3	3.5	Ω	I_D = –100 mA, V_{GS} = –4 V Note 2
	$R_{DS\ (on)\ 2}$	—	5.0	9.0	Ω	I_D = –40 mA, V_{GS} = –2.5 V Note 2
Forward transfer admittance	$\|y_{fs}\|$	0.13	0.23	—	S	I_D = –100 mA, V_{DS} = –10 V Note 2
Input capacitance	Ciss	—	2.4	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	31	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.6	—	pF	f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	170	—	ns	I_D = –0.1 A
Rise time	t_r	—	680	—	ns	V_{GS} = –10 V
Turn-off delay time	$t_{d\ (off)}$	—	3.0	—	µs	R_L = 100 Ω
Fall time	t_f	—	2.8	—	µs	

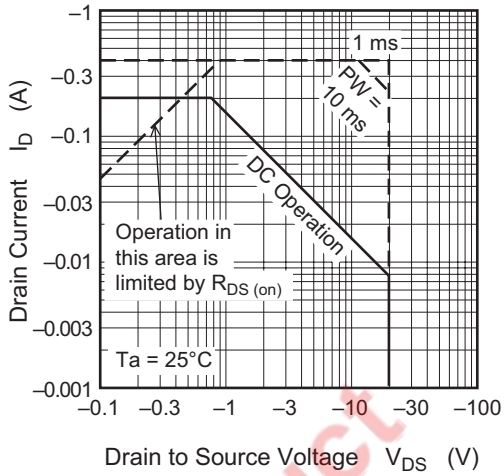
Note: 2. Pulse test

Main Characteristics

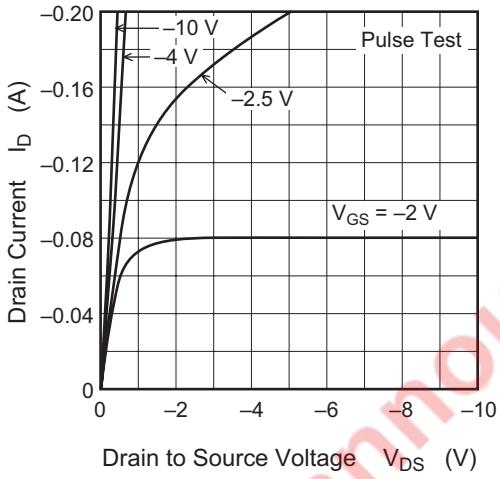
Maximum Channel Dissipation Curve



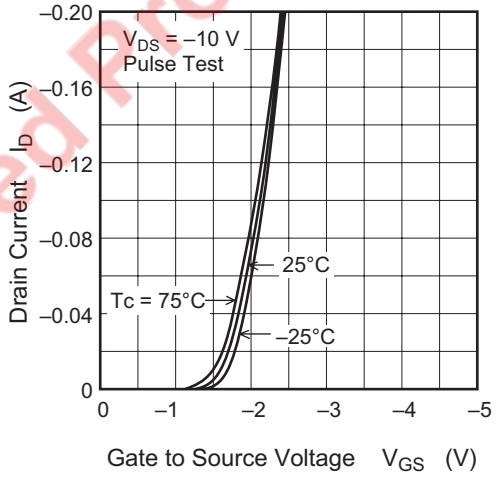
Maximum Safe Operation Area



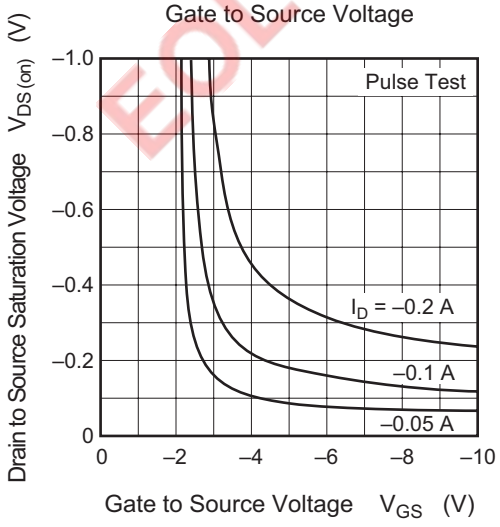
Typical Output Characteristics



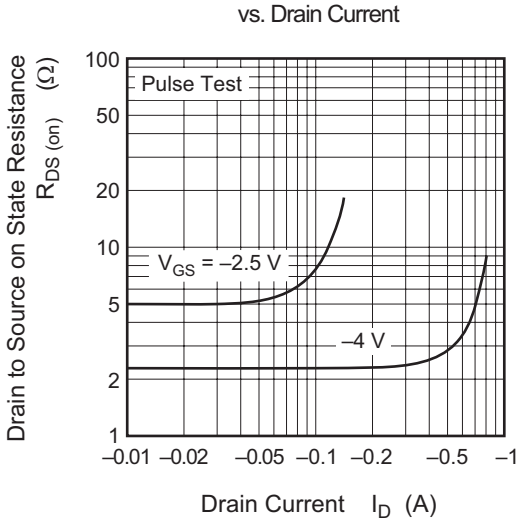
Typical Transfer Characteristics



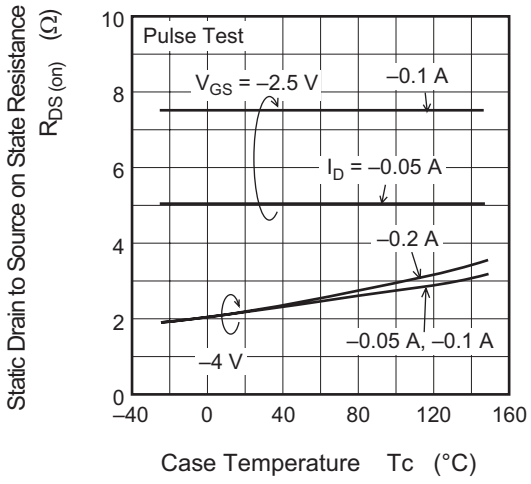
Drain to Source Saturation Voltage vs. Gate to Source Voltage



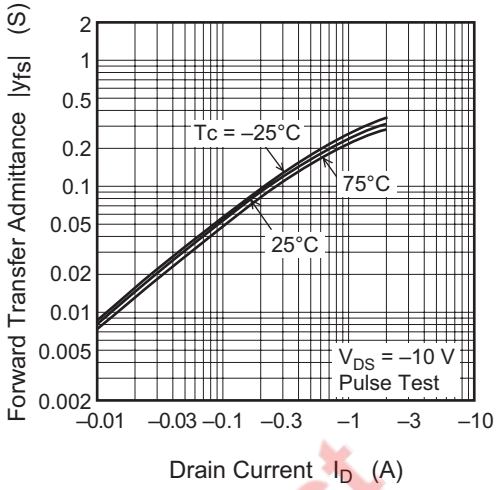
Static Drain to Source on State Resistance vs. Drain Current



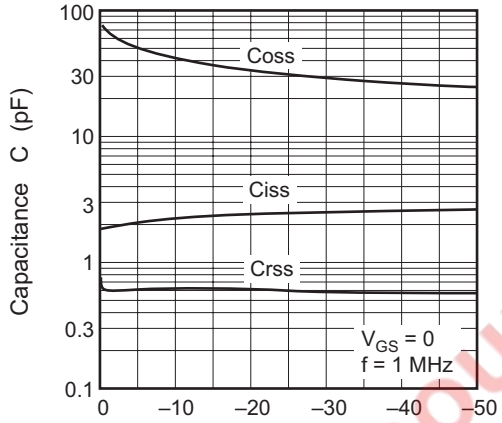
Static Drain to Source on State Resistance vs. Temperature



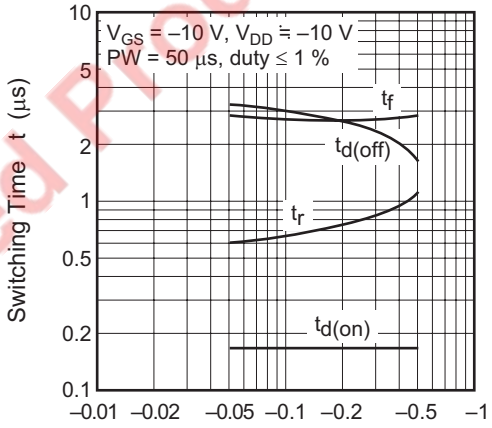
Forward Transfer Admittance vs. Drain Current



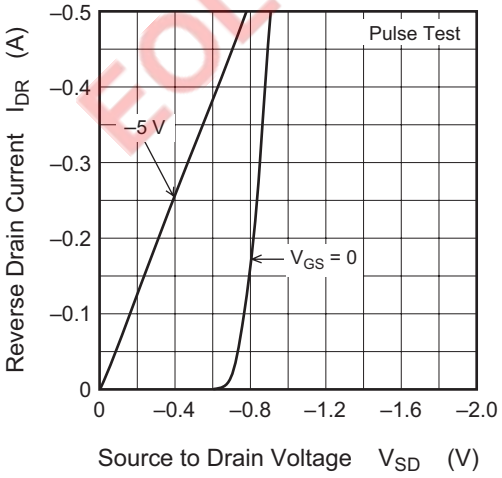
Typical Capacitance vs. Drain to Source Voltage



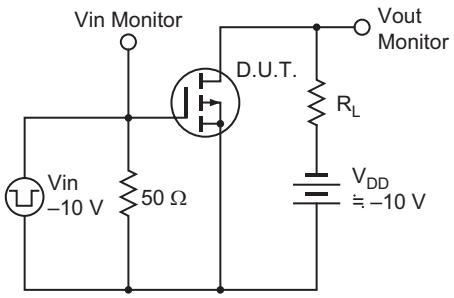
Switching Characteristics



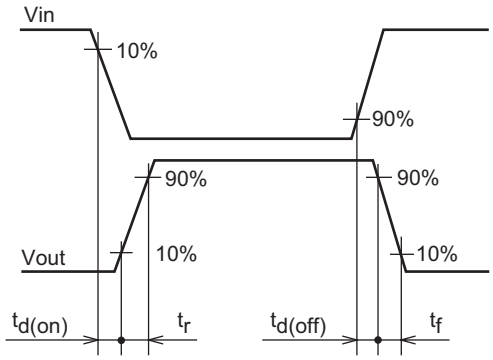
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit

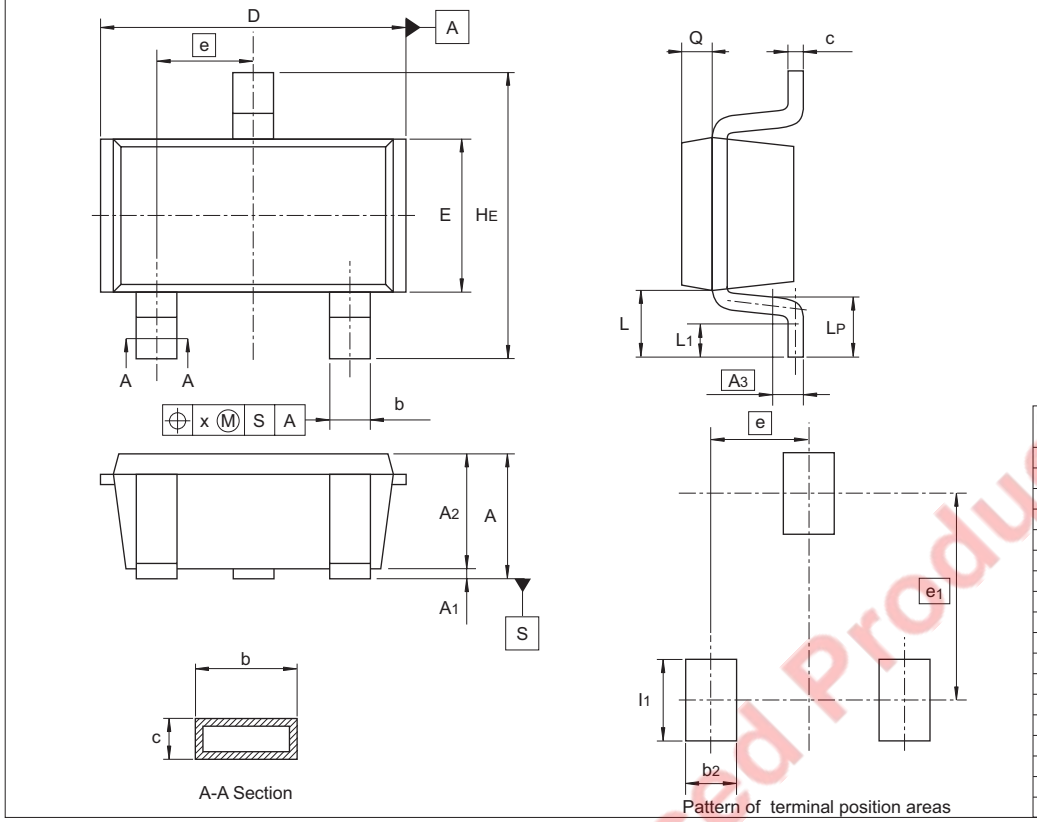


Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MPAK	SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	–	1.3
A_1	0	–	0.1
A_2	1.0	1.1	1.2
A_3	–	0.25	–
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	–	3.1
E	1.35	1.5	1.65
e	–	0.95	–
H_E	2.2	2.8	3.0
L	0.35	–	0.75
L_1	0.15	–	0.55
L_P	0.25	–	0.65
x	–	–	0.05
b_2	–	–	0.55
e_1	–	1.95	–
l_1	–	–	1.05
Q	–	0.3	–

Ordering Information

Part Name	Quantity	Shipping Container
2SJ451ZK-TL-E	3000 pcs	Taping
2SJ451ZK-TR-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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