



Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTER

IDT29FCT520A
IDT29FCT520B
IDT29FCT520C

FEATURES:

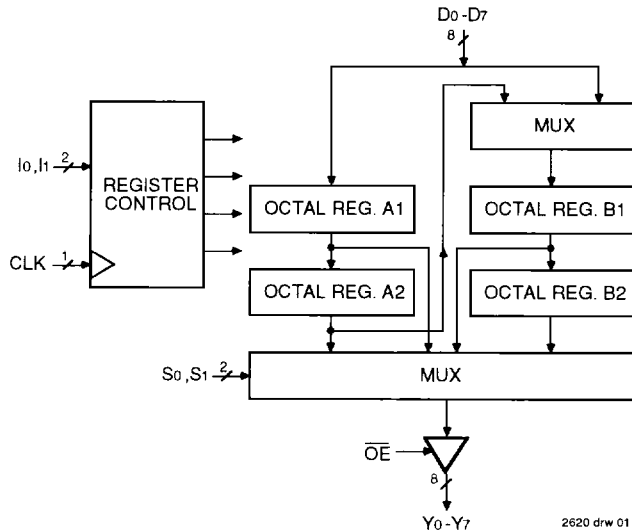
- Equivalent to AMD's Am29520 bipolar Multilevel Pipeline Register in pinout/function, speed and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar (5µA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CMOS processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520A/B/C contains four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

In the IDT29FCT520A/B/C when data is entered into the first level ($I = 2$ or $I = 1$), the existing data in the first level is moved to the second level. Transfer of data to the second level is achieved using the 4-level shift instruction ($I = 0$). This transfer also causes the first level to change.

FUNCTIONAL BLOCK DIAGRAMS

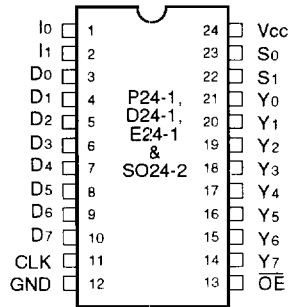


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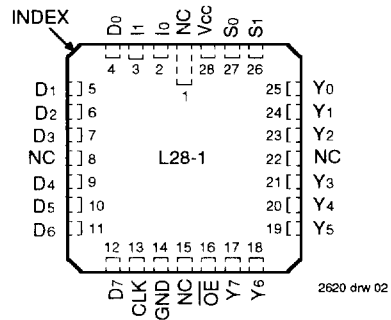
MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

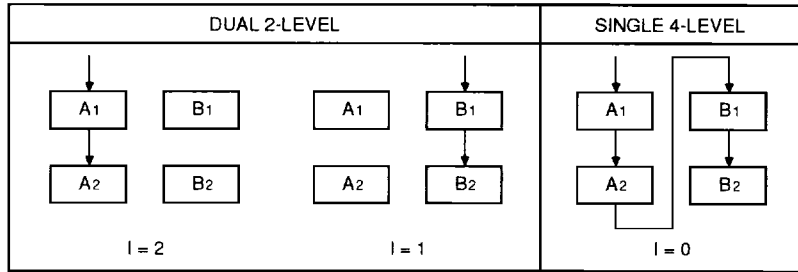
Pin Names	Description
D_n	Register input port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and Instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A1, A2, B1 or B2 data to be available at the output port.
\overline{OE}	Output enable for 3-state output port
Y_n	Register output port.

2620 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B2
0	1	B1
1	0	A2
1	1	A1

2620 tbl 02



NOTE:
1. I = 3 for hold.

2620 drw 03

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2620 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Inputs and Vcc terminals.
- Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COU	Output Capacitance	VOU = 0V	8	12	pF

NOTE:

2620 tbl 04

- This parameter is measured at characterization data but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$ $V_I = 2.7V$	—	—	5	μA	
I_{IL}	Input LOW Current		$V_I = 0.5V$	—	—		$-5^{(4)}$
			$V_I = GND$	—	—		-5
I_{OZH}	Off State (High Impedance) Output Current		$V_{CC} = \text{Max.}$ $V_O = V_{CC}$ $V_O = 2.7V$ $V_O = 0.5V$ $V_O = GND$	—	—		10
		—		—	$10^{(4)}$		
		—		—	$-10^{(4)}$		
		—		—	-10		
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_O = GND$	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
			$I_{OH} = -12mA$ MIL.	2.4	4.3		—
			$I_{OH} = -15mA$ COM'L.	2.4	4.3		—
V_{OL}	Output LOW Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA$ MIL.	—	0.3		0.5
			$I_{OL} = 48mA$ COM'L.	—	0.3		0.5

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2620 tbl 05



POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}	—	0.2	1.5	mA	
ΔI _{CC}	Quiescent Power Supply Current, TTL Input HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾	—	0.5	2.0	mA	
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max., Outputs Open OE = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25 mA/ MHz	
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND One Bit Toggling at f _i = 5MHz, 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4.0	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6.0	
		V _{CC} = Max., Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND Eight Bits Toggling at f _i = 5MHz, 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	7.0	12.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	9.2	21.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_{CC} = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_C P/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

2620 tbl 06

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT520A				IDT54/74FCT520B				IDT54/74FCT520C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPHL	Propagation Delay CLK to Y _n	CL = 50pF RL = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
tPLH	Propagation Delay S ₀ or S ₁ to Y _n		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
tsu	Set-up Time HIGH or LOW D _n to CLK		5.0	—	6.0	—	2.5	—	2.8	—	2.5	—	2.8	—	ns
tH	Hold Time HIGH or LOW D _n to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tsu	Set-up Time HIGH or LOW I ₀ or I ₁ to CLK		5.0	—	6.0	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW I ₀ or I ₁ to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tPHZ	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.0	ns
tPLZ	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	1.5	6.0	1.5	7.0	ns
tw	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	5.5	—	6.0	—	ns

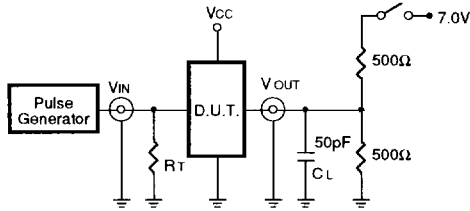
NOTES:

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.
3. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.

2620 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

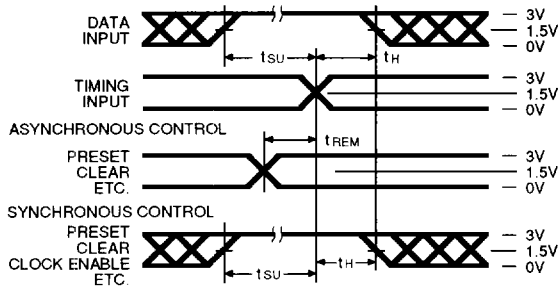
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

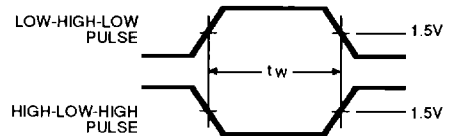
C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

2620 tbl 08

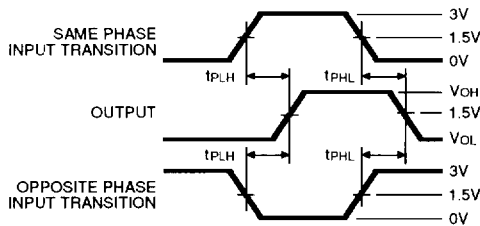
SET-UP, HOLD AND RELEASE TIMES



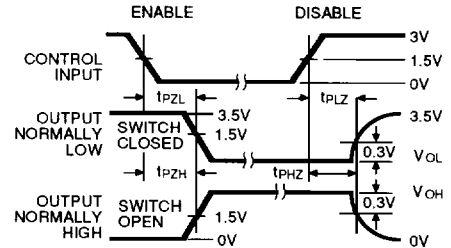
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

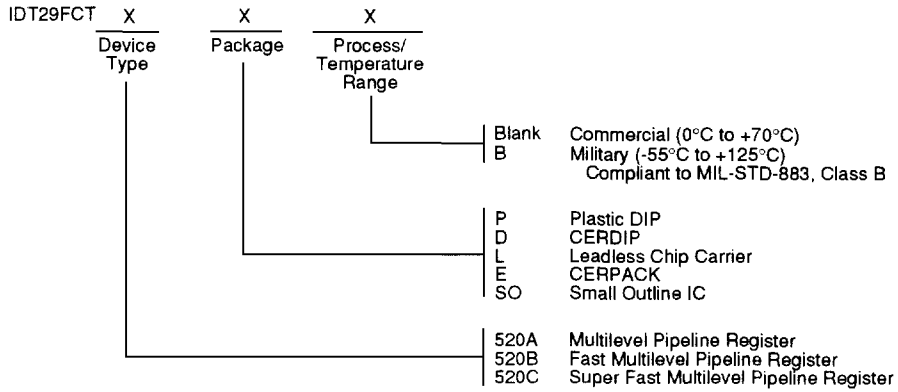


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate \leq 1.0 MHz; $Z_0 \leq$ 50Ω; $t_r \leq$ 2.5ns; $t_f \leq$ 2.5ns.

2620 drw 05

ORDERING INFORMATION



2620 dnr 04