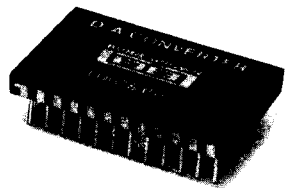
BURR-BROWN®



DAC63

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

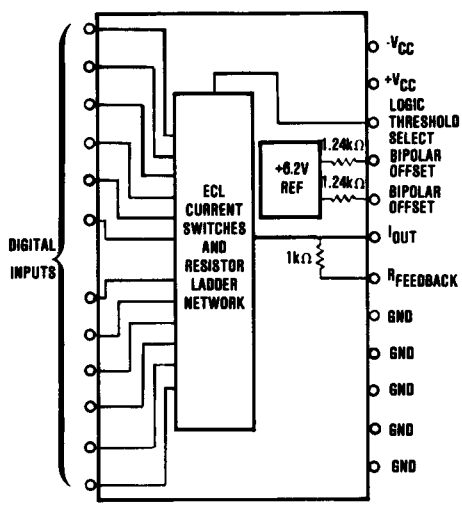
FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 30nsec SETTLING TIME (MAJOR CARRY)
- ECL-COMPATIBLE INPUTS
- LOW GLITCH ENERGY
- ±30ppm/°C MAX GAIN DRIFT
- LINEARITY ERROR LESS THAN ±1/2LSB OVER SPECIFIED TEMP RANGE
- ADJUSTABLE LOGIC THRESHOLD FOR IDEAL SWITCHING
- INTERNALLY-BYPASSED SUPPLY LINES TO MINIMIZE SETTLING TIME
- INTERNAL FEEDBACK RESISTOR FOR EXCELLENT THERMAL TRACKING
- INDUSTRIAL AND MILITARY GRADES
- HIGH RELIABILITY SCREENING AVAILABLE

DESCRIPTION

The DAC63 is an ultra-fast-settling 12-bit current output D/A converter in a 24-pin dual-in-line package. The inputs are ECL-compatible and the output settles in 30nsec, typ (40nsec, max for C and T grades) to within ±0.012% of Full Scale Range for an MSB change. The DAC63 utilizes a monolithic 12-bit switch chip and a stable thin-film-on-sapphire resistor network to achieve fast settling time and excellent stability over temperature and time. Because of the close thermal tracking of the current-switching transistors (all on one monolithic chip), the possibility of thermal-tail settling time problems are eliminated. An internal applications resistor for use with an external output op amp is included to convert the output current to insure excellent tracking and therefore lower drift. The linearity is guaranteed to be within ±1/2LSB over the specified temperature range of −25°C to +85°C for the CG, CM, BG, and BM grades and −55°C to +125°C for SM and TM grades. Gain drift is ±30ppm/°C max and bipolar offset drift is ±10ppm of FSR/°C max (high grades). Also included internally is a +6.2V reference. An output voltage compliance range of +2.0V to −0.5V allows the generation of an output voltage without using an external output amplifier. The device is available in both metal and ceramic bottom-brazed packages.

FUNCTIONAL DIAGRAM



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PDS-439B

SPECIFICATIONS

ELECTRICAL

At +25°C and rated supplies unless otherwise specified.

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			12			"	Bits
Logic Inputs[1]		ECL-compatible			"		
Logic "1": Voltage	−0.78	−0.90	−0.96	"	"	"	V
Current	6.0		33.0	"		"	μA
Logic "0": Voltage	−1.62	−1.75	−1.85	"	"	"	V
Current		10.0			"		nA
Logic Threshold: Voltage	−1.20	−1.33	−1.40	"	"	"	V
Current			0.25			"	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.012			"	% of FSR[3]
Differential Linearity Error			±0.012			"	% of FSR
Gain Error[2]		±0.02	±0.1		"	"	%
Offset Error[2]: Unipolar		±0.01	±0.04		"	"	% of FSR
Bipolar		±0.02	±0.1		"	"	% of FSR
Monotonicity Temp. Range (min)							
CG, CM, BG, BM	−25		+85	"		"	°C
TM, SM	−55		+125	"		"	°C
SETTLING TIME (into 150Ω)							
1LSB Change							
Settling to ±0.012% of FSR							
CM/TM, BM/SM		30	40		40	50	nsec
CG, BG		30	40		35	45	nsec
Full Scale Change							
Settling to ±1% of FSR		17			20		nsec
±0.1% of FSR		30			"		nsec
±0.024% of FSR							
CM/TM, BM/SM		55	65		65	75	nsec
CG, BG		35	50		40	55	nsec
±0.012% of FSR							
CM/TM, BM, SM		70			80		nsec
CG, BG		40			"		nsec
Glitch Energy[4]		250			"		LSB/nsec
DRIFT (over specified temp. range)							
Gain		±15	±30		±20	±40	ppm/°C
Offset: Unipolar		±0.3	±0.6		±0.5	±1	ppm/°C
Bipolar			±10			±15	ppm/°C
Linearity Error							
(over specified temp. range)			±0.012			±0.025	% of FSR
Differential Linearity Error							
(over specified temp. range)			±0.025			±0.05	% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current		0 to −10, ±5			"		mA
Output Voltage Ranges							
with External Op Amp		0 to +10, ±5			"		V
without External Op Amp[5]		0 to +15, ±0.5			"		V
Output Impedance without							
External Op Amp							
Unipolar: Positive		150			"		Ω
Negative		200			"		Ω
Bipolar		170			"		Ω
Compliance Voltage	−0.5		+2.0	"		"	V
POWER SUPPLIES AND REFERENCE							
Internal Reference Voltage		+6.2			"		V
Internal Reference Drift		±15			"		ppm/°C
Power Supply Voltages	±13	±15	±18	"	"	"	V
Power Supply Current: +15V		26	31		"	"	mA
−15V		38	46		"	"	mA
Power Supply Sensitivity: +15V		±0.0035			"		%/%ΔV
−15V		±0.0004			"		%/%ΔV
Power Dissipation		960	1160		"	"	mW

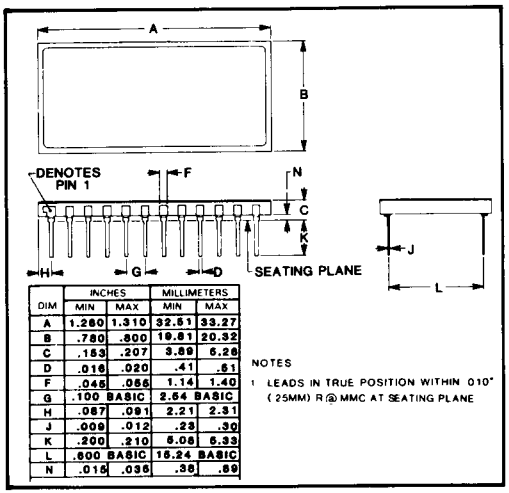
ELECTRICAL (CONT)

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification: CG, CM, BG, BM	−25		+85	*		*	°C
TM, SM	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C
PACKAGE							
CG, BG	24-pin DIP bottom-brazed ceramic						
CM, TM, BM, SM	24-pin DIP metal						

*Specification same as for DAC63CG/CM/TM.

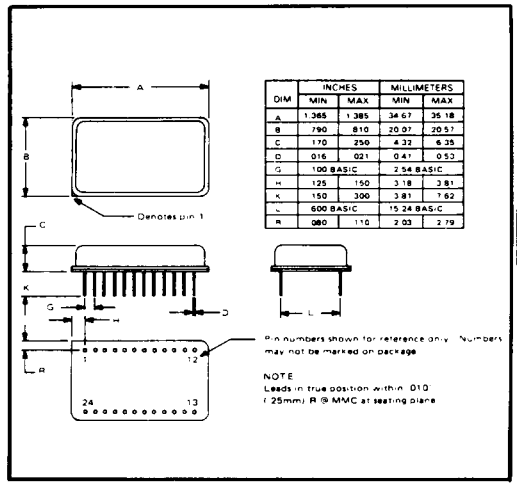
NOTES: (1) Logic input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column. (2) When used with an external output op amp or when the internal impedances/resistors are used as the load. (3) FSR is Full Scale Range, which is 10mA for both the DAC63BG and DAC63CG. (4) Refer to Output Glitch section. (5) Refer to Figures 8 and 9.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.260	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.087	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

NOTES
1. LEADS IN TRUE POSITION WITHIN .010" (.25MM) R @ MMC AT SEATING PLANE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin No.	Function
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12 (LSB)
13	GND
14	GND
15	GND
16	GND
17	GND
18	Feedback Resistor Connection
19	Current Output
20	Bipolar Offset
21	Bipolar Offset
22	Logic Threshold
23	+15VDC
24	-15VDC

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC63 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for the DAC63 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC63 is +2.0V and −0.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC63 (pins 13, 14, 15, 16, and 17). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC63. To achieve fast settling performance it is recommended that pins 13 through 17 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC63 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

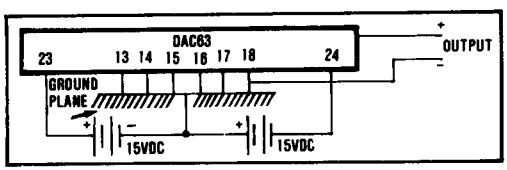


FIGURE 1. DAC63 Grounding.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC63 is compatible with conventional ECL logic families such as ECL 10,000. The circuit diagram shows that the equivalent circuit of each DAC63 digital input is the base of one side of a differential amplifier. The logic 1 input voltage is −0.85V with a typical input current of 8μA. The logic 0 input voltage is −1.75V with an input current of less than 8nA.

The Logic Threshold function of the DAC63 is very important in dealing with noise in the ECL input-driving circuitry. The ECL 10,000 logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of −1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision D/A converter is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the logic can couple through the D/A, resulting in an unacceptably noisy output.

Through the logic threshold input, the threshold voltage of the DAC63 is dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

If an MC10115 line receiver (or similar logic function) is used to drive the DAC63 input, the logic threshold pin can be driven by the V_{BB} output of the ECL gate. Refer to an ECL 10,000 data book for more detail. Figure 2 shows alternate methods for generating the drive signal for logic threshold, pin 22.

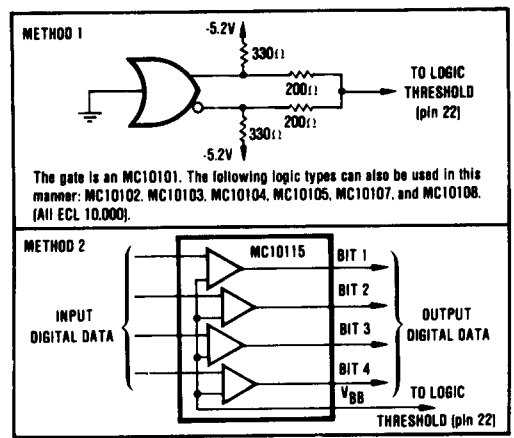


FIGURE 2. Driving the Logic Threshold Input.

SETTLING TIME

Settling time for the DAC63 is the total time required for the output to settle within an error band around its final value after a digital input change. This time includes the digital delay of the internal switches.

The settling time of the DAC63 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Application Note AN-115 which can be obtained from the factory.

Figure 3 shows a typical settling time curve of the DAC63 versus output error. This curve is for full-scale digital code changes. Figure 4 is a photograph showing typical output response characteristics of the DAC63.

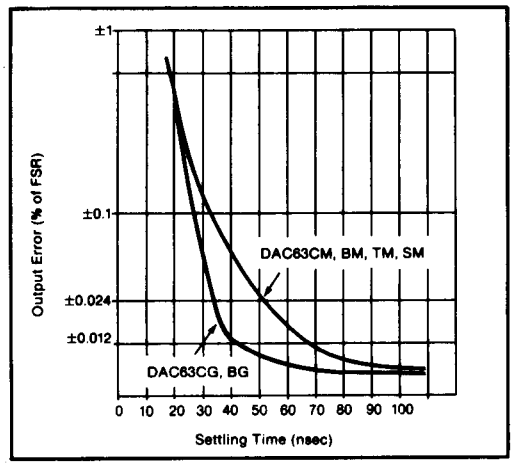


FIGURE 3. Output Error vs Settling Time (typical).

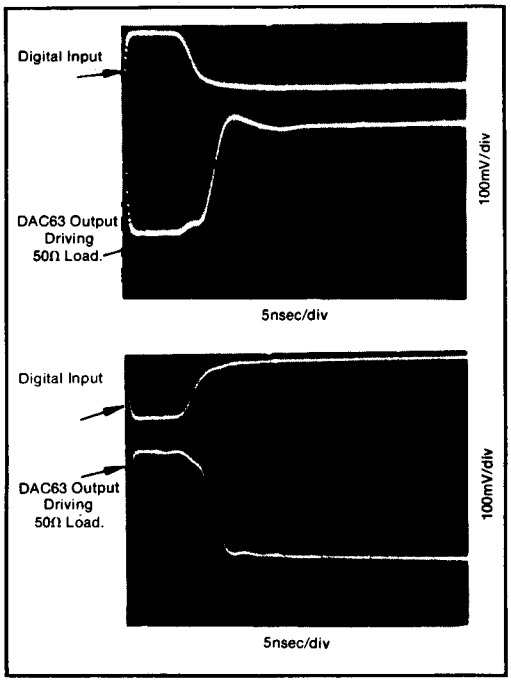


FIGURE 4. Full Scale Settling of DAC63 into 50Ω Load.

In order to achieve minimum settling time it is necessary to observe the following good high frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC63 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. Figure 6 shows how to interface the DAC63 to an input register. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC63 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC if there is data skew and if there is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSB-nsec is achievable with the DAC63 because it employs ECL circuitry with current switches that have virtually identical delay times for logic signals making either positive or negative transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates a noisy output which can be troublesome in some applications such as precision displays and complex waveform generation. Figure 5 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC63 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits (more than three lines may be adjusted if desired). Refer to Figure 6. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about −1.3V. Then

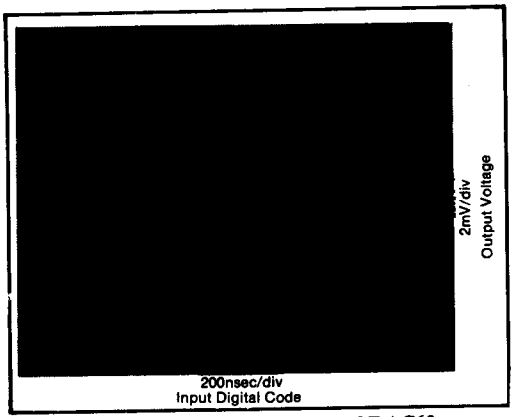


FIGURE 5. Typical Glitch Repsonse of DAC63 at Major Carry Transition with a 1.6V Full Scale Range.

examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 2 and then to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC63 contains two 1.24kΩ resistors for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC63 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 7 shows the DAC63 connected to an external op amp in unipolar and bipolar modes. With the Burr-Brown model OPA600 it is possible to achieve settling times to ±0.01% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC63 should be used without an external op amp. Figures 8 and 9 show how to connect the DAC63 for bipolar and positive unipolar

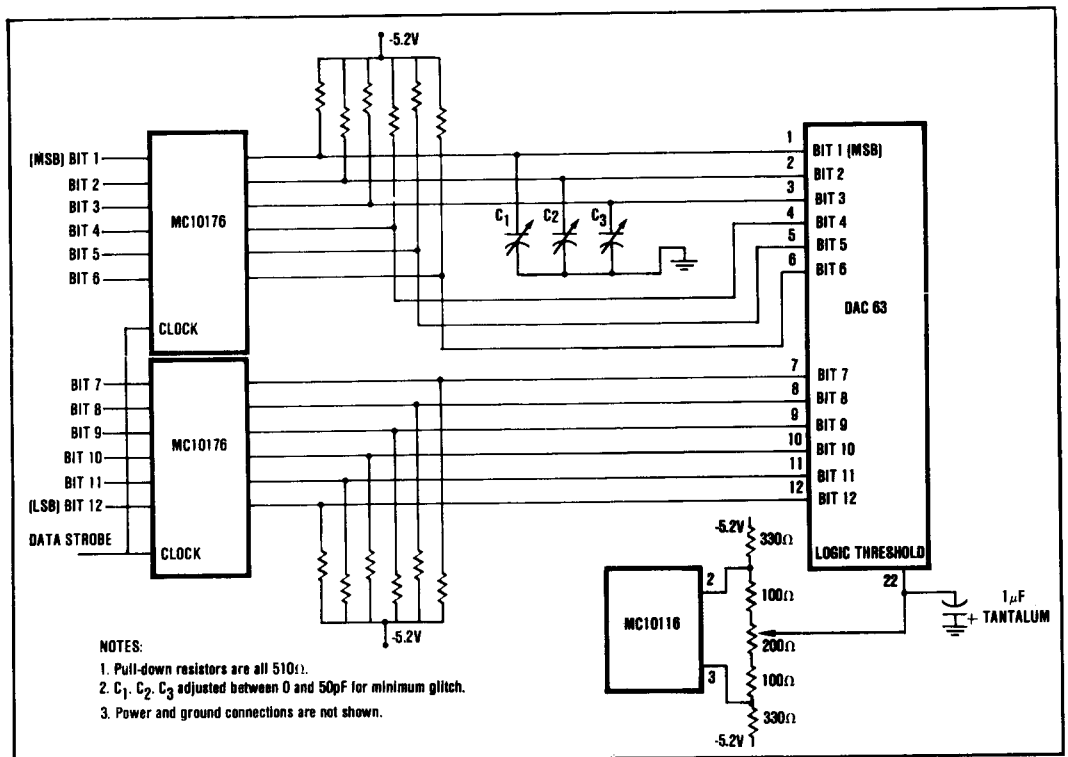
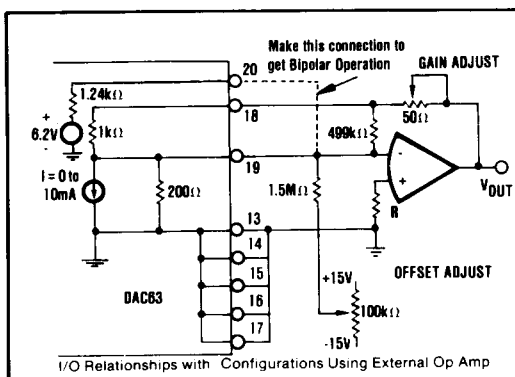


FIGURE 6. DAC63 Interface to Input Latches Including Glitch-Adjust Circuitry.

operation. Figure 10 illustrates how to connect the DAC63 to construct a fast A/D converter. The ADC attempts to create a null at the DAC output, so it is possible to clamp the output voltage with a pair of diodes, thereby avoiding the negative compliance limit.



		Unipolar	Bipolar
Digital Codes vs Output Voltage	111111111111	0.0000V	-5.0000V
	011111111111	5.0000V	0.0000V
	000000000000	9.9976V	4.9976V
R Value	R	169Ω	147Ω
Pin 20 Connection		Open	Connect to Pin 19

FIGURE 7. Bipolar and Unipolar Output Connections when Used with External Op Amp.

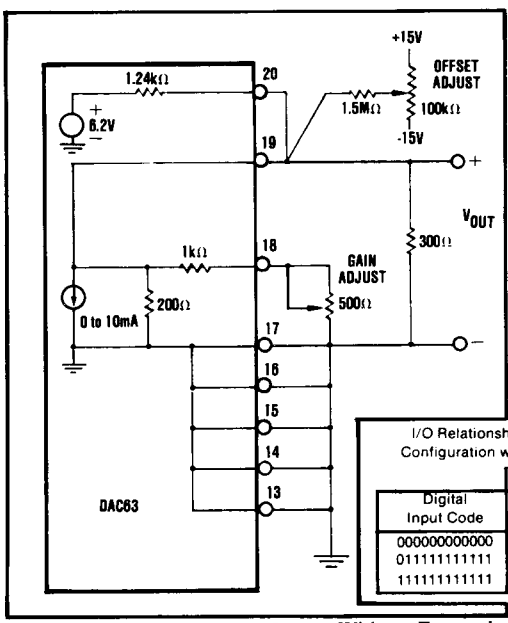


FIGURE 8. Bipolar Voltage Output Without External Op Amp.

I/O Relationships for Voltage Output Configuration without External Op Amp

Digital Input Code	Output Voltage: Positive Unipolar	Output Voltage: Bipolar
000000000000	0.0000V	-0.500V
011111111111	0.7500V	0.000V
111111111111	1.4996V	0.500V

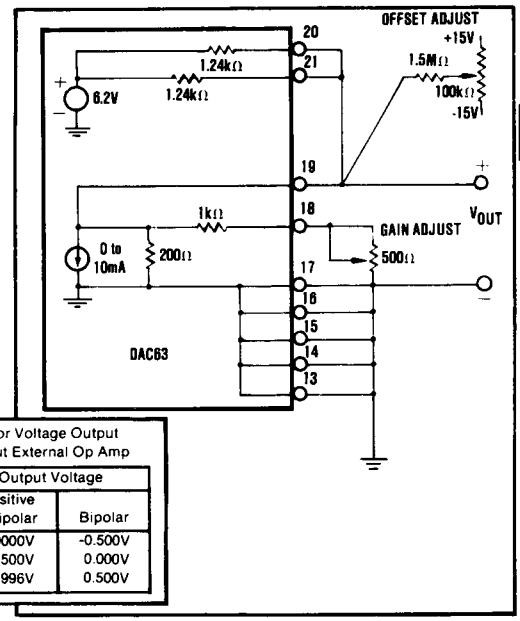


FIGURE 9. Positive Unipolar Voltage Output Without External Op Amp.

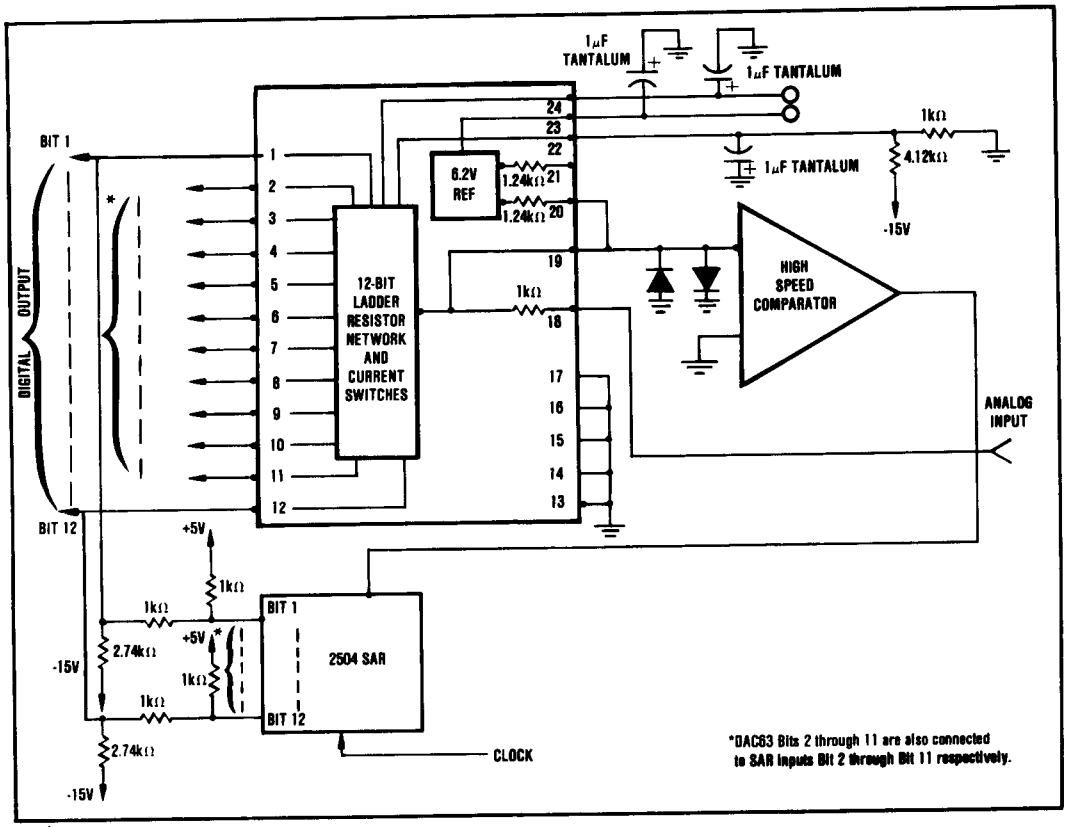


FIGURE 10. DAC63 Used in a Fast A/D Converter.