MOTOROLA

Quad 2-Input NAND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30002

Military 54LS03

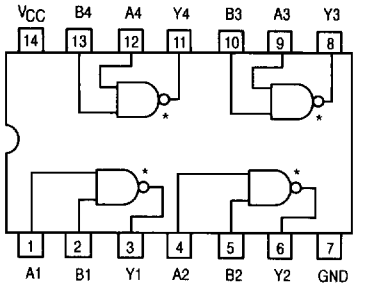
AVAILABLE AS:

1) JAN: JM38510/30002BXA
2) SMD: N/A
3) 883: 54LS03/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

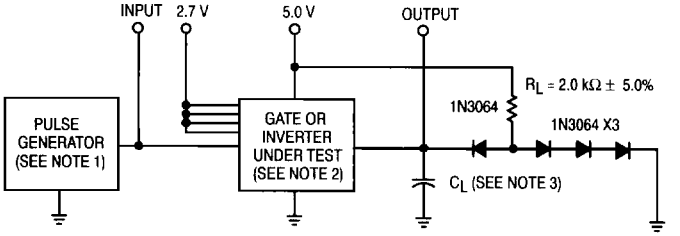
THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOGIC DIAGRAM

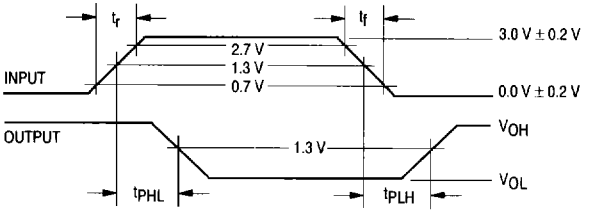


*OPEN COLLECTOR OUTPUT

AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, duty cycle = 50% and $Z_{OUT} = 50\ \Omega$.
2. Inputs not under test are at 2.7 V.
3. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
4. $R_L = 2.0\ k\Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	V_{CC}
B1	2	2	3	GND
Y1	3	3	4	V_{CC}
A2	4	4	6	V_{CC}
B2	5	5	8	GND
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y3	8	8	12	V_{CC}
A3	9	9	13	V_{CC}
B3	10	10	14	GND
Y4	11	11	16	V_{CC}
A4	12	12	18	V_{CC}
B4	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

5

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V on both inputs.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other input is open.
I_{CEX}	Open Collector Input Current		100		100		100	µA	V_{CC} = 4.5 V, V_{IL} = 0.7 V, V_{IN} = 5.5 V on other input, V_{OUT} = 5.5 V.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other input = 0 V.
I_{IH2}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other input = 0 V.
I_{IL}	Logical "0" Input Current	− 150	− 380	− 150	− 380	− 150	− 380	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
I_{CCH}	Power Supply Current		1.6		1.6		1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		4.4		4.4		4.4	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay /Data-Output Output High-Low	2.0 —	36 28	2.0 —	55 50	2.0 —	55 50	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PLH} t_{PLH}	Propagation Delay /Data-Output Output Low-High	2.0 —	40 32	2.0 —	60 55	2.0 —	60 55	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.

5