EL7583C

3-Channel DC:DC Converter

PRELIMINARY

Features

- TFT/LCD display supply
  - Boost regulator
  - V_{ON} charge pump
  - V_{OFF} charge pump
- 2V to 14V V_{IN} supply
- 5V < V_{BOOST} < 18V
- 5V < V_{ON} < 40V
- -40V < V_{OFF} < 0V
- V_{BOOST} = 5V @700mA
- V_{BOOST} = 12V @450mA
- V_{BOOST} = 15V @400mA
- High frequency, small inductor DC:DC boost circuit
- Up to 90% efficient DC:DC boost converter capability
- Adjustable frequency
- Adjustable soft-start
- Adjustable outputs
- Small parts count

Applications

- TFT-LCD panels
- PDAs

Ordering Information

Part No	Package	Tape & Reel	Outline #
EL7583CR	20-Pin TSSOP		MDP0044

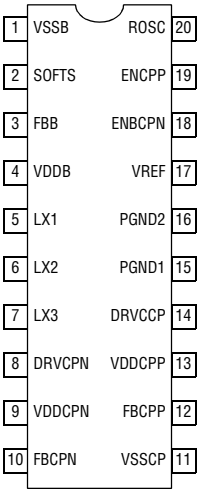
General Description

The EL7583C is a 3-channel DC:DC converter IC which is designed primarily for use in TFT/LCD applications. It features a 2.0V to 14V input capability and provides 5V to 18V output from a micropower boost converter. This output is designed to power the column drivers and can provide up to 400mA @15V, or 700mA @5V output. A pair of charge pump control circuits provide regulated outputs of V_{ON} and V_{OFF} supplies at 8V to 40V and -5V to -40V, respectively (depending on the V_{BOOST} set and external component configuration), each at up to 15mA.

The EL7583C features adjustable switching frequency, adjustable soft start, and each supply channel has a separate output enable control to allow selection of supply start-up sequence. An over-temperature feature is provided to allow the IC to be automatically protected from excessive power dissipation.

The EL7583C is available in a 20-pin TSSOP package and is specified for operation over the full -40°C to +85°C temperature range.

Connection Diagram



EL7583CR
(20-Pin TSSOP Top View)

EL7583C

3-Channel DC:DC Converter

PRELIMINARY

Absolute Maximum Ratings (T_A = 25°C)

Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied

V_{IN} Input Voltage	15V
SW Voltage	18V
Maximum Continuous Output Current	1A
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Lead Temperature	300°C
Power Dissipation	See Curves
ESD Voltage	2kV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Characteristics

V_{IN} = 3.3V, V_{BOOST} = 12V, I_{OUT} = 225mA, F_{OSC} = 1MHz, T_A = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Unit
DC:DC Boost Converter						
IQ1	Quiescent Current - Shut-down	V(ENB) = 0V			10	µA
IQ2	Quiescent Current - Switching	V(ENB) = VDDB, frequency = 600kHz		5	8	mA
V(FBB)	Feedback Voltage		1.204	1.229	1.254	V
V_{REF}	Reference Voltage		1.218	1.260	1.302	V
I(FBB)	Feedback Input Bias Current	Current magnitude			0.1	µA
V_{IN}	Input Supply Range		2		14	V
D_{MAX}	Maximum Duty Cycle		85	90		%
$I(LX)_{MAX}$	Current Limit - Max Average Input Current	V_{BOOST} = 12V, $I(V_{BOOST})$ = 350mA, V_{IN} = 3.3V		1.5		A
R_{DS-ON}	Switch On Resistance	at V_{BOOST} = 12V, I(LX1+LX2+LX3+LX4) = 350mA		0.22		Ω
$I_{LEAK-SWITCH}$	Switch Leakage Current				1	µA
V_{BOOST}	Output Range	$V_{BOOST} > V_{IN} + V_{DIODE}$	5		15	
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	2.7V < V_{IN} < 13.2V, V_{BOOST} = 15V			0.1	%
$\Delta V_{BOOST}/\Delta I_{O1}$	Load Regulation	50mA < I_{O1} < 250mA		0.5		%
$F_{OSC-RANGE}$	Frequency Range	R_{OSC} range = 240kΩ to 60kΩ	200		1000	kHz
F_{OSC1}	Switching Frequency	R_{OSC} = 100kΩ	480	600	720	kHz
F_{OSC2}	Switching Frequency	R_{OSC} = 220kΩ	240	300	360	kHz
Positive Regulated Charge Pump (V_{ON})						
		Most positive V_{ON} output depends on the magnitude of the VDDCPP input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)				
VDDCPP	Supply Input for Positive Charge Pump	Usually connected to V_{BOOST}	5		15	V
V(FBCPP)	Feedback Reference Voltage		1.32	1.42	1.52	V
I(FBCPP)	Feedback Input Bias Current	Current magnitude			0.1	µA
$I(DRCPP)_{MAX}$	Maximum RMS DRCPP Output Current	VDDCPP = 15V			80	mA
		VDDCPP = 6V			15	mA
F_{PUMP}	Charge Pump Frequency	Frequency set by R_{OSC} - see boost section		0.5*F_{OSC}		Hz
Negative Regulated Charge Pump (V_{OFF})						
		Most negative V_{OFF} output depends on the magnitude of the VDDCPN input voltage (normally connected to V_{BOOST}) and the external component configuration (doubler or tripler)				
VDDCPN	Supply Input for Negative Charge Pump	Usually connected to V_{BOOST}	5		15	V

Electrical Characteristics

V_{IN} = 3.3V, V_{BOOST} = 12V, I_{OUT} = 225mA, F_{OSC} = 1MHz, T_A = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Unit
V(FBCPN)	Feedback Reference Voltage		-100	-50	0	mV
I(FBCPN)	Feedback Input Bias Current	Magnitude of input bias			0.1	µA
$I(DRCPNf)_{MAX}$	Maximum Continuous RMS DRCPN Output Current	VDDCPN = 15V			80	mA
		VDDCPN = 6V			15	mA
F_{PUMP}	Charge Pump Frequency	Frequency set by ROSC - see boost section		$0.5*F_{OSC}$		Hz
Enable Control Logic						
$VHI\text{-}EN_X$	Enable Input High Threshold	x = "BCPN", CPP"	1.6			V
$VLO\text{-}EN_X$	Enable Input Low Threshold	x = "BCPN", CPP"			0.8	V
$I(EN_X)$	Enable Input Bias Current	x = "BCPN", CPP"; current magnitude			0.1	µA

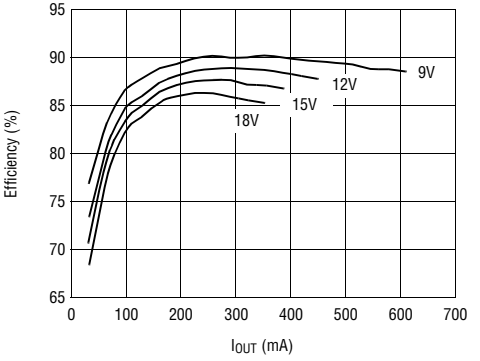
Pin Descriptions

I = Input, O = Output, S = Supply

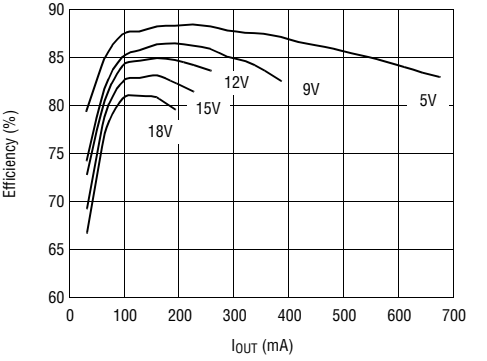
EL7583CR 20-Pin TSSOP	Pin Name	Pin Type	Pin Function
1	VSSB	S	Ground for DC:DC boost and reference circuits; chip substrate
2	SOFTS	I	Soft-start input; the capacitor connected to this pin sets the current limited start time
3	FBB	I	Voltage feedback input for boost circuit; determines boost output voltage, V_{BOOST}
4	VDDB	S	Positive supply input for DC:DC boost circuits
5	LX1	O	Boost regulator inductor drive pin 1
6	LX2	O	Boost regulator inductor drive pin 2
7	LX3	O	Boost regulator inductor drive pin 3
8	DRVCPN	O	Driver output for the external generation of negative charge pump voltage, V_{OFF}
9	VDDCPN	S	Positive supply for input for V_{OFF} generator
10	FBCPN	I	Voltage feedback input to determine negative charge pump output, V_{OFF}
11	VSSCP	S	Negative supply pin for both the positive and negative charge pumps
12	FBCPP	I	Voltage feedback to determine positive charge pump output, V_{ON}
13	VDDCPP	S	Positive supply input for V_{ON} generator
14	DRVCPP	O	Voltage driver output for the external generation of positive charge pump, V_{ON}
15	PGND1	O	Power ground for LX switching FET
16	PGND2	O	Power ground for LX switching FET
17	VREF	I	Voltage reference for V_{COM} and charge pump circuits; decouple to ground
18	ENBCPN	I	Enable pin for the DC:DC boost function (V_{BOOST} generation) and negative charge pump function (V_{OFF} generation)
19	ENCPP	I	Enable for DRVCPP (V_{ON} generation); active high
20	ROSC	I	Connected to an external resistor to ground; sets the switching frequency of the DC:DC boost

Typical Performance Curves

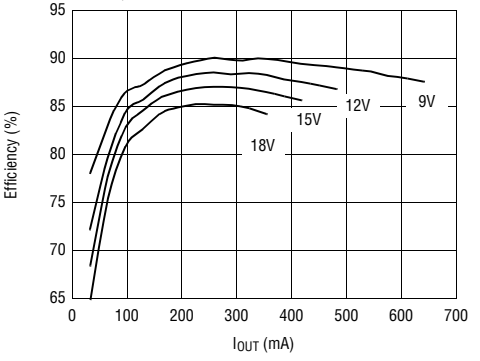
Efficiency vs I_{OUT}
f=675kHz, V_{IN}=5.0V



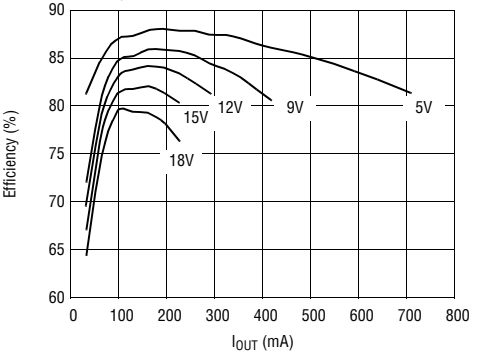
Efficiency vs I_{OUT}
f=675kHz, V_{IN}=3.3V



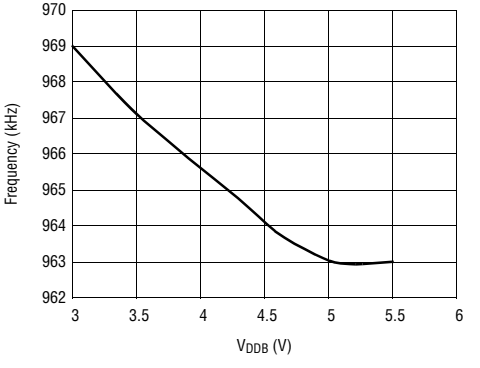
Efficiency vs I_{OUT}
f=1MHz, V_{IN}=5.0V



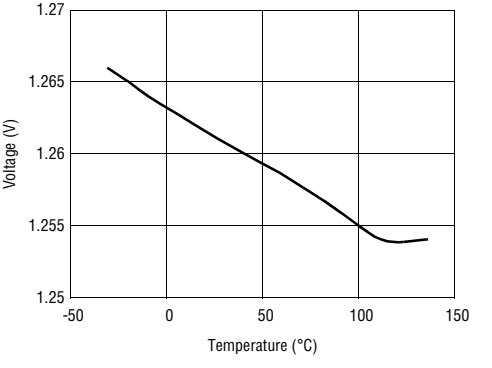
Efficiency vs I_{OUT}
f=1MHz, V_{IN}=3.3V



Frequency vs V_{CC}

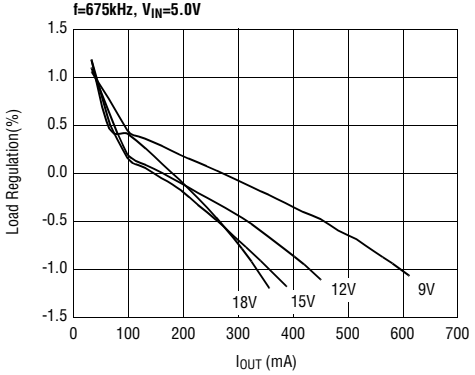


V_{REF} vs Temperature

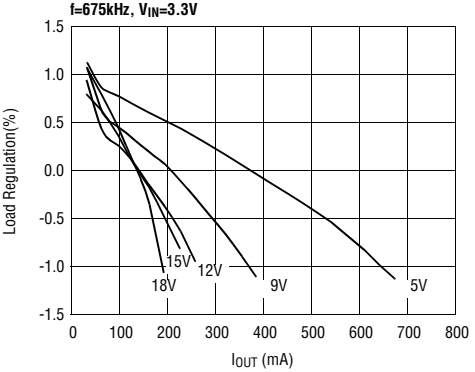


Typical Performance Curves

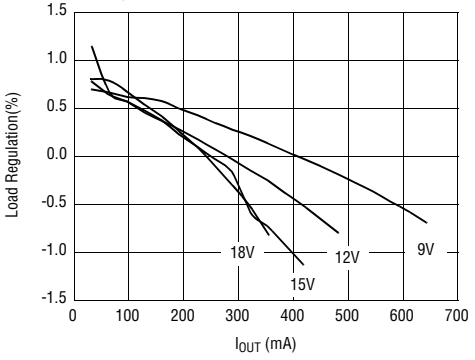
Load Regulation vs I_{OUT}
f=675kHz, V_{IN}=5.0V



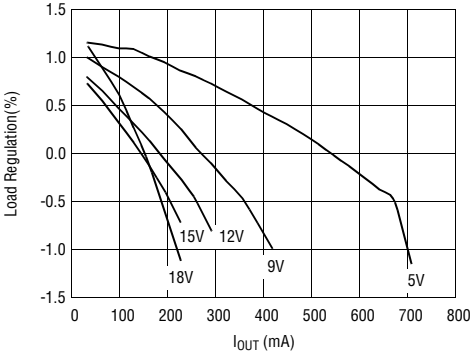
Load Regulation vs I_{OUT}
f=675kHz, V_{IN}=3.3V



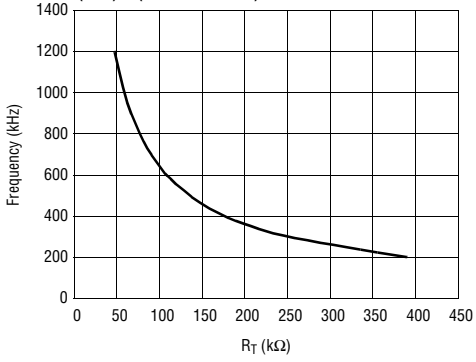
Load Regulation vs I_{OUT}
f=1MHz, V_{IN}=5.0V



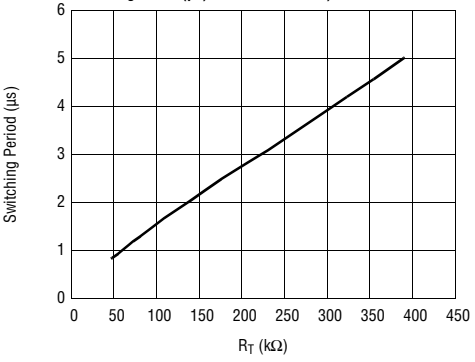
Load Regulation vs I_{OUT}
f=1MHz, V_{IN}=3.3V



Frequency vs R_T
f(MHz)=1/(0.0118 R_T+0.378)

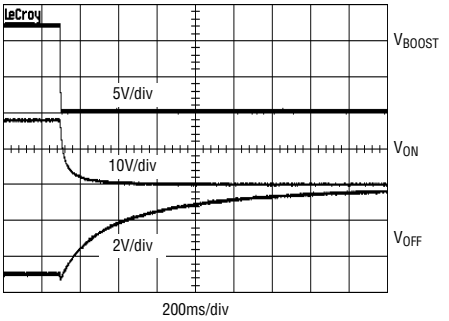


Switching Period vs R_T
Switching Period(µs)=0.0118 R_T+0.378)

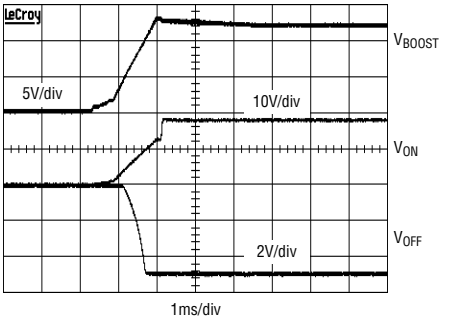


Typical Performance Curves

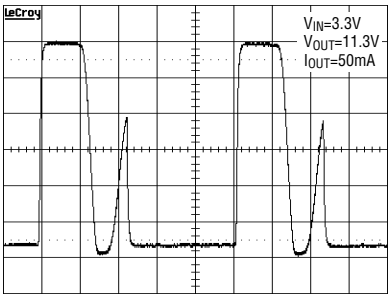
Power-Down
100k & 0.1µF Delay Network on ENCPP, C_{SS}=0.1µF



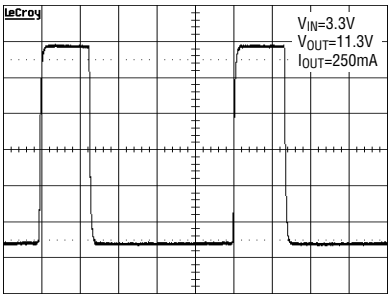
Power-Up
100k & 0.1µF Delay Network on ENCPP, C_{SS}=0.1µF



LX Waveform - Discontinuous Mode



LX Waveform - Continuous Mode



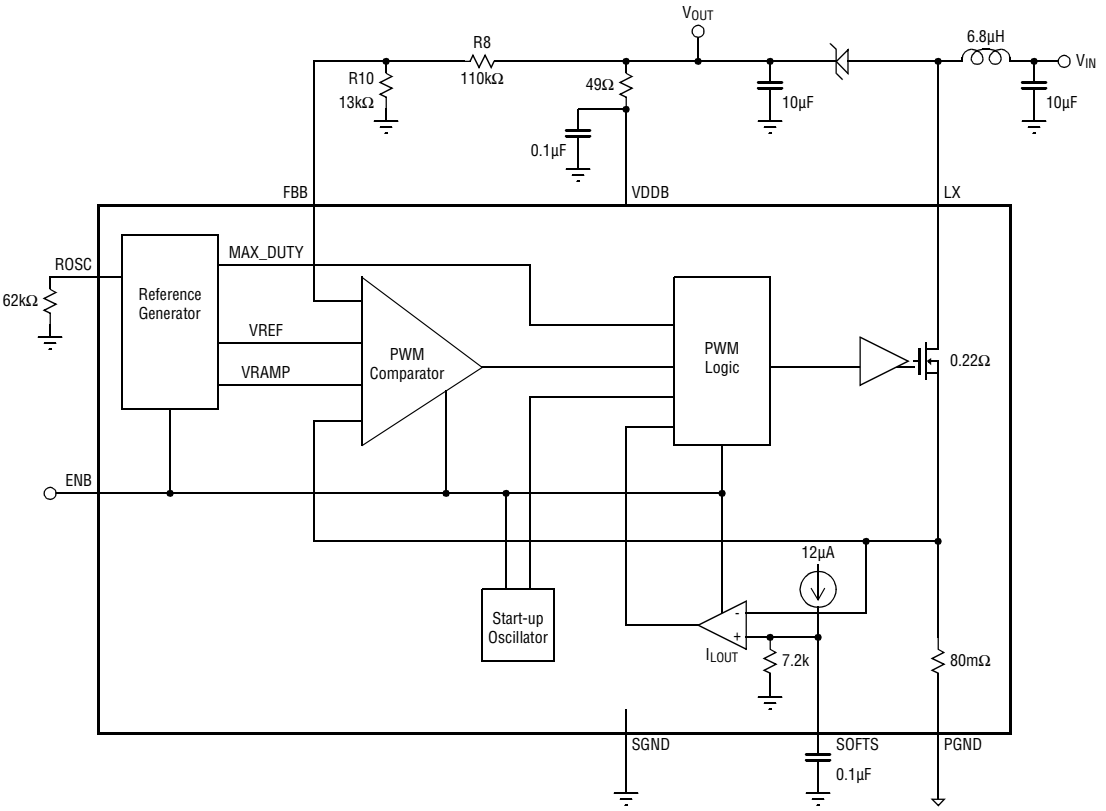
Applications Information

The EL7583C is high efficiency multiple output power solution designed specifically for thin-film transistor (TFT) liquid crystal display (LCD) applications. The device contains one high current boost converter and two low power charge pumps (V_{ON} and V_{OFF}).

The boost converter contains an integrated N-channel MOSFET to minimize the number of external components. The converter output voltage can be set from 5V to 18V with external resistors. The V_{ON} and V_{OFF} charge pumps are independently regulated to positive and negative voltages using external resistors. Output voltages as high as 40V can be achieved with additional capacitors and diodes.

Boost Converter

The boost converter operates in constant frequency pulse-width-modulation (PWM) mode. Quiescent current for the EL7583C is only 5mA when enabled, and since only the low side MOSFET is used, switch drive current is minimized. 90% efficiency is achieved in most common application operating conditions.



A functional block diagram with typical circuit configuration is shown on the previous page. Regulation is performed by the PWM comparator which regulates the output voltage by comparing a divided output voltage with an internal reference voltage. The PWM comparator outputs its result to the PWM logic. The PWM logic switches the MOSFET on and off through the gate drive circuit. Its switching frequency is external adjustable with a resistor from timing control pin (R_T) to ground. The boost converter has 200kHz to 1.2MHz operating frequency range.

Start-Up

After V_{DD} reaches a threshold of about than 2V, the power MOSFET is controlled by the start-up oscillator, which generates fixed duty-ratio of 0.5-0.7 at a frequency of several hundred kilohertz. This will boost the output voltage, providing the initial output current load is not too great (< 250mA).

When V_{DD} reaches about 3.7V, the PWM comparator takes over the control. The duty ratio will be decided by the multiple-input direct summing comparator, Max_Duty signal (about 90% duty-ratio), and the Current Limit Comparator, whichever is the smallest.

The soft-start is provided by the current limit comparator. As the internal 12µA current source changes the external soft-start capacitor, the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of output voltage.

The regulator goes through the start-up sequence as well after the ENB signal is pulled to HI.

Steady-State Operation

When the output reaches the preset voltage, the regulator operates at steady state. Depending on the input/output condition and component, the inductor operates at either continuous-conduction mode or discontinuous-conduction mode.

In the continuous-conduction mode, the inductor current is a triangular waveform and LX voltage a pulse waveform. In the discontinuous-conduction mode, the inductor current is complete dry out before the MOSFET is turned on again. The input voltage source, the inductor, and the MOSFET and output diode parasitic capacitors forms a resonant circuit. Oscillation will occur in this period. This oscillation is normal and will not affect the regulation.

At very low load, the MOSFET will skip pulse sometimes. This is normal.

Current Limit

The MOSFET current limit is nominal 1.5A. This restricts the maximum output current I_{OMAX} based on the following formula:

$$I_{OMAX} = 1 - \frac{\Delta I_L}{2} \times \frac{V_{IN}}{V_O}$$

where:

ΔI_L is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{F_S}$$

D is the MOSFET turn-on radio and is decided by:

$$D = \frac{V_O - V_{IN}}{V_O}$$

F_S is the switching frequency.

The following table gives typical values:

Maximum Continuous Output Current

V_{IN} (V)	V_O (V)	L (µH)	F_S (MHz)	I_{OMAX} (mA)
3	5	6.8	1	700
3.3	9	6.8	1	400
3.3	12	10	1	275
5	9	6.8	1	600
5	12	6.8	1	450
5	15	10	1	400

Component Considerations

Input Capacitor

It is recommended that C_{IN} is larger than 10µF. Theoretically, the input capacitor has ripple current of ΔI_L. Due to high-frequency noise in the circuit, the input current ripple may exceed the theoretical value. Larger capacitor will reduce the ripple further.

Boost Inductor

The inductor has peak and average current decided by:

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_O}{1 - D}$$

The inductor should be chosen to be able to handle this current. Furthermore, due to the fixed internal compensation, It is recommended that maximum inductance of 10µH and 15µH to be used in the 5V and 12V or higher output voltage, respectively.

The output diode has average current of I_O, and peak current the same as the inductor's peak current. Schottky diode is recommended and it should be able to handle those currents.

Output voltage ripple is the product of peak inductor current times the ESR of output capacitor. Low ESR capacitor is to be used to reduce the output ripple. The minimum out capacitance of 330µF, 47µF, and 33µF is recommended for 5V, 12V, and 16V for 600kHz switching frequency, respectively. For 1MHz switching frequency, 220µF, 33µF, and 22µF capacitor can be used for the output voltages. In addition to the voltage rating, the output capacitor should also be able to handle the rms current is given by:

$$I_{CORMS} = \sqrt{(1 - D) \times \left(D + \frac{\Delta I_L^{\,2}}{I_{LAVG}^{\,2}} \times \frac{1}{12} \right)} \times I_{LAVG}$$

Feedback Resistor Network

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 200kΩ is recommended. The boost converter output voltage is determined by the following relationship:

$$V_{OUT} = \frac{R_8 + R_{10}}{R_{10}} \times V_{FBB}$$

Schottky Diode

Speed, forward voltage drop, and reverse current are the three most critical specifications for selecting the Schottky diode. The entire output current flows through the diode, so the diode average current is the same as the average load current and the peak current is the same as the inductor peak current. When selecting the diode, one must consider the forward voltage drop at the peak diode current. On the elantec demo board, MBRM120 is selected. Its forward voltage drop is 450mV at 1A forward current.

Output Capacitor

The EL7583C is specially compensated to be stable with capacitors which have a value of 10µF at the particular V_{OUT} being set. Also, output ripple voltage requirements also determine the minimum value and the type of capacitors. Output ripple voltage consists of two components - the voltage drop caused by the switching current though the ESR of the output capacitor and the charging and discharging of the output capacitor:

$$V_{RIPPLE} = I_{PEAK} \times ESR + \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times \frac{I_{OUT}}{C_{OUT} \times FREQ}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging/discharging of the output capacitor.

EL7583C

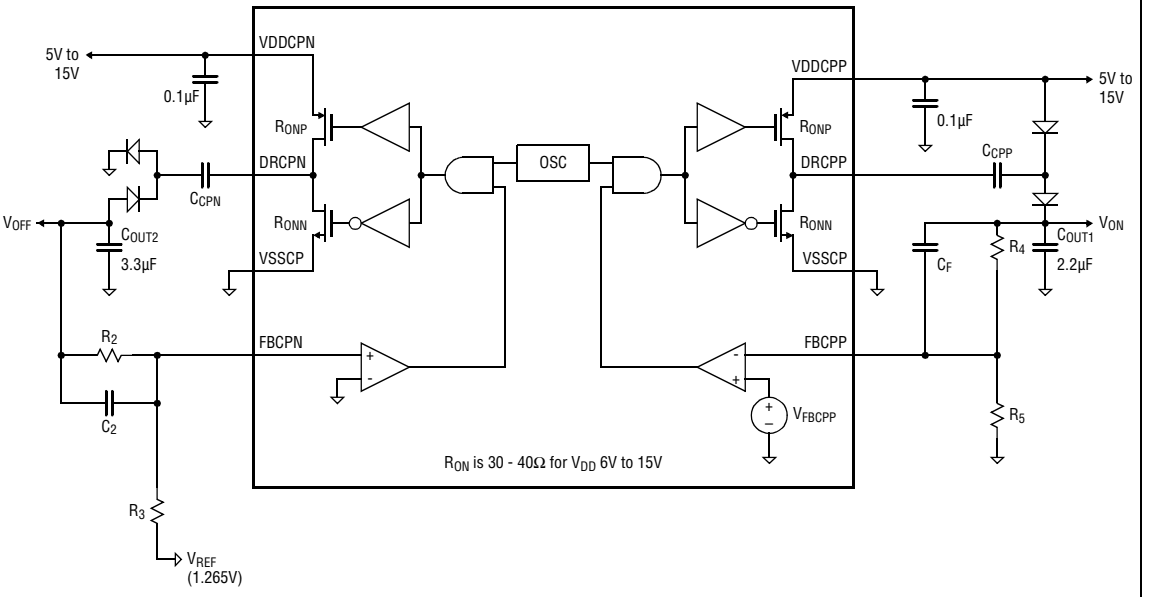
3-Channel DC:DC Converter

PRELIMINARY

Positive and Negative Charge Pump (V_{ON} and V_{OFF})

The EL7583C contains two independent charge pumps, see charge pump block and connection diagram. The negative charge pump inverts the VDDCPN supply voltage and provides a regulated negative output voltage. The positive charge pump doubles the VDDCPP supply voltage and provides a regulated positive output voltage. The regulation of both the negative and positive charge pumps is generated by the internal comparator that senses the output voltage and compares it with and internal reference. The switching frequency of the charge pump is set to ½ the boost converter switching frequency.

The pumps use pulse width modulation to adjust the pump period, depending on the load present. The pumps are short circuit-protected and can supply 15mA to 80mA for V_{DD} 6V to 15V.



Positive Charge Pump Design Considerations

A single stage charge pump is shown above. The maximum V_{ON} output voltage is determined by the following equation:

$$V_{ON}(max) \le 2 \times VDDCPP - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) -$$

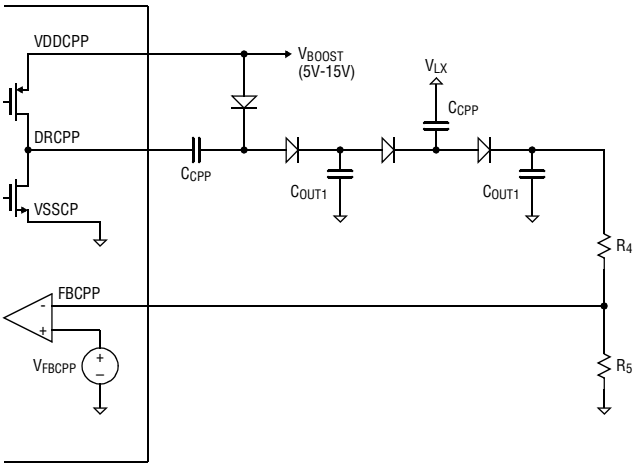
$$2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT1}}$$

where:

R_{ONN} and R_{ONP} resistance values depend on the VDDCPP voltage levels. For 15V supply, R_{ON} is typically 30V. For 6V supply, R_{ON} is typically 40Ω

If additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The drive impedance at the LX switching is typically 150mΩ. The figure on the next page illustrates an implementation for two-stage positive charge pump circuit.

Two-Stage Positive Charge Pump Circuit



The maximum V_{ON} output voltage for N+1 stage charge pump is:

$$V_{ON}(max) \le 2 \times VDDCPP - I_{OUT} \times 2 \times (R_{ONN} + R_{ONP}) - 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{CPP}} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT1}} + N \times V_{LX}(max) - N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{CPP}} + I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT1}}\right)$$

R_4 and R_{12} set the V_{ON} output voltage:

$$V_{ON} = V_{FBCPP} \times \frac{R_4 + R_5}{R_5}$$

Negative Charge Pump Design Considerations

The criteria for the negative charge pump is similar to the positive charge pump. For a single stage charge pump, the maximum V_{OFF} output voltage is:

$$V_{OFF}(max) \ge I_{OUT} \times 2 \times (R_{ONN} + R_{ONNP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_{SQ} \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT2}} - VDDCPN$$

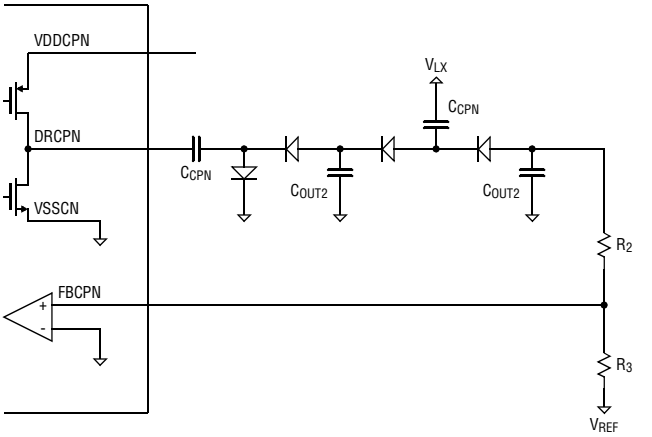
Similar to positive charge pump, if additional stage is required, the LX switching signal is recommended to drive the additional charge pump diodes. The figure on the next page shows a two stage negative charge pump circuit.

EL7583C

3-Channel DC:DC Converter

PRELIMINARY

Two-Stage Negative Charge Pump Circuit



The maximum V_{OFF} output voltage for N+1 stage charge pump is:

$$V_{OFF}(max) \geq I_{OUT} \times 2 \times (R_{ONN} + R_{ONNP}) + 2 \times V_{DIODE} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{CPN}} - I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT2}} - VDDCPN - N \times V_{LX}(max) + N \times \left(2 \times V_{DIODE} + I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{CPN}} + I_{OUT} \times \frac{1}{0.5 \times F_{SW} \times C_{OUT2}}\right)$$

R_2 and R_3 determine V_{OFF} output voltage:

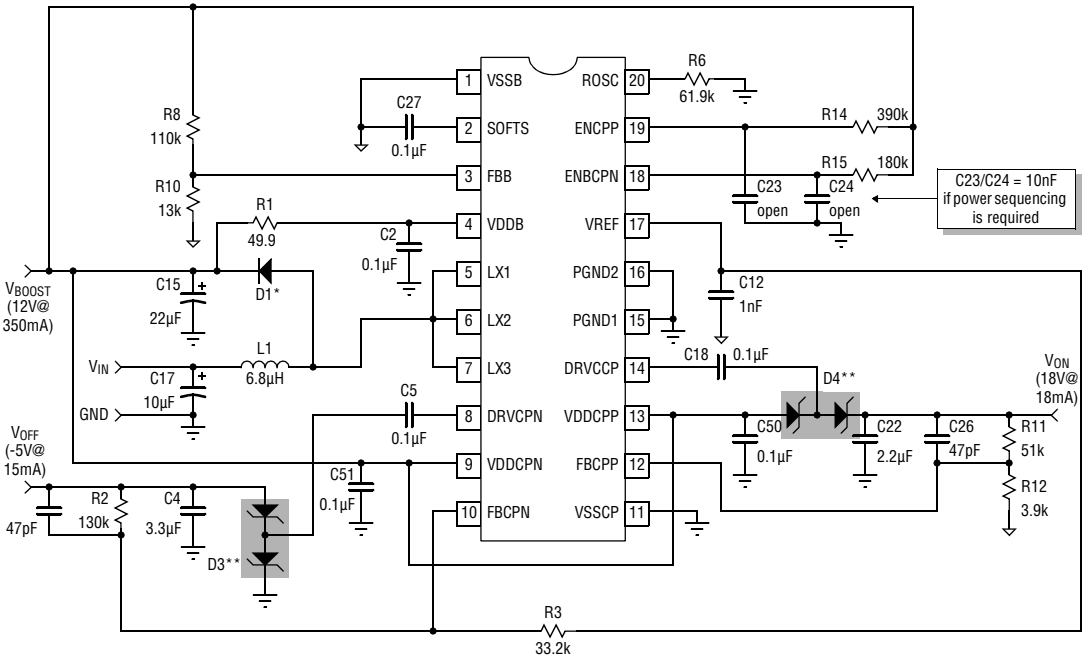
$$V_{OFF} = -(V_{REF} - V_{FBCPN}) \times \frac{R_2}{R_3}$$

PCB Layout Guidelines

Careful layout is critical in the successful operation of the application. The following layout guidelines are recommended to achieve optimum performance.

1. V_{REF} and VDDB bypass capacitors should be placed next to the pins.
2. Place the boost converter diode and inductor close to the LX pins.
3. Place the boost converter output capacitor close to the PGND pins.
4. Locate feedback dividers close to their respected feedback pins to avoid switching noise coupling into the high impedance node.
5. Place the charge pump feedback resistor network after the diode and output capacitor node to avoid switching noise; a demo board is available to illustrate the proper layout implementation.

Typical Application Circuit



* MBRM120LT3
** BAT54S

EL7583C

3-Channel DC:DC Converter

PRELIMINARY

Effective May 15, 2002, Elantec, a leader in high performance analog products, is now a part of Intersil Corporation.

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