FEATURES:

- **128K x 36, 256K x 18 memory configurations**
- **Supports high system speed:**
  - *– 200MHz 3.1ns clock access time*
  - *– 183MHz 3.3ns clock access time*
  - *– 166MHz 3.5ns clock access time*
  - *– 150MHz 3.8ns clock access time*
  - *– 133MHz 4.2ns clock access time*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **2.5V or 3.3V I/O option**
- **Packaged in a JEDEC Standard 100-lead plastic thin quad flatpack (TQFP) and 119-lead ball grid array (BGA)**

DESCRIPTION:

The IDT71Vx576/578 are high-speed SRAMs organized as 128K x 36/ 256K x 18. The IDT71Vx576/578 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71Vx576/578 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71Vx576/578 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-lead thin plastic quad flatpack (TQFP) as well as a 119-lead ball grid array (BGA).

PIN DESCRIPTION SUMMARY

A_0-A_{17}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

4876 tbl 01

NOTE:

1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71Vx578.

APRIL 1999

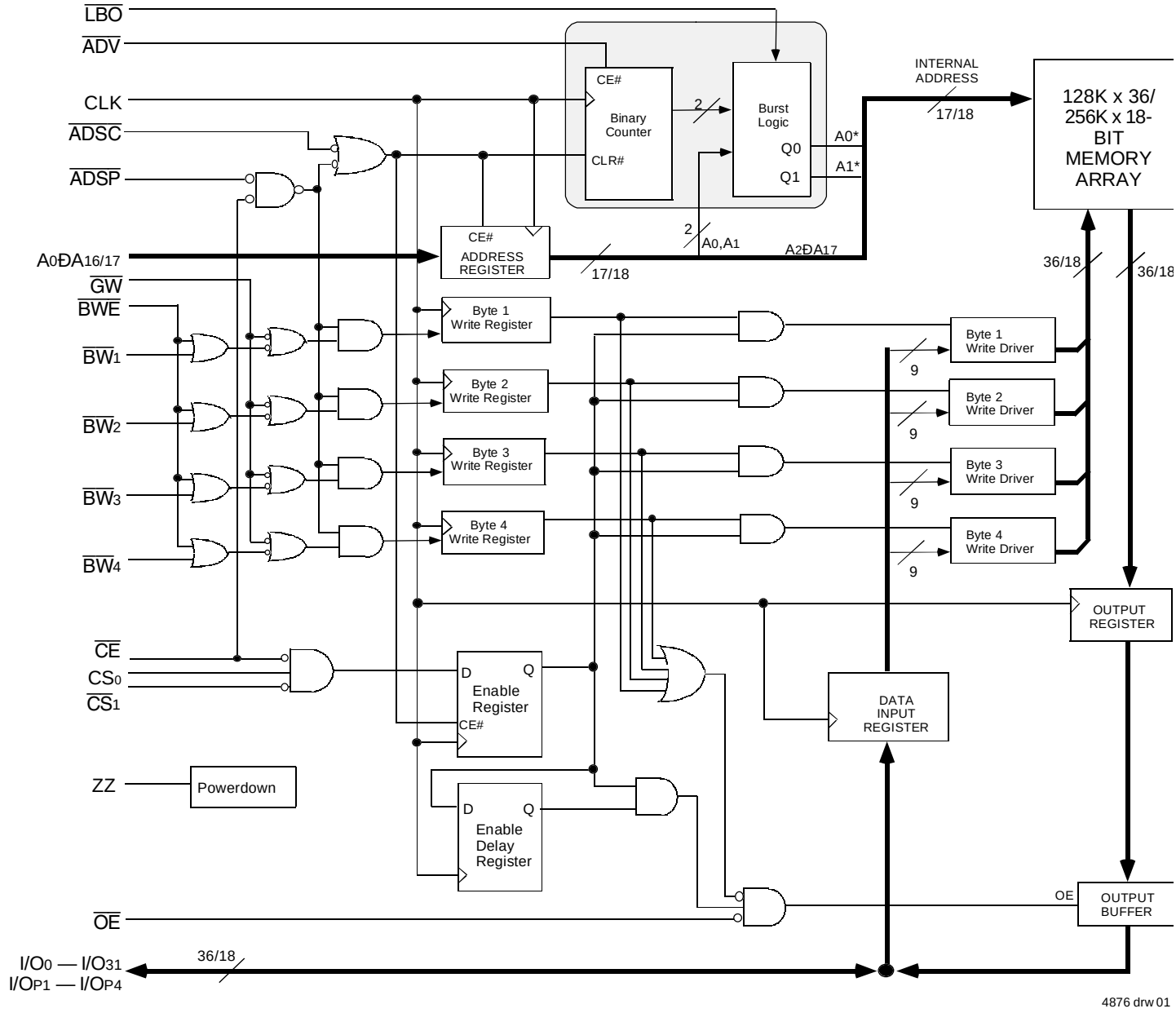
PIN DEFINITIONS(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{17}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O_{0-7}, I/O_{P1}, $\overline{BW_2}$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71Vx576/578. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the interleaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V or 2.5V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71Vx576/78 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

4876 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A	Operating Temperature	-0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

4876 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

4876 tbl 07

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	2.5V±5%
Commercial	0°C to +70°C	0V	3.3V±5%	V_{DD}

4876 tbl 04

RECOMMENDED DC OPERATING CONDITIONS WITH VDDQ AT 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	1.7	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	1.7	—	V_{DDQ} +0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.7	V

4876 tbl 05

NOTES:
1. V_{IH} (max) = VDDQ + 1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

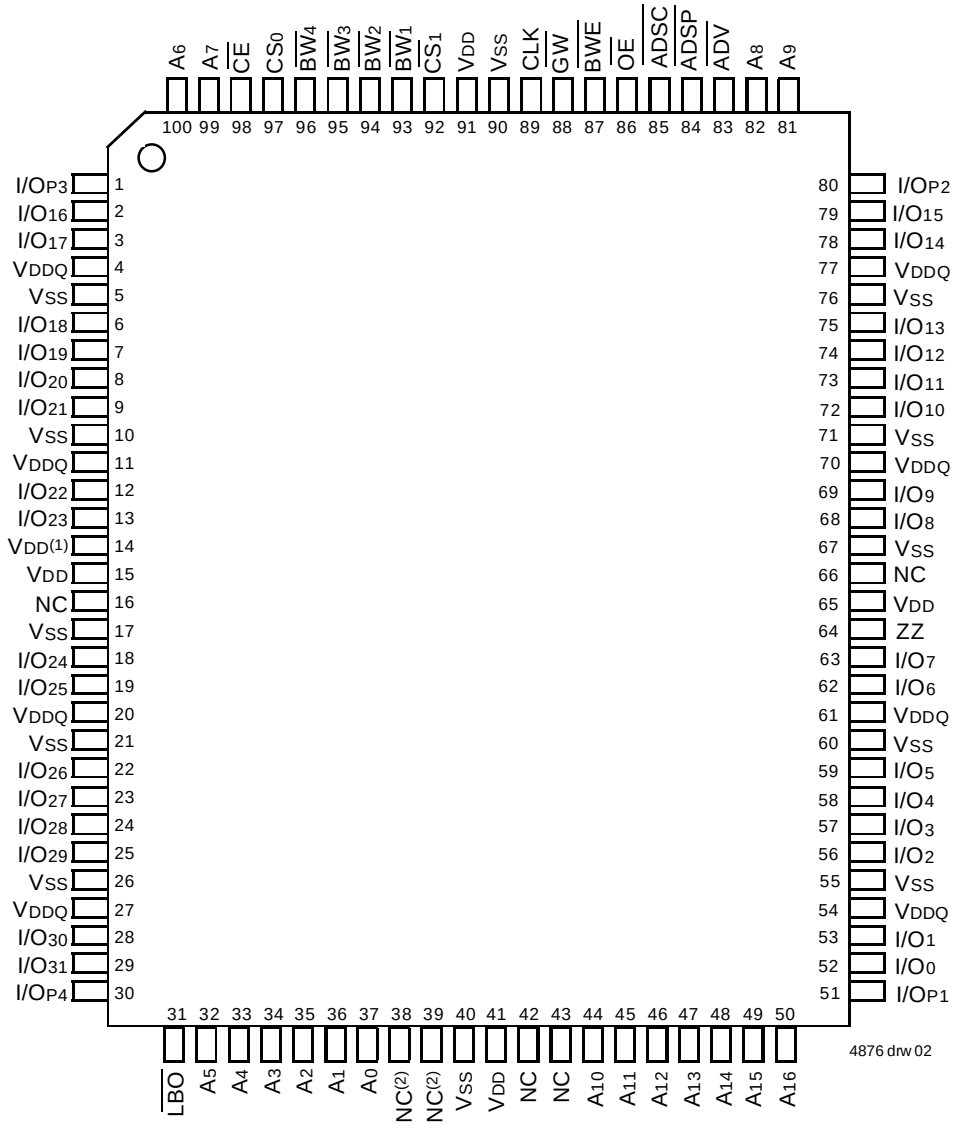
RECOMMENDED DC OPERATING CONDITIONS WITH VDDQ AT 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} +0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.8	V

4876 tbl 06

NOTES:
1. V_{IH} (max) = VDDQ + 1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

PIN CONFIGURATION – 128K x 36 TQFP

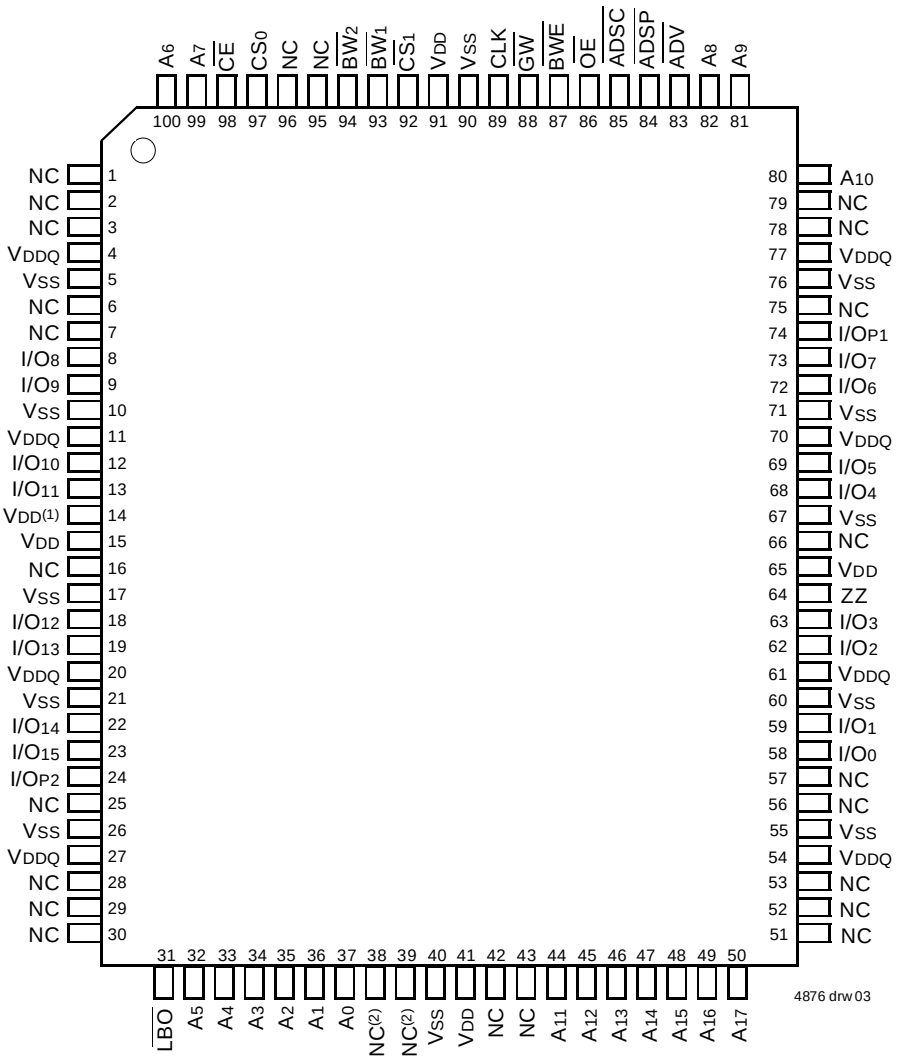


TOP VIEW

NOTES:

1. Pins 14 does not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pins 38 and 39 can be either NC or connected to V_{SS}.

PIN CONFIGURATION – 256K x 18 TQFP



TOP VIEW

NOTES:
1. Pins 14 does not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pins 38 and 39 can be either NC or connected to V_{SS}.

PIN CONFIGURATION – 128K x 36 BGA[1,2]

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{DDQ}
B	NC	$\overline{CS_0}$	A3	$\overline{ADSC}$	A9	$\overline{CS_1}$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O_{16}	I/O_{P3}	V_{SS}	NC	V_{SS}	I/O_{P2}	I/O_{15}
E	I/O_{17}	I/O_{18}	V_{SS}	$\overline{CE}$	V_{SS}	I/O_{13}	I/O_{14}
F	V_{DDQ}	I/O_{19}	V_{SS}	$\overline{OE}$	V_{SS}	I/O_{12}	V_{DDQ}
G	I/O_{20}	I/O_{21}	$\overline{BW_3}$	$\overline{ADV}$	$\overline{BW_2}$	I/O_{11}	I/O_{10}
H	I/O_{22}	I/O_{23}	V_{SS}	$\overline{GW}$	V_{SS}	I/O_9	I/O_8
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	I/O_{24}	I/O_{26}	V_{SS}	CLK	V_{SS}	I/O_6	I/O_7
L	I/O_{25}	I/O_{27}	$\overline{BW_4}$	NC	$\overline{BW_1}$	I/O_4	I/O_5
M	V_{DDQ}	I/O_{28}	V_{SS}	$\overline{BWE}$	V_{SS}	I/O_3	V_{DDQ}
N	I/O_{29}	I/O_{30}	V_{SS}	A_1	V_{SS}	I/O_2	I/O_1
P	I/O_{31}	I/O_{P4}	V_{SS}	A_0	V_{SS}	I/O_0	I/O_{P1}
R	NC	A_5	$\overline{LBO}$	V_{DD}	V_{DD}	A_{13}	NC
T	NC	NC	A_{10}	A_{11}	A_{14}	NC	$\overline{ZZ}$
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

4876 drw 04

TOP VIEW

PIN CONFIGURATION – 256K x 18 BGA[1,2]

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_4	$\overline{ADSP}$	A_8	A_{16}	V_{DDQ}
B	NC	CS0	A_3	$\overline{ADSC}$	A_9	$\overline{CS_1}$	NC
C	NC	A_7	A_2	V_{DD}	A_{13}	A_{17}	NC
D	I/O_8	NC	V_{SS}	NC	V_{SS}	I/O_7	NC
E	NC	I/O_9	V_{SS}	$\overline{CE}$	V_{SS}	NC	I/O_6
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	I/O_5	V_{DDQ}
G	NC	I/O_{10}	$\overline{BW_2}$	$\overline{ADV}$	V_{SS}	NC	I/O_4
H	I/O_{11}	NC	V_{SS}	$\overline{GW}$	V_{SS}	I/O_3	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	I/O_{12}	V_{SS}	CLK	V_{SS}	NC	I/O_2
L	I/O_{13}	NC	V_{SS}	NC	$\overline{BW_1}$	I/O_1	NC
M	V_{DDQ}	I/O_{14}	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	I/O_{15}	NC	V_{SS}	A_1	V_{SS}	I/O_0	NC
P	NC	I/O_{P2}	V_{SS}	A_0	V_{SS}	NC	I/O_{P1}
R	NC	A_5	$\overline{LBO}$	V_{DD}	V_{DD}	A_{12}	NC
T	NC	A_{10}	A_{15}	NC	A_{14}	A_{11}	$\overline{ZZ}$
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

4876 drw 05

TOP VIEW

NOTES:
1. R5 does not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. L4 and U4 can be either NC or connected to V_{SS}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LZZ}\|$	ZZ and $\overline{LBO}$ Input Leakage Current(1)	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}(3.3V)	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}(3.3V)	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V
V_{OL}(2.5V)	Output Low Voltage	I_{OL} = +6mA, V_{DD} = Min.	—	0.4	V
V_{OH}(2.5V)	Output High Voltage	I_{OH} = -6mA, V_{DD} = Min.	2.0	—	V

NOTE: 4876 tbl 08

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

Symbol	Parameter	Test Conditions	200MHz	183MHz	166MHz	150MHz	133MHz	Unit
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	360	340	320	295	250	mA
20	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2,3)	20	20	20	20	20	mA
130	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}(2,3)	130	120	110	100	90	mA
20	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	20	20	20	20	20	mA

NOTES: 4876 tbl 09

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC TEST CONDITIONS

(V_{DDQ} = 3.3V/2.5V)

Input Pulse Levels	0 to 3V / 0 to V_{DDQ}
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V / (V_{DDQ}/2)
Output Timing Reference Levels	1.5V / (V_{DDQ}/2)
AC Test Load	See Figure 1

4876 tbl 10

AC TEST LOADS

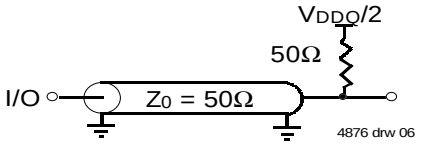


Figure 1. AC Test Load

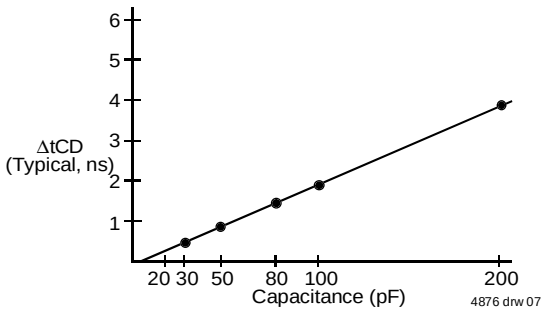


Figure 2. Lumped Capacitive Load, Typical Derating

SYNCHRONOUS TRUTH TABLE(1,3)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}x$	$\overline{OE}$ (2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	-	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	-	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	-	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	-	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	-	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	-	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	-	DIN

NOTES:

4876 tbl 11

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ = low for this table.

SYNCHRONOUS WRITE FUNCTION TRUTH TABLE(1, 2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1(3)	H	L	L	H	H	H
Write Byte 2(3)	H	L	H	L	H	H
Write Byte 3(3)	H	L	H	H	L	H
Write Byte 4(3)	H	L	H	H	H	L

NOTES: 4876 tbl 12

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71Vx579.
3. Multiple bytes may be selected during the same cycle.

ASYNCHRONOUS TRUTH TABLE(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

NOTES: 4876 tbl 13

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

INTERLEAVED BURST SEQUENCE TABLE ($\overline{LBO}$=VDD)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

NOTE: 4876 tbl 14

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

LINEAR BURST SEQUENCE TABLE ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

NOTE: 4876 tbl 15

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ±5%, T_A = 0 to 70°C)

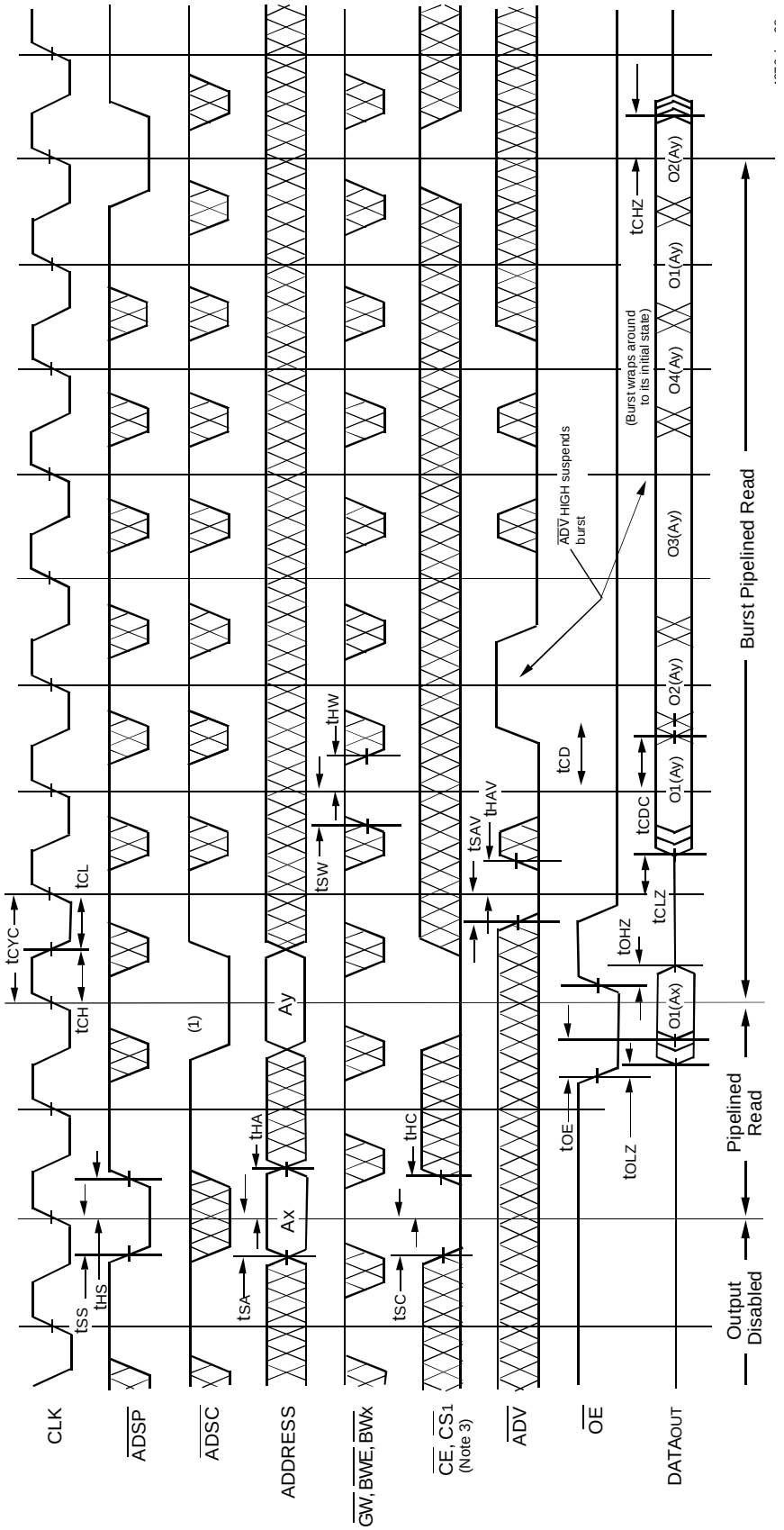
Symbol	Parameter	200MHz		183MHz		166MHz		150MHz		133MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5	—	5.5	—	6	—	6.7	—	7.5	—	ns
t_{CH}(1)	Clock High Pulse Width	2	—	2.2	—	2.4	—	2.6	—	3	—	ns
t_{CL}(1)	Clock Low Pulse Width	2	—	2.2	—	2.4	—	2.6	—	3	—	ns
Output Parameters												
t_{CD}	Clock High to Valid Data	—	3.1	—	3.3	—	3.5	—	3.8	—	4.2	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CLZ}(2)	Clock High to Output Active	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}(2)	Clock High to Data High-Z	1.5	3.1	1.5	3.3	1.5	3.5	1.5	3.8	1.5	4.2	ns
t_{OE}	Output Enable Access Time	—	3.1	—	3.3	—	3.5	—	3.8	—	4.2	ns
t_{OLZ}(2)	Output Enable Low to Output Active	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Enable High to Output High-Z	—	3.1	—	3.3	—	3.5	—	3.8	—	4.2	ns
Set Up Times												
t_{SA}	Address Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SD}	Data In Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SW}	Write Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SAV}	Address Advance Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.2	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Hold Times												
t_{HA}	Address Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.4	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
Sleep												
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	100	—	100	—	ns
t_{ZZR}(3)	ZZ Recovery Time	100	—	100	—	100	—	100	—	100	—	ns
t_{CFG}(4)	Configuration Set-up Time	20	—	22	—	24	—	27	—	30	—	ns

NOTES:

4876tbl 16

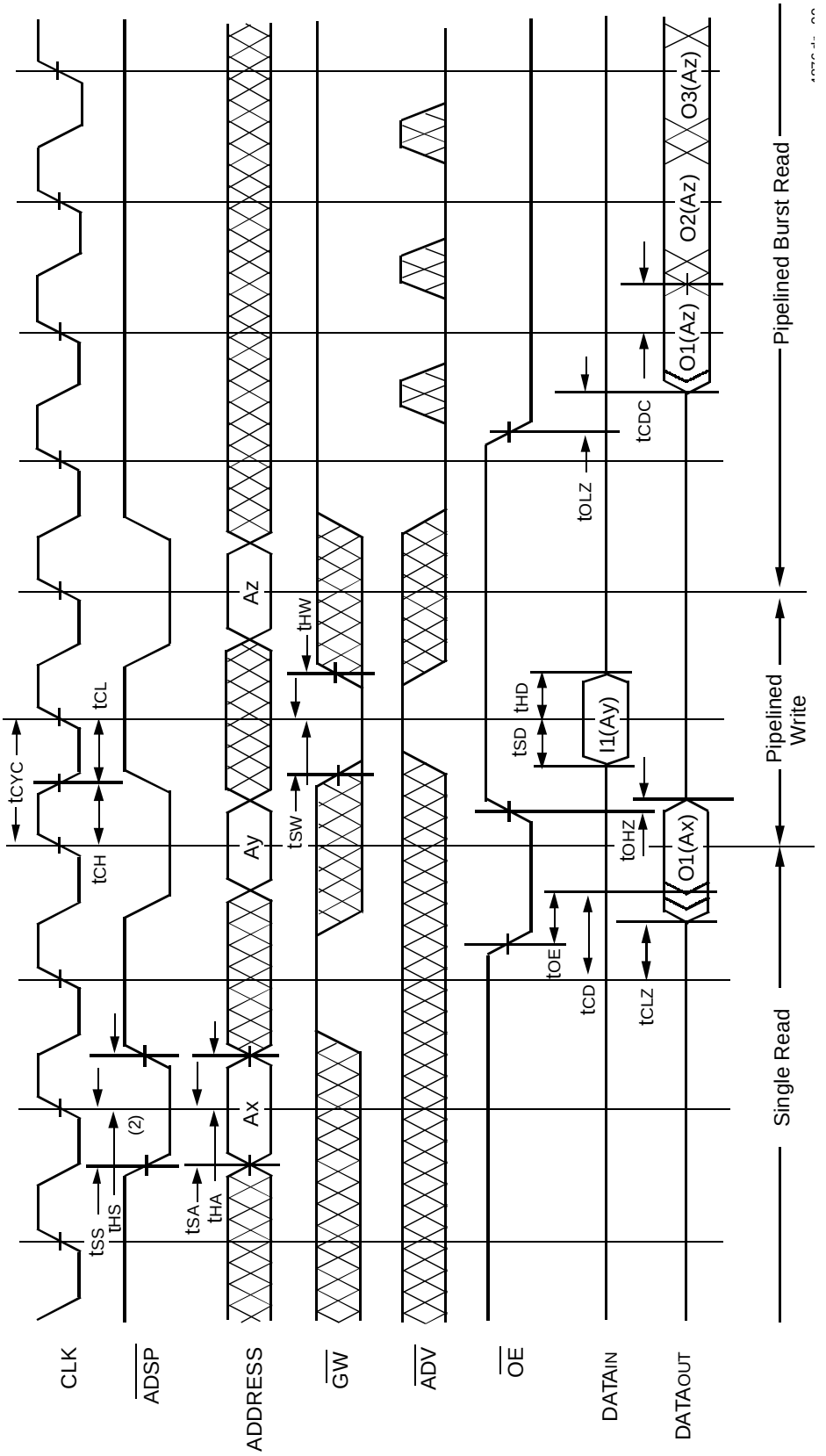
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.

TIMING WAVEFORM OF PIPELINED READ CYCLE(1,2)



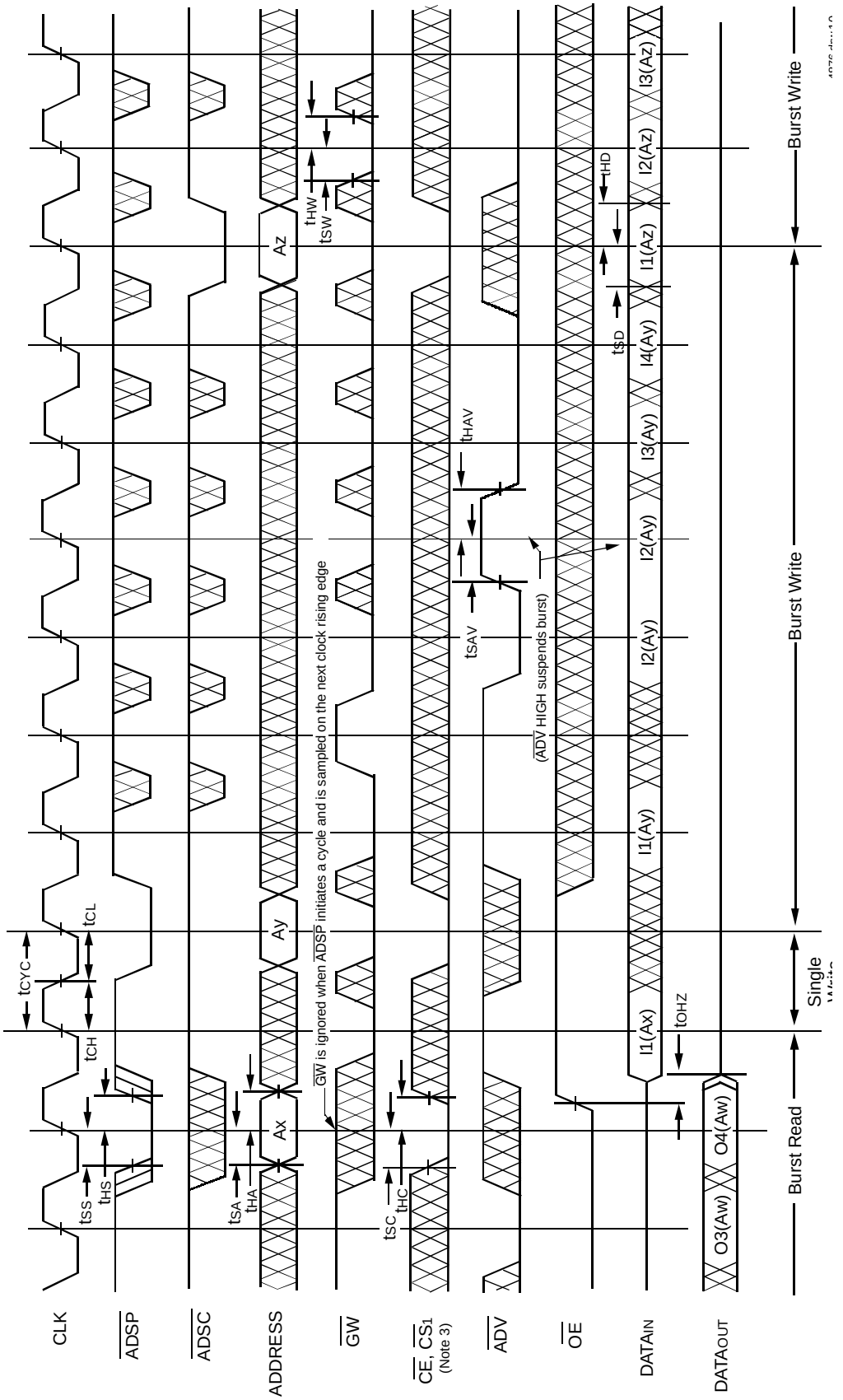
NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. $\overline{LBO}$ is Don't Care for this cycle.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS_0 is HIGH.

TIMING WAVEFORM OF COMBINED PIPELINED READ AND WRITE CYCLES(1,2,3)



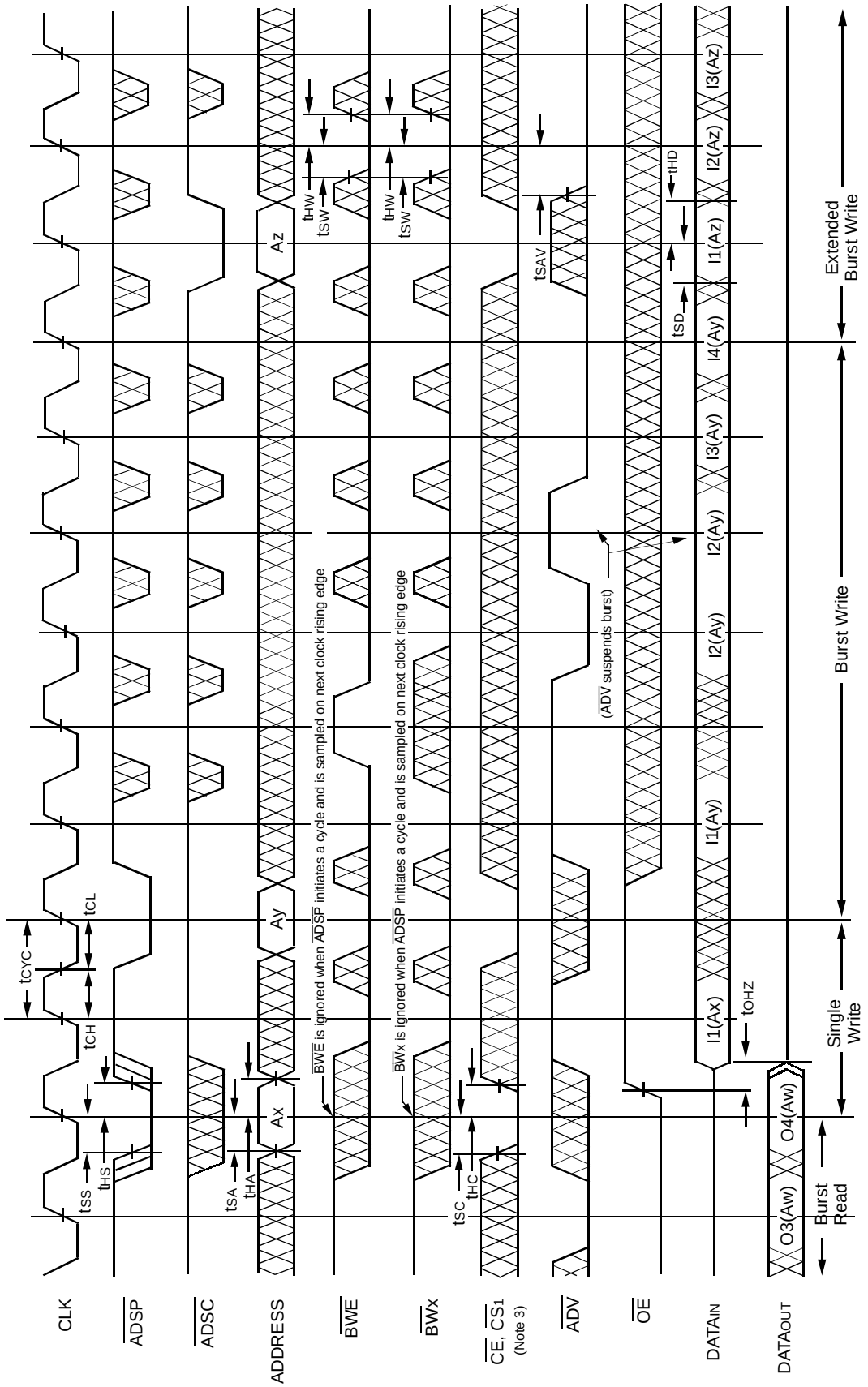
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS}_1$ are LOW, CS_0 is HIGH.
2. $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 - $\overline{GW}$ CONTROLLED(1,2,3)



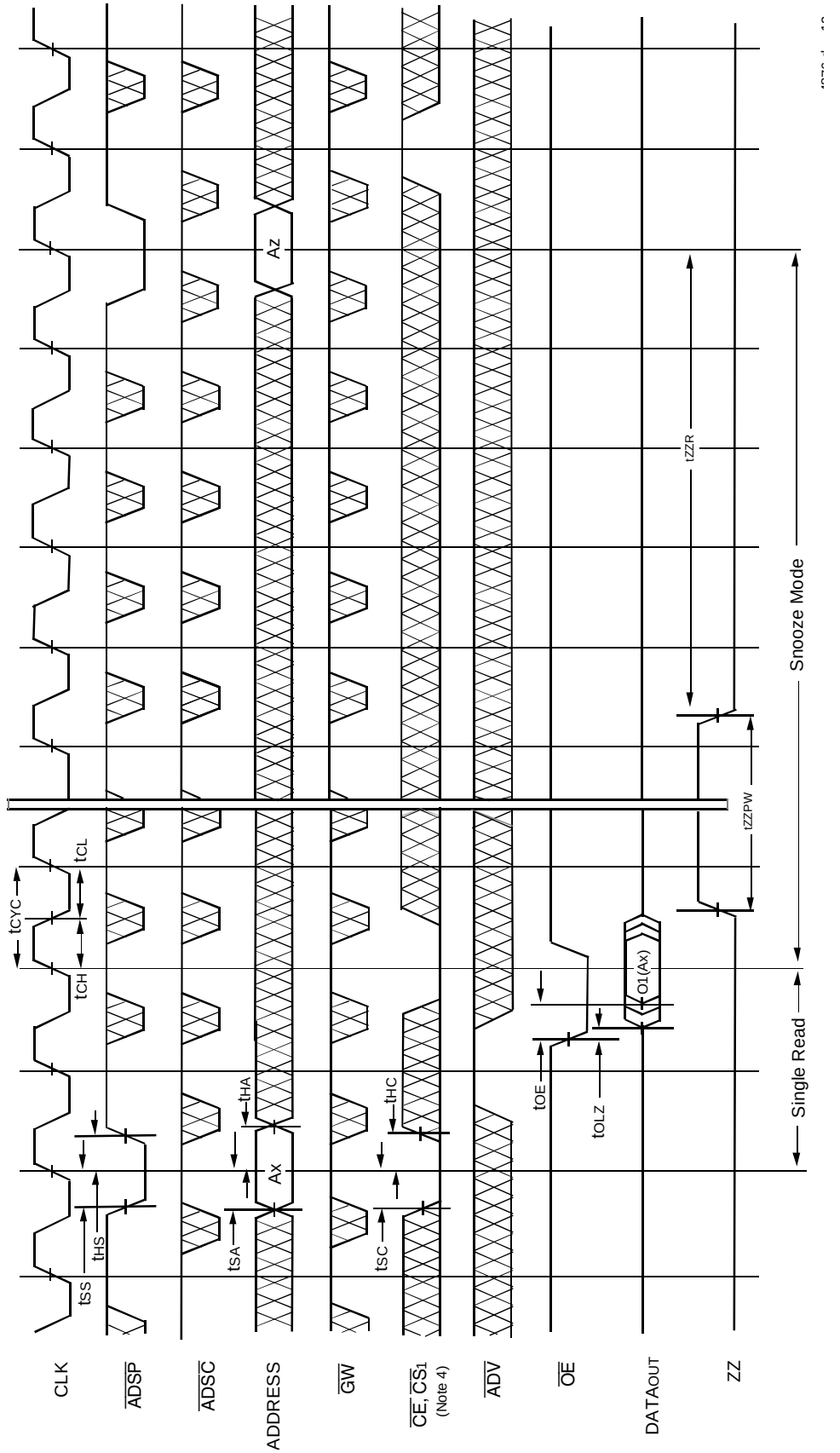
NOTES:
1. $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 - BYTE CONTROLLED(1,2,3)



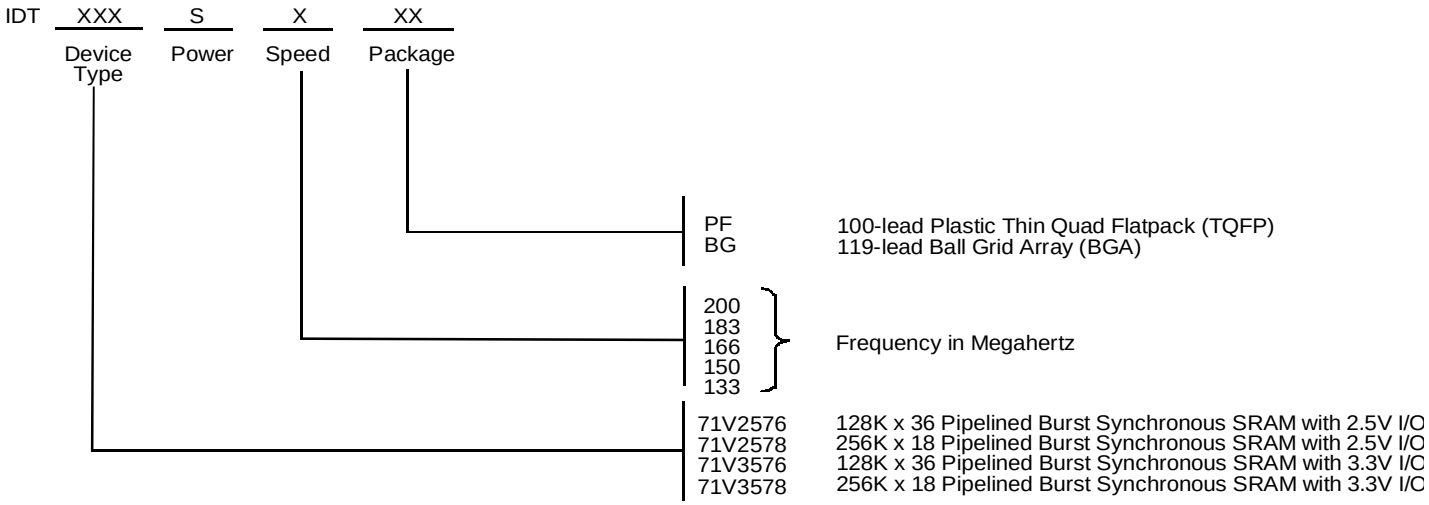
NOTES:
1. $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS_1}$ signals. For example, when $\overline{CE}$ and $\overline{CS_1}$ are LOW on this waveform, CS0 is HIGH.

TIMING WAVEFORM OF SLEEP (ZZ) AND POWER-DOWN MODES(1,2,3)



NOTES:
1. Device must power up in deselected Mode ($\overline{CE}$ and $\overline{CS}_1$ are HIGH, CS0 is LOW.)
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when CE and CS1 are LOW on this waveform, CS_0 is HIGH.

ORDERING INFORMATION



4876 drw 13

2975 Stender Way
Santa Clara, CA 95054

fax: 831-754-4547
www.idt.com

800-544-SRAM
SRAMHELP@IDT.COM