TC74HC259P/F

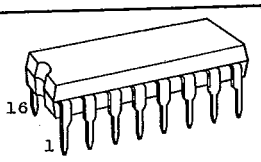
T-67-21-51

TC74HC259P/F 8-BIT ADDRESSABLE LATCH

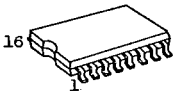
The TC74HC259 is a high speed CMOS 8-BIT ADDRESSABLE LATCH fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by A, B and C inputs. When $\overline{CLEAR}$ input is held "H" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "L" level, the data is written into the bit selected by A, B and C inputs, the other bits hold their previous conditions. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$($\overline{G}$) input held "H" level, write of all bits is inhibited regardless of A, B and C input, and their previous conditions are held. When $\overline{CLEAR}$ input is held "L" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "H" level, all bits are reset to "L" level regardless of the other inputs. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$ ($\overline{G}$) input held "L" level, all bits which isn't selected by A, B and C inputs are reset to "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS259



DIP16(3D16A-P)



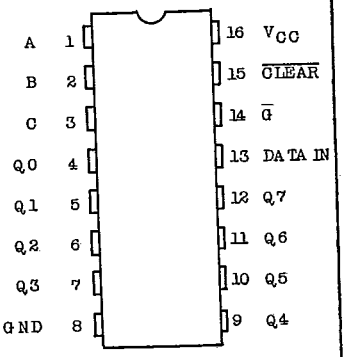
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

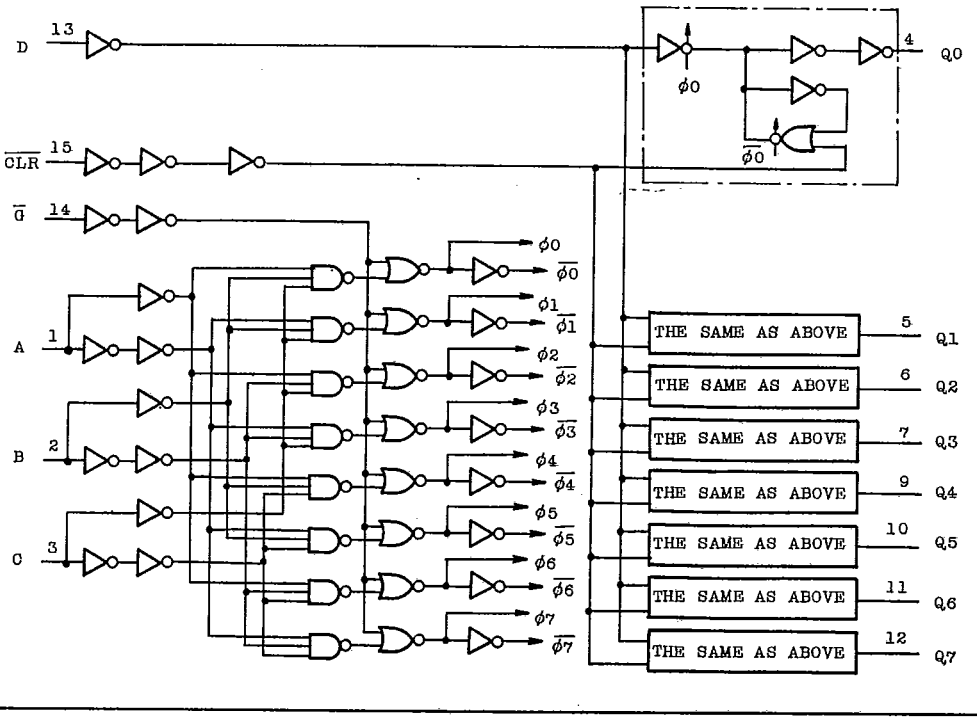
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : THE LEVEL AT THE DATA INPUT

Q_{i0} : THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i=0,1,·····,7).

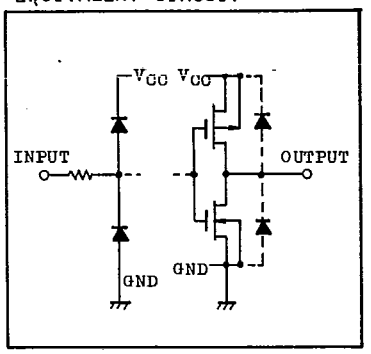
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

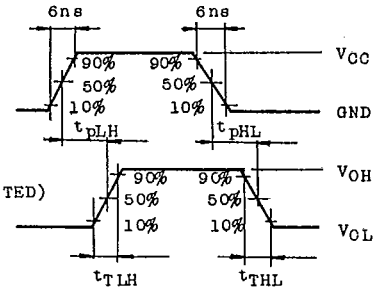
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (A, B, C - Q)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time ($\overline{G}$ - Q)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	15	23	-	29	
Minimum Pulse Width ($\overline{G}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (DATA)	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Hold Time (DATA)	t_h		2.0	-	10	25	-	30	
			4.5	-	2	5	-	6	
			6.0	-	2	5	-	5	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	32	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

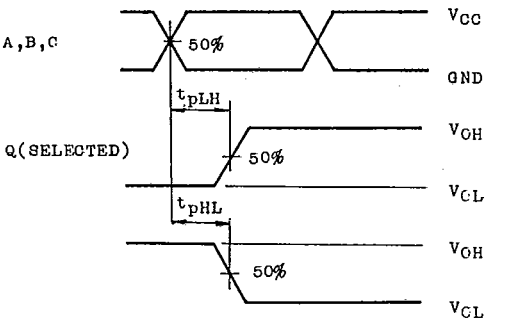
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

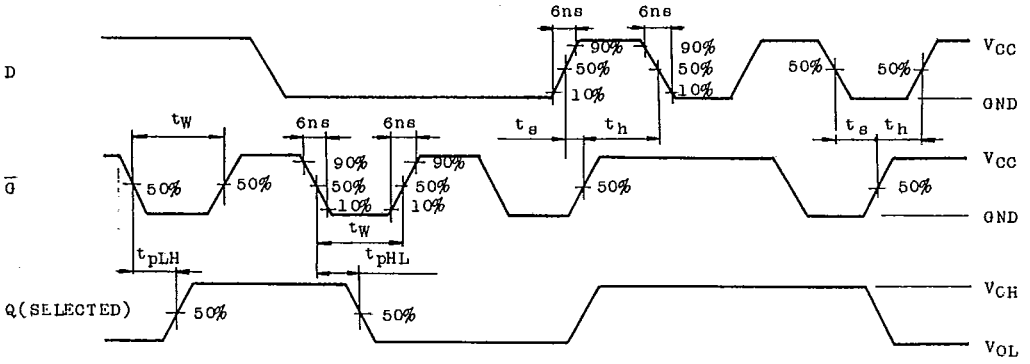
WAVEFORM 1. ($\overline{G}$=L, $\overline{CLR}$=H, A~C=STABLE)



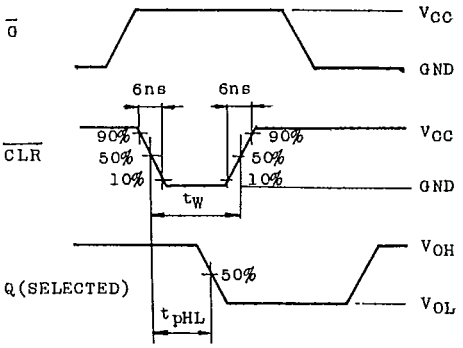
WAVEFORM 2. ($\overline{G}$=L)



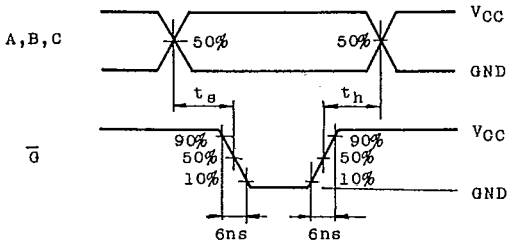
WAVEFORM 3. ($\overline{CLR}$=H, A~C=STABLE)



WAVEFORM 4. (D=H, A~C=STABLE)



WAVEFORM 5. ($\overline{CLR}$=H)



I_{CC}(Opr.) TEST CIRCUIT