Am29C841A/Am29C843A

High-Performance CMOS Bus Interface Latches

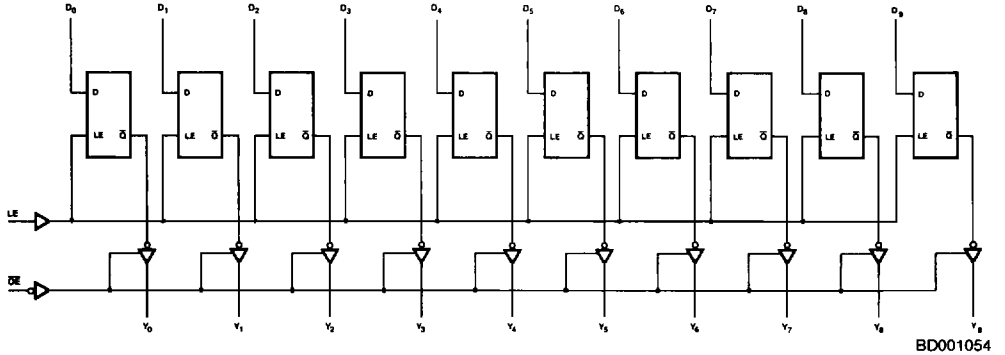
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - D-Y propagation delay = 5 ns typical
- Low standby power
- Very high output drive
  - I_{OL} = 48 mA Commercial, 32 mA Military
- JEDEC FCT-compatible specs
- Extra-wide (9- and 10-bit) data paths
- Proprietary edge-rate controlled outputs
- Power-up/down disable circuit provides for glitch-free power supply sequencing

BLOCK DIAGRAMS

Am29C841A



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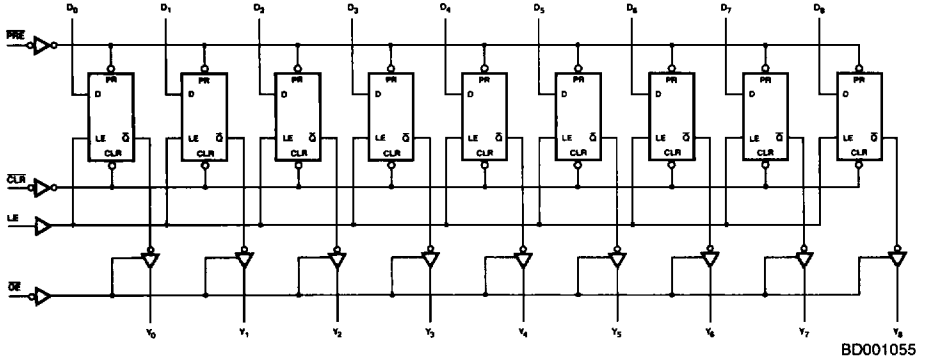
Am29C843A



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GENERAL DESCRIPTION

The Am29C841A and Am29C843A CMOS Bus Interface Latches are designed to eliminate the extra devices required to buffer stand alone latches and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A latches are produced with AMD's exclusive CS11SA CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C841A is a buffered, 10-bit version of the popular '373 function. The Am29C843A is a 9-bit buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C841A and Am29C843A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and ouput ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry provices for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

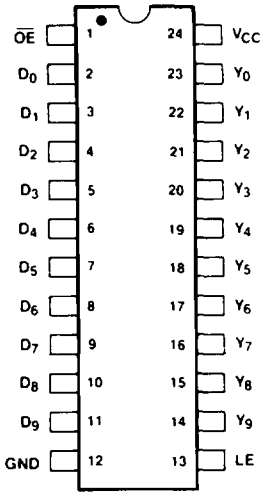
The Am29C841A and Am29C843A are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A).

CONNECTION DIAGRAMS
Top View

Am29C841A

DIPs*



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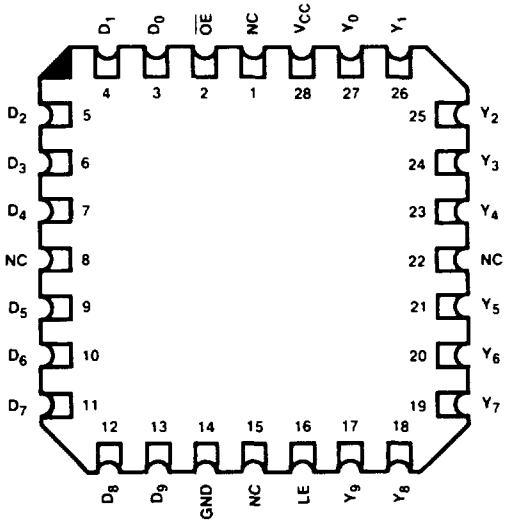
LCC**



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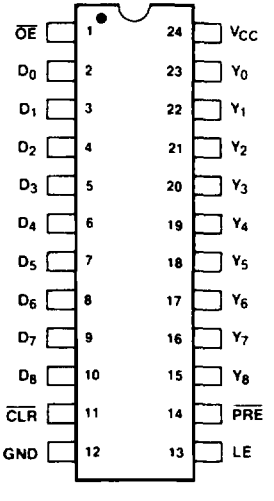
Am29C843A

DIPs*



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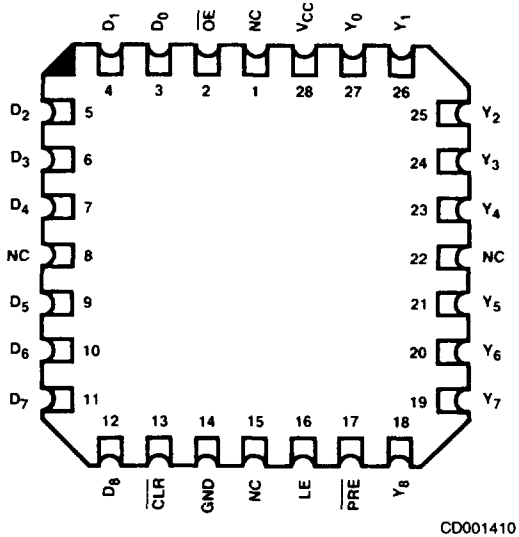
LCC**



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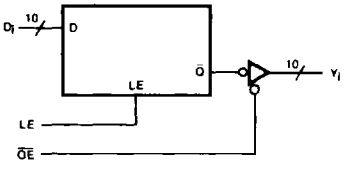
* Also available in 24-Pin Flatpack and Small Outline package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

LOGIC SYMBOLS

Am29C841A



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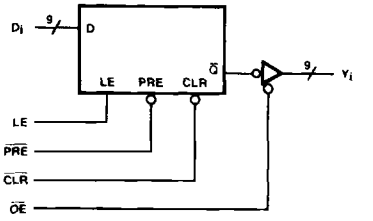
Am29C843A



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FUNCTION TABLES

Am29C841A

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	X	X	X	Z	Hi-Z
H	H	L	H	Z	Hi-Z
H	H	H	L	Z	Hi-Z
H	L	X	NC	Z	Latched (Hi-Z)
L	H	L	H	L	Transparent
L	H	H	L	H	Transparent
L	L	X	NC	NC	Latched

Am29C843A

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	$\overline{Q}_i$	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	H	Transparent
H	H	L	H	L	H	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	L	H	Preset
L	H	L	X	X	H	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	L	Z	Latched (Hi-Z)

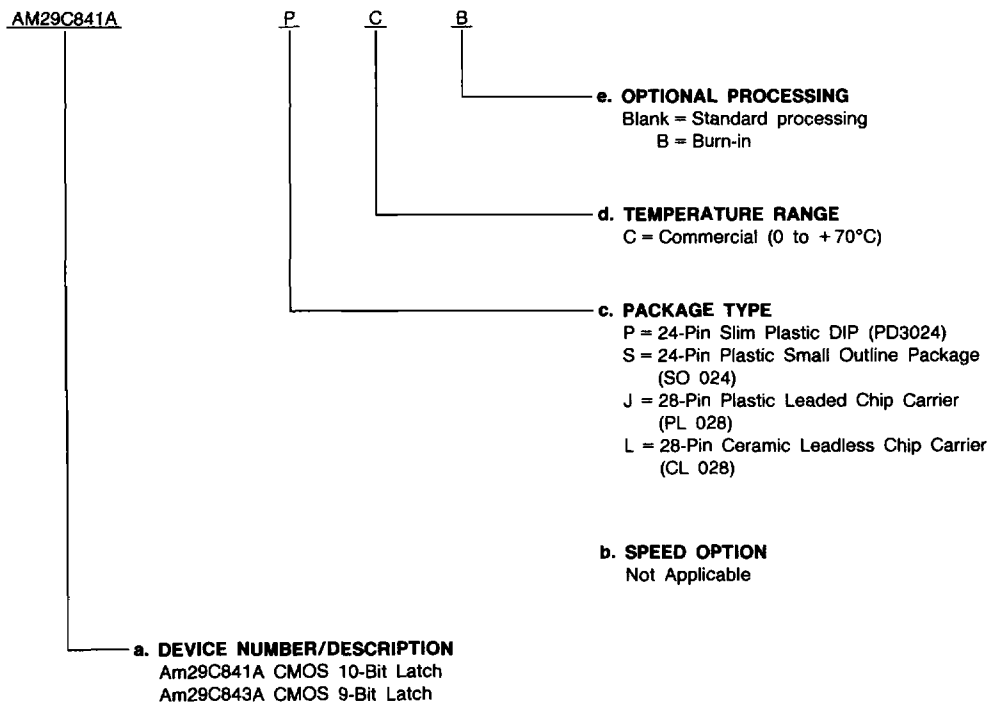
H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C841A	PC, PCB, SC, JC, LC
AM29C843A	

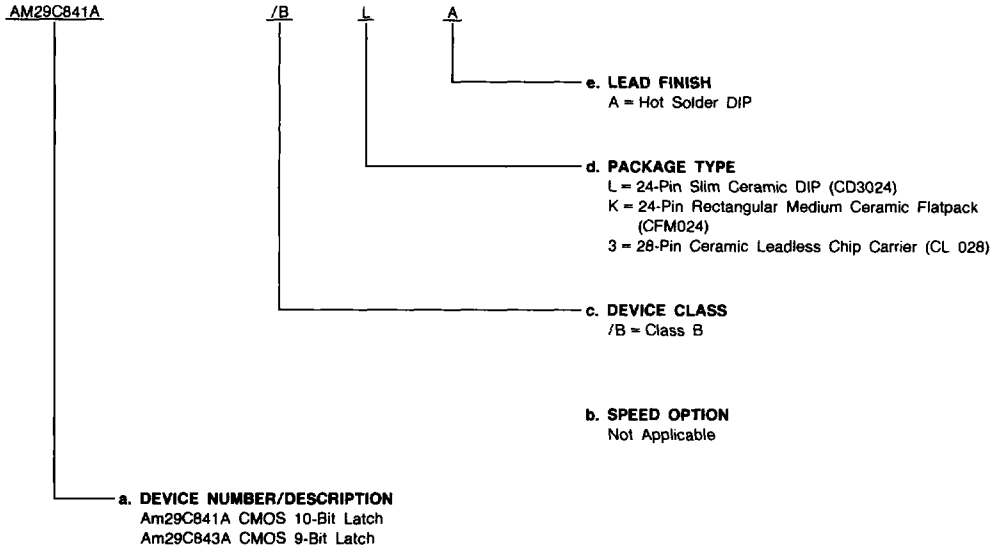
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C841A	/BLA, /BKA, /B3A
AM29C843A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C841A/Am29C843A

D_i Data Inputs (Input)
D_i are the latch data inputs.

Y_i Data Outputs (Output)
Y_i are the three state data outputs.

LE Latch Enable (Input, Active HIGH)
The latches are transparent when LE is HIGH. Input data is latched on a HIGH-to-LOW transition.

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, the latch data is passed to the Y_i outputs. When $\overline{OE}$ is HIGH, the Y_i outputs are in the high impedance state.

Am29C843A Only

$\overline{PRE}$ Preset (Input, Active LOW)
When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides the $\overline{CLR}$ pin. $\overline{PRE}$ will set the latch independent of the state of $\overline{OE}$.

$\overline{CLR}$ Clear (Input, Active LOW)
When $\overline{CLR}$ is LOW, the internal latch is cleared. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW and $\overline{PRE}$ is HIGH. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +6 V
DC Output Voltage ..... −0.5 V to +6 V
DC Input Voltage ..... −0.5 V to +6 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +70 mA
I_{SOURCE} ..... −30 mA
Total DC Ground Current .$(n \times I_{OL} + m \times I_{CCT})$ mA (Note 1)
Total DC V_{CC} Current .... $(n \times I_{OH} + m \times I_{CCT})$ mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	MIL I_{OL} = 32 mA			0.5	Volts
			COM'L I_{OL} = 48 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				−10	µA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V				−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V				5	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V, V_O = 5.5 V or 2.7 V (Note 3)				+10	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.4 V or GND (Note 3)				−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 4)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	mA
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OE}$, $\overline{PRE}$, $\overline{CLR}$, LE		3.0	mA/Bit
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 5)				275	µA/MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Off-state currents are only tested at worst-case conditions of V_{OUT} = 5.5 V or 0.0 V.
4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
5. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Test Conditions*	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
t_{PLH}	Data (D_i) to Output Y_i (LE = HIGH) (Note 1)		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		7.5		8.5	ns
t_{PHL}					7.5		8.5	ns
t_S	Data to LE Setup Time			2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		2.5		ns
t_{PLH}	Latch Enable (LE) to Y_i				8		9	ns
t_{PHL}					8		9	ns
t_{PLH}	Propagation Delay, Preset to Y_i				9		11	ns
t_{PHL}					9		11	ns
t_{REC}	Preset ($\overline{PRE}$ ⌐) to LE Setup Time			4		4		ns
t_{PLH}	Propagation Delay, Clear to Y_i				11		12	ns
t_{PHL}					11		12	ns
t_{REC}	Clear ($\overline{CLR}$ ⌐) to LE Setup Time			3		3		ns
t_{PWH}	LE Pulse Width	HIGH		4		4		ns
t_{PWL}	Preset Pulse Width	LOW		4		4		ns
t_{PWL}	Clear Pulse Width	LOW		4		4		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ⌙ to Y_i				9		9.5	ns
t_{ZL}					9		9.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ⌐ to Y_i				8		8.5	ns
t_{LZ}					8		8.5	ns

*See Test Circuit and Waveforms.

Notes: 1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (PID #10181A)