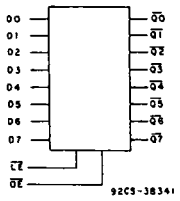
T-46-07-11

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

File Number **1599**

HARRIS SEMICOND SECTOR 27E D 4302271 0017825 6 HAS

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Inverting Transparent Latch, 3-State Outputs

Type Features:
- *Common latch-enable control*
- *Common 3-state output-enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 13 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (Data to Output)*

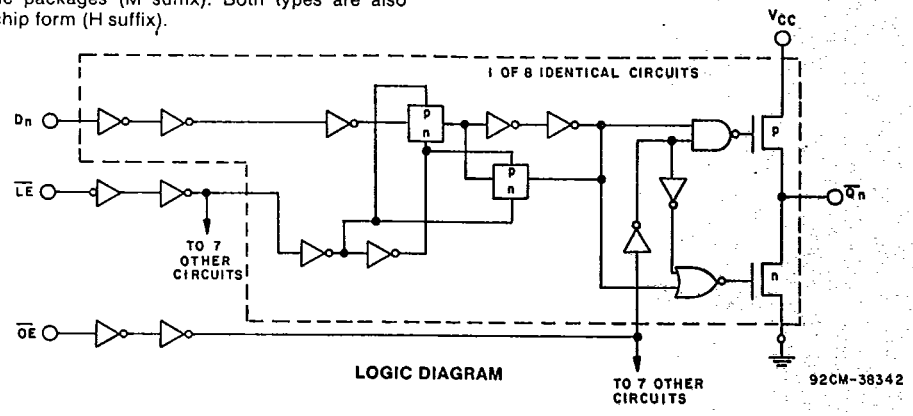
The RCA CD54/74HC/HCT533/563 are high-speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs will be in the high impedance state. The latch operation is independent of the state of the output enable.

The CD54/74HC533 and CD54/74HCT533 are identical in function to the CD54/74HC563 and CD54/74HCT563 but have different pinouts. The CD54/74HC533 and CD54/74HCT533 are similar to the CD54/74HC373 and CD54/74HCT373; the latter are non-inverting types.

The CD54HC/HCT533/563 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT533/563 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features
- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC};
  @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



LOGIC DIAGRAM

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

MAXIMUM RATINGS, *Absolute-Maximum Values:*

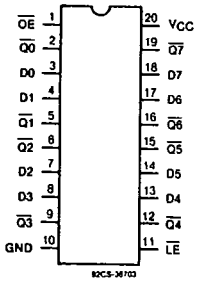
DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) ..... ± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



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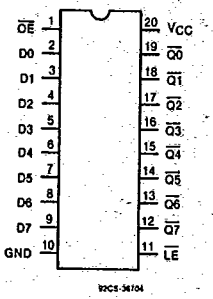
CD54/74HC533, CD54/74HCT533
TERMINAL ASSIGNMENT



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CD54/74HC563, CD54/74HCT563
TERMINAL ASSIGNMENT

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC533/CD54HC533 CD74HC563/CD54HC563										CD74HCT533/CD54HCT533 CD74HCT563/CD54HCT563									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin. 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0 — D7	0.15
$\overline{LE}$	0.30
$\overline{OE}$	0.55

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC 533	HC 563	HCT 533	HCT 563	UNITS
Propagation Delay Data to Qn Output Fig. 3	t_{PLH} t_{PHL}	15	13	12	14	12	ns
Propagation Delay $\overline{LE}$ to Qn Output Fig. 4	t_{PLH} t_{PHL}	15	14	13	16	14	ns
Output High Z to High Level, Fig. 6	t_{PZH}	15	12	12	14	14	ns
Output High Z to Low Level, Fig.7	t_{PZL}	15	12	12	14	14	ns
Output High Level to High Z, Fig. 6	t_{PHZ}	15	12	12	12	14	ns
Output Low Level to High Z, Fig. 7	t_{PLZ}	15	12	12	12	14	ns
Power Dissipation Capacitance	C_{PD}*	—	42	42	42	42	pF

*C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:

P_D (total power per latch) = $C_{PD}\ V_{CC}^2\ f_i + \Sigma\ C_L\ V_{CC}^2\ f_o$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25° C HC Min.	HC Max.	HCT Min.	HCT Max.	-40° C to +85° C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55° to +125° C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
$\overline{LE}$ Pulse Width (Fig. 4)	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	ns
Set-up Time Data to $\overline{LE}$ (Fig. 5)	t_{su}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	ns
		6	9	—	—	—	11	—	—	—	13	—	—	—	ns
Hold Time Data to $\overline{LE}$ (Fig. 5)	t_H 533	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	8	—	9	—	10	—	11	—	12	—	ns
		6	6	—	—	—	8	—	—	—	7	—	—	—	ns
	563	2	4	—	—	—	4	—	—	—	4	—	—	—	ns
		4.5	4	—	5	—	4	—	5	—	4	—	5	—	ns
		6	4	—	—	—	4	—	—	—	4	—	—	—	ns

TRUTH TABLE

$\overline{Output\ Enable}$	$\overline{Latch\ Enable}$	Data	Q Output
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

Note:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transition.
h = High voltage level one set-up time prior to the high to low latch enable transition
X = Don't care
Z = High impedance state

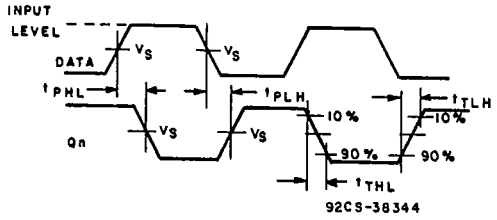
T-46-07-11

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

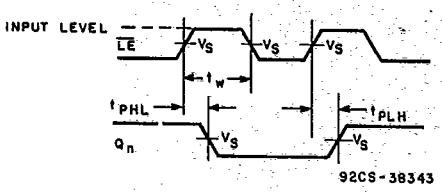
CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS +25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay Data to Qn	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
	t_{PHL}	4.5	—	33	—	34	—	41	—	43	—	50	—	51	ns
	533	6	—	28	—	—	—	35	—	—	—	43	—	—	
$\overline{LE}$ to Qn	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	ns
	533	6	—	30	—	—	—	37	—	—	—	45	—	—	
Enable Times	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PZL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
	533	6	—	26	—	—	—	33	—	—	—	38	—	—	
Disable Times	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PLZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
	533	6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay Data to Qn	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
	563	6	—	26	—	—	—	33	—	—	—	38	—	—	
$\overline{LE}$ to Qn	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
	t_{PHL}	4.5	—	33	—	35	—	41	—	44	—	50	—	53	ns
	563	6	—	28	—	—	—	35	—	—	—	43	—	—	
Enable and Disable Times	t_{PZH}, t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
	563	6	—	26	—	—	—	33	—	—	—	38	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563



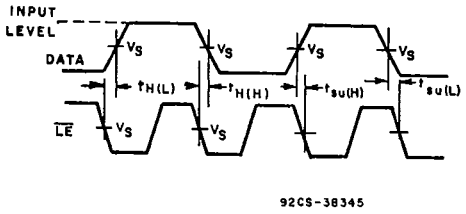
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 — Data to Q_n output propagation delays and output transition times.



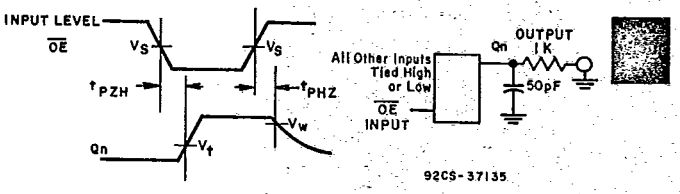
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 — Latch enable propagation delays.



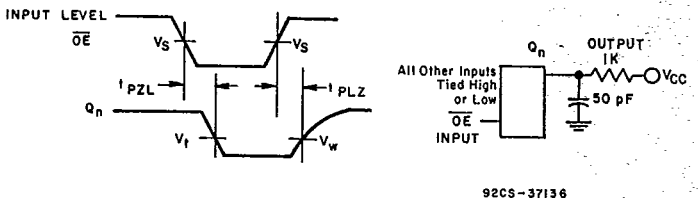
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 — Latch enable pre-requisite times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_W	90% V_{CC}	4.15 V

Fig. 6 - 3-state propagation delays.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_W	10% V_{CC}	0.45 V

Fig. 7 — 3-state propagation delays.