HARRIS

HM-65262

16K x 1 Asynchronous CMOS Static RAM

Features

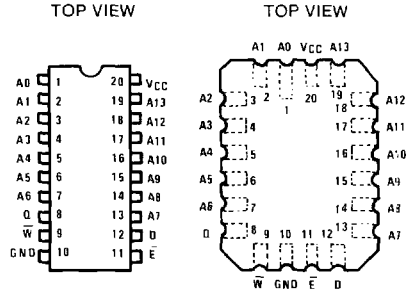
- Low Standby Current.....50μA
- Low Operating Current.....50mA
- Fast Access Time.....55/70/85ns
- Low Voltage Data Retention at 2.0V
- CMOS/TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Single 5 Volt Supply
- Gated Inputs - No Pull-up or Pull-down Resistors Required
- Wide Temperature Range.....-55°C to +125°C
- Easy Microprocessor Interfacing

Description

The HM-65262 is a CMOS 16384 x 1 bit Static Random Access Memory manufactured using the Harris advanced SAJI VI process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262 is available in both the JEDEC standard 20-pin, 0.300 inch wide dual-in-line and 20 pad LCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

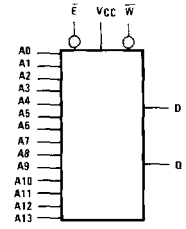
The HM-65262, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

Pinouts



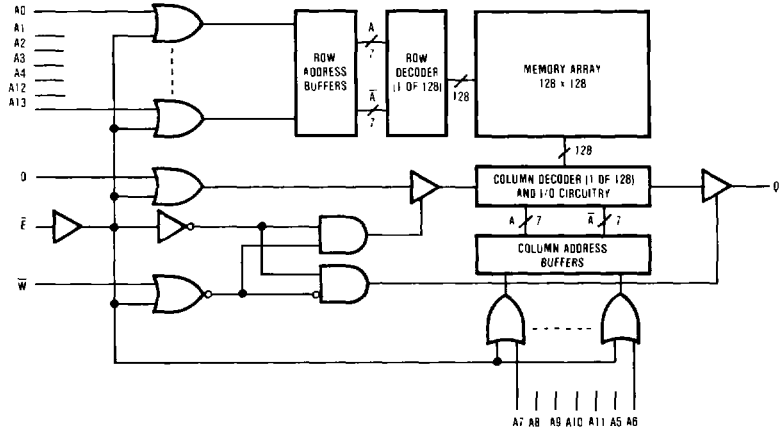
DIP LCC

Logic Symbol



A — Address Input
$\overline{E}$ — Chip Enable
$\overline{W}$ — Write Enable
D — Data Input
Q — Data Output

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65262B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	50	μA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	μA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	30	μA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	μA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100μA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES.

1. Input pulse levels. 0 to 3.0V, Input rise and fall times. 5ns (max). Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	70	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	70	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	70	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	40	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	70	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	55	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	40	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	30	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(16) TWHQX	Write Disable Output Enable Time	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	55	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	55	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	55	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	40	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	30	—	ns	(Notes 1, 4)
(24) TEHDX	Data Hold Time	0	—	ns	(Notes 1, 4)

NOTES.

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V: Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating. 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65262-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	µA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	30	µA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times. 5ns (max). Input and output timing reference level. 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating. 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	85	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	85	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	85	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	40	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	85	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	65	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	45	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	35	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	40	ns	(Notes 2, 4)
(16) TWHQX	Write Disable Output Enable Time	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	65	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	45	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	35	—	ns	(Notes 1, 4)
(24) TEHDX	Data Hold Time	0	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262S-9 ..... -40°C to +85°C

D.C. Electrical Specifications (Note 1) VCC = 5V ± 10%; T_A = HM-65262S-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	µA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	30	µA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V. Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V, Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	55	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	55	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	55	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	30	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	55	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	45	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	35	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	25	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(16) TWHQX	Write Disable Output Enable Time	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	45	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	45	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	45	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	35	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	25	—	ns	(Notes 1, 4)
(24) TEHDX	Data Hold Time	0	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V. Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262B-9 ..... -40°C to +85°C

D.C. Electrical Specifications (Note 1) VCC = 5V ± 10%, T_A = HM-65262B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	50	μA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	μA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	30	μA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	μA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100μA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	*Read Cycle Time*	70	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	70	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	70	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	30	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	70	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	55	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	40	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	30	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(16) TWHQX	*Write Disable Output Enable Time*	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	55	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	55	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	55	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	40	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	30	—	ns	(Notes 1, 4)
(24) TEHDX	*Data Hold Time*	0	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V. Input rise and fall times: 5ns (max). Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. *Tested at initial design and after major design changes.*
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262-9 ..... -40°C to +85°C

D.C. Electrical Specifications (Note 1) VCC = 5V ± 10%; T_A = HM-65262-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	20	µA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	30	µA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:

1. Input pulse levels: 0 to 3.0V. Input rise and fall times: 5ns (max); Input and output timing reference level. 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	85	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	85	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	85	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	30	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	85	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	65	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	45	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	35	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(16) TWHQX	Write Disable Output Enable Time	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	65	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	45	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	35	—	ns	(Notes 1, 4)
(24) TEHDX	Data Hold Time	0	—	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. *Tested at initial design and after major design changes.*
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 15°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 69°C/W (CERDIP Package), TBD (LCC Package)
Gate Count ..... 26256 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HM-65262C-9 ..... -40°C to +85°C

D.C. Electrical Specifications (Note 1) VCC = 5V ± 10%; T_A = HM-65262C-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	900	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	—	5	mA	IO = 0, $\overline{E}$ = 2.2V
ICCEN	Enabled Supply Current	—	50	mA	IO = 0, $\overline{E}$ = 0.8V
ICCOP	Operating Supply Current (Note 3)	—	50	mA	IO = 0, $\overline{E}$ = 0.8V, f = 1MHz
ICCDR	Data Retention Supply Current	—	400	µA	VCC = 2.0V, $\overline{E}$ = VCC
ICCDR1	Data Retention Supply Current	—	550	µA	VCC = 3.0V, $\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOL	Output Low Voltage	—	0.4	V	IO = 8.0mA
VOH1	Output High Voltage	2.4	—	V	IO = -4.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	—	V	IO = -100µA
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.2	VCC+0.3	V	

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES.

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max). Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

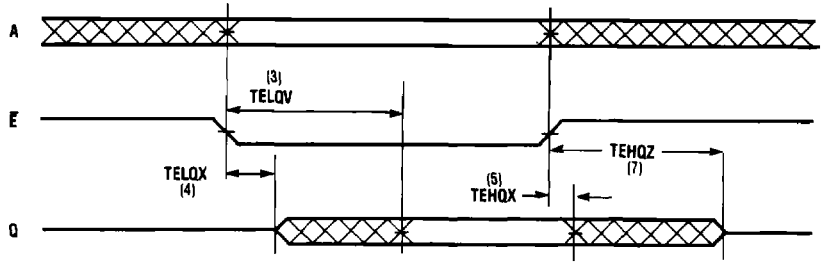
A.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
(1) TAVAX	Read Cycle Time	85	—	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	—	85	ns	(Notes 1, 4)
(3) TELQV	Chip Enable Access Time	—	85	ns	(Notes 1, 4)
(4) TELQX	Chip Enable Output Enable Time	5	—	ns	(Notes 2, 4)
(5) TEHQX	Chip Disable Output Hold Time	5	—	ns	(Notes 2, 4)
(6) TAXQX	Address Invalid Output Hold Time	5	—	ns	(Notes 2, 4)
(7) TEHQZ	Chip Disable Output Disable Time	—	30	ns	(Notes 2, 4)
WRITE CYCLE					
(8) TAVAX	Write Cycle Time	85	—	ns	(Notes 1, 4)
(9) TELWH	Chip Enable to End of Write	65	—	ns	(Notes 1, 4)
(10) TWLWH	Write Enable Pulse Width	45	—	ns	(Notes 1, 4)
(11) TAVWL	Address Setup Time	0	—	ns	(Notes 1, 4)
(12) TWHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(13) TDVWH	Data Setup Time	35	—	ns	(Notes 1, 4)
(14) TWHDX	Data Hold Time	0	—	ns	(Notes 1, 4)
(15) TWLQZ	Write Enable Output Disable Time	—	30	ns	(Notes 2, 4)
(16) TWHQX	Write Disable Output Enable Time	0	—	ns	(Notes 2, 4)
(17) TAVWH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(18) TAVEL	Address Setup Time	0	—	ns	(Notes 1, 4)
(19) TEHAX	Address Hold Time	0	—	ns	(Notes 1, 4)
(20) TAVEH	Address Valid to End of Write	65	—	ns	(Notes 1, 4)
(21) TELEH	Enable Pulse Width	65	—	ns	(Notes 1, 4)
(22) TWLEH	Write to End of Write	45	—	ns	(Notes 1, 4)
(23) TDVEH	Data Setup Time	35	—	ns	(Notes 1, 4)
(24) TEHDX	Data Hold Time	0	—	ns	(Notes 1, 4)

NOTES:

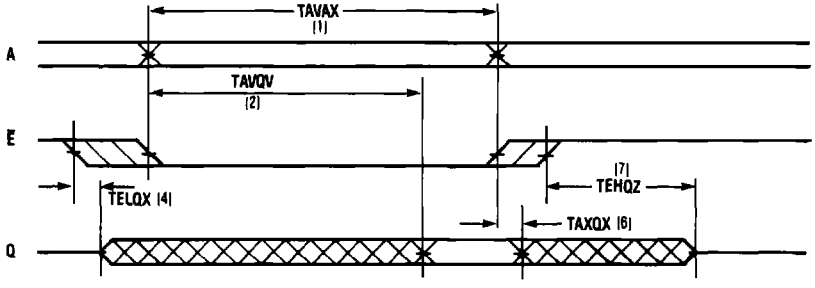
1. Input pulse levels: 0 to 3.0V. Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

READ CYCLE 1: CONTROLLED BY $\overline{E}$



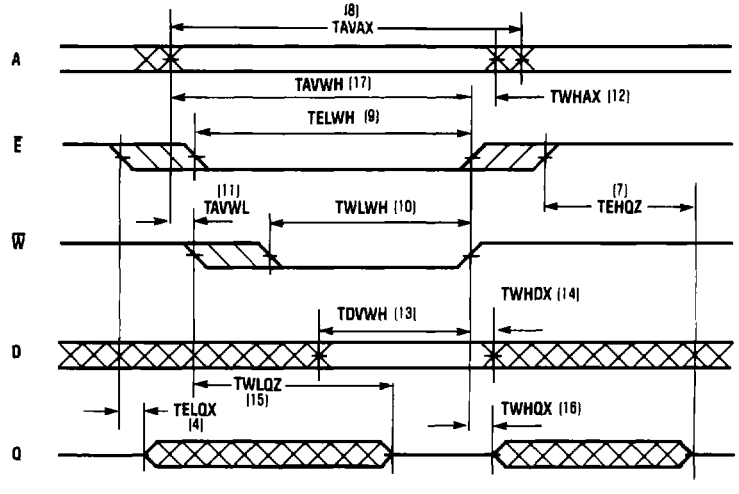
NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS



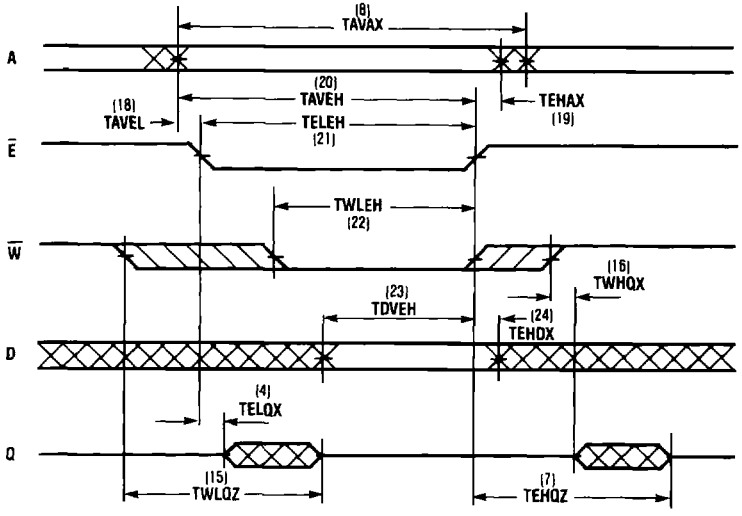
NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

WRITE CYCLE 1 TIMING: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

WRITE CYCLE 2: CONTROLLED BY E (EARLY WRITE)



NOTE: *In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding* TWLQZ (Max) - TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughout the cycle.

The address must remain stable whenever $\overline{E}$ and $\overline{W}$ are both low.