



High Speed SRAM

32K-Word By 8 Bit

CS18HS02563

Revision History

<u>Rev. No</u>	<u>History</u>	<u>Issue Date</u>
1.1	Add green code in part no.	Jul. 22,2005
1.2	Add in 28L TSOP 1 –8x13.4mm	Mar. 10,2006
1.3	Revise speed option and DC/AC characteristics	Mar. 7,2007



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■ DESCRIPTION

The CS18HS02563 series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the CS18HS02563 series products exhibit very high-speed performance with single +3.3-volt power supply while requiring low power and no clock or refreshing to operate. The CS18HS02563 is packed in 28-pin SOP-330mil, 28-pin SOJ-300mil 28-pin TSOP 1-8x13.4mm and Skinny 28-pin PDIP-300mil.

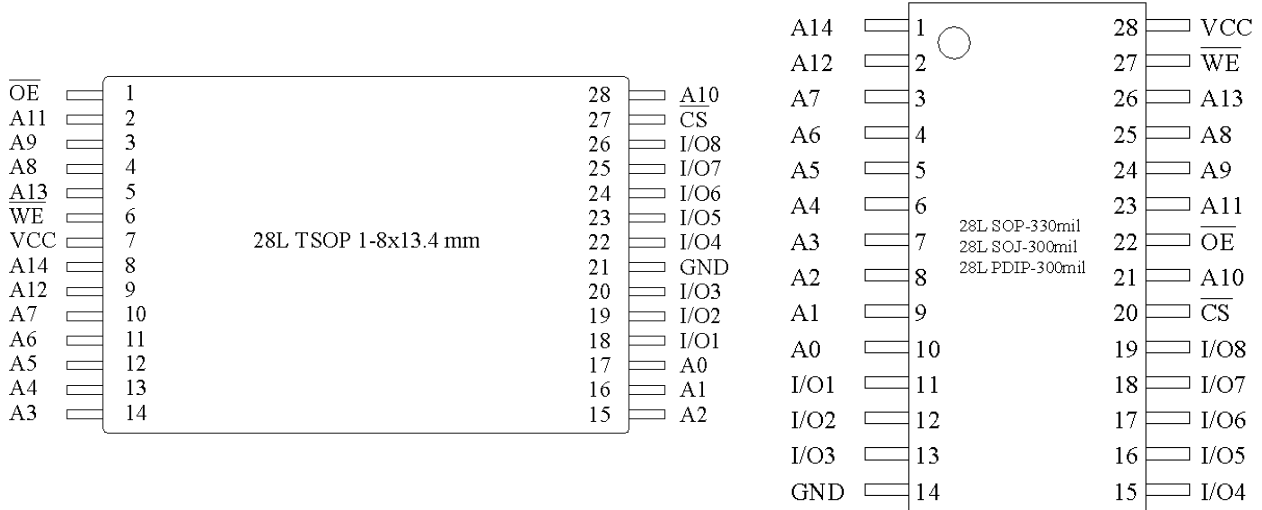
■ FEATURES

1. 32,768-word x 8-bit organization
2. Low operation voltage: 3.0~3.6V
3. Fully static operation: no clock or refreshing required
4. LVTTTL-compatible inputs and outputs
5. Common I/O capability
6. Low power consumption
 - Active: 100/90 mA (Max.)
 - Standby: 2 mA
7. Very high speed access: 10/12 ns (Max.)
8. Output Enable (\overline{OE}) available for very fast access
9. Standard pin configuration
 - 28 SOP - 330mil
 - 28 TSOP (I) - 8*13.4mm
 - 28 SOJ - 300mil
 - Skinny 28 PDIP - 300mil

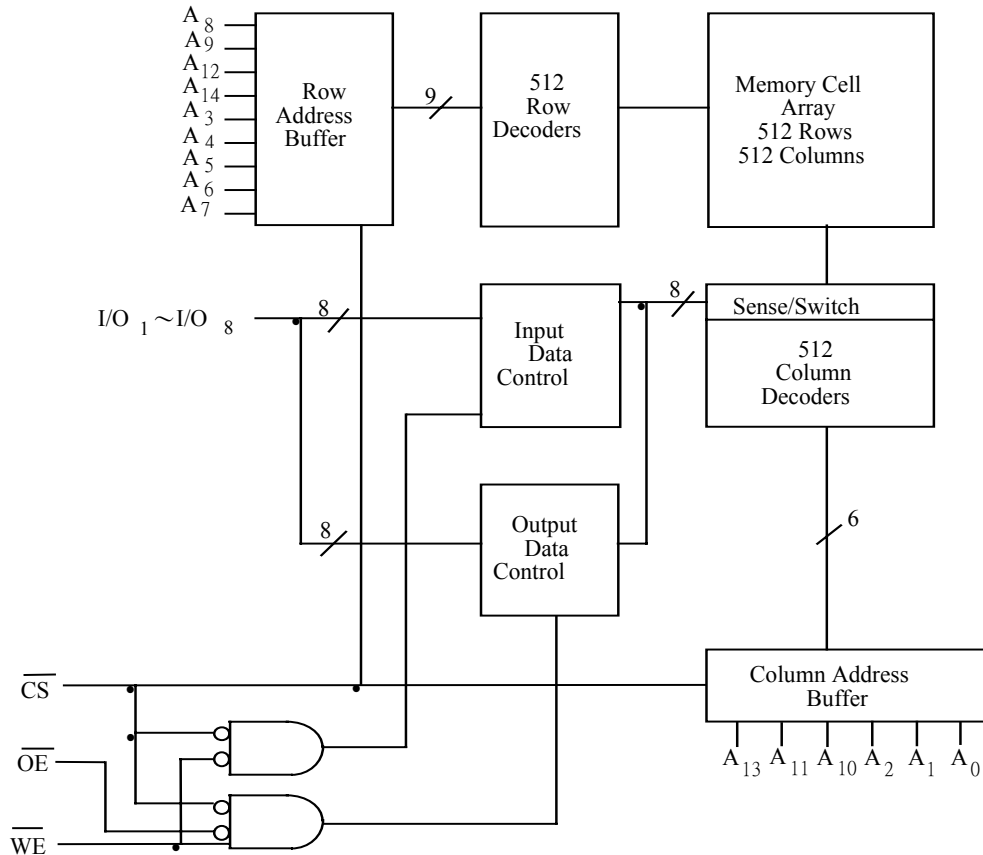
■ Product Family

Part No.	Operating Temp	Vcc. Range	Speed (ns)	Supply Current mA (Max.)	Package Type
CS18HS02563A	0~70°C	3.0~3.6V	10	100	28 SOP
CS18HS02563B					28 TSOP
CS18HS02563J			12	90	28 SOJ
CS18HS02563R					Skinny 28 PDIP

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM





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■ PIN DESCRIPTIONS

Symbols	Functions
A0~A14	Address Inputs
I/O1~I/O8	Data Inputs / Outputs
\overline{CS}	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
VDD	Power Supply
VSS	Ground

■ TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	I/O1~I/O8	VDD Current
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

■ ABSOLUTE MAXIMUM RATINGS

Parameters	Rating	Unit
Supply Voltage to Vss	-0.5 to +4.6	V
Input/Output to Vss	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	3.3V±5%



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■ DC ELECTRICAL CHARACTERISTICS

(VDD = 3.3V, VSS = 0V, Ta = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max	Unit	
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V	
Input High Voltage	V _{IH}	-	2.1	-	V _{DD} +0.3	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , \overline{CS} = V _{IH} or \overline{OE} = V _{IH} or \overline{WE} = V _{IL}	-10	-	+10	μA	
Output Low Voltage	V _{OL}	I _{OL} = +8.0mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	-	-	V	
Operating Power Supply Current	I _{DD}	\overline{CS} = V _{IL} , I/O = 0 mA Cycle = MIN Duty = 100%	10	-	-	100	mA
			12	-	-	90	mA
Standby Power Supply Current	I _{SB}	\overline{CS} = V _{IH} , Cycle = MIN Duty = 100%	-	-	15	mA	
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	2	mA	

Note: Typical characteristics are measured at VDD = 3.3V, Ta = 25°C

■ AC CHARACTERISTICS

Capacitances

(VDD = 3.3V, Ta = 25°C, f = 1 MHz)

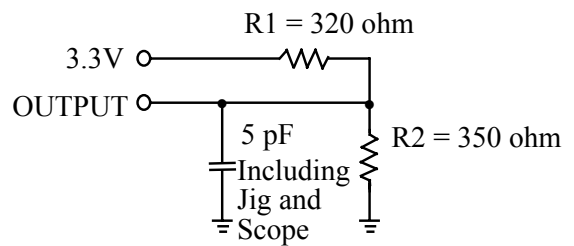
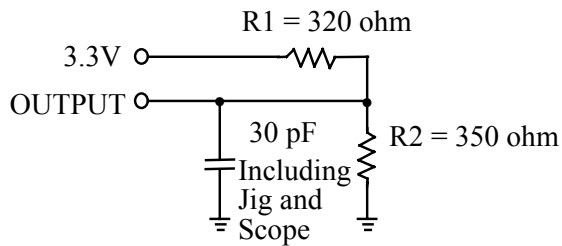
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

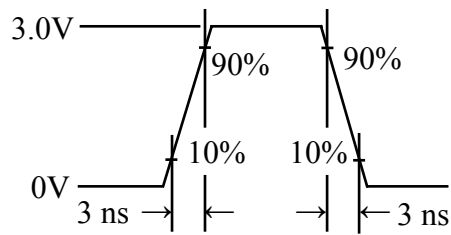
AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, IOH/IOL = -4 mA / 8 mA

■ AC Test Loads and Waveforms



(For T_{CLZ} , T_{OLZ} , T_{CHZ} , T_{OHZ} , T_{WHZ} , T_{OW})





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■ AC PERFORMANCES

(VDD = 3.3V, VSS = 0V, Ta = 0 to 70°C)

(1) Read Cycle

Parameters	Symbols	CS18HS02563-10		CS18HS02563-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	TRC	10	-	12	-	ns
Address Access Time	TAA	-	10	-	12	ns
Chip Select Access Time	TACS	-	10	-	12	ns
Output Enable to Output Valid	TAOE	-	6	-	7	ns
Chip Selection to Output in Low Z	TCLZ*	3	-	3	-	ns
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	ns
Chip Deselection to Output in High Z	TCHZ*	-	5	-	6	ns
Output Disable to Output in High Z	TOHZ*	-	5	-	6	ns
Output Hold from Address Change	TOH	3	-	3	-	ns

*These parameters are sampled but not 100% tested

(2) Write Cycle

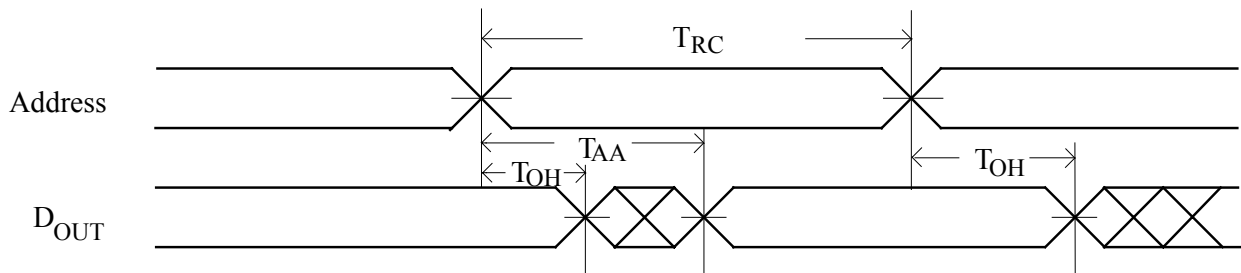
Parameters	Symbols	CS18HS02563-10		CS18HS02563-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	TWC	10	-	12	-	ns
Chip Selection to End of Write	TCW	8	-	10	-	ns
Address Valid to End of Write	TAW	8	-	10	-	ns
Address Setup Time	TAS	0	-	0	-	ns
Write Pulse Width	TWP	8	-	10	-	ns
Write Recovery Time	TWR	0	-	0	-	ns
Data Valid to End of Write	TDW	6	-	8	-	ns
Data Hold from End of Write	TDH	0	-	0	-	ns
Write to Output in High Z	TWHZ*	-	5	-	6	ns
Output Disable to Output in High Z	TOHZ*	-	5	-	6	ns
Output Active from End of Write	TOW	0	-	0	-	ns

*These parameters are sampled but not 100% tested.

■ Timing Waveforms

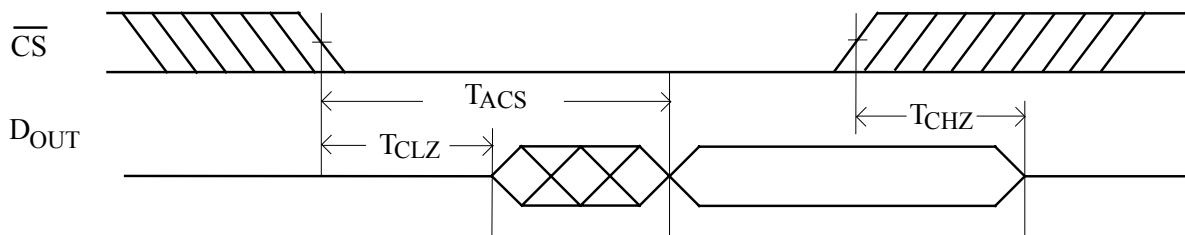
Read Cycle 1

(Address Controlled)



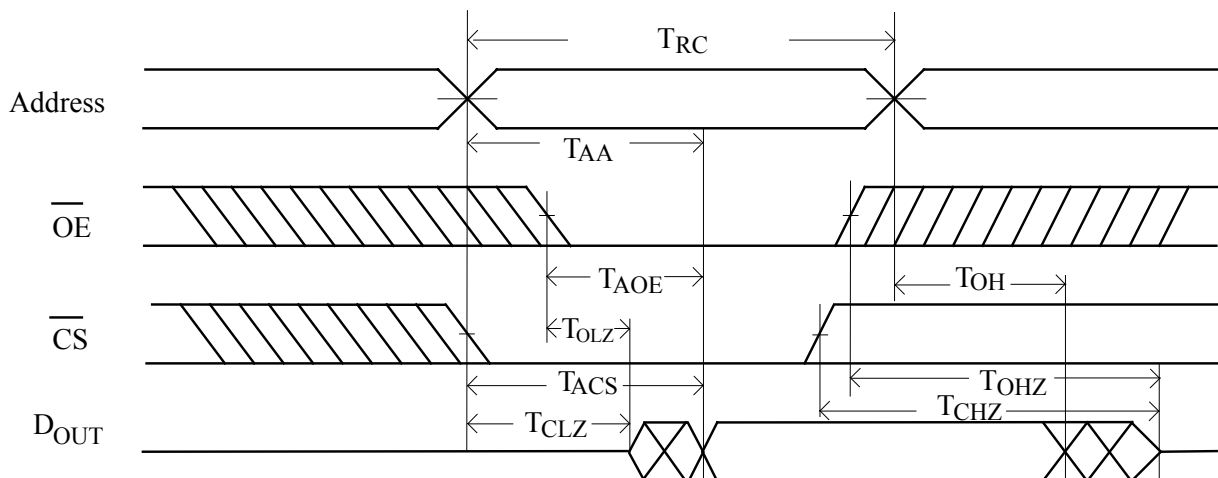
Read Cycle 2

(Chip Select Controlled)



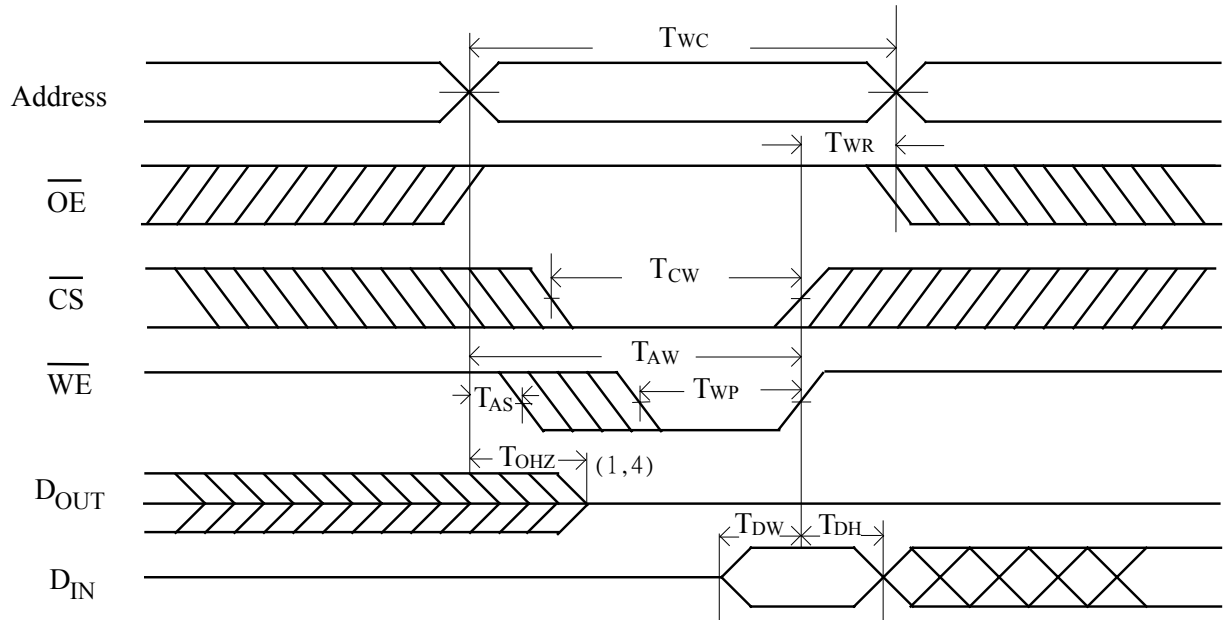
Read Cycle 3

(Output Enable Controlled)



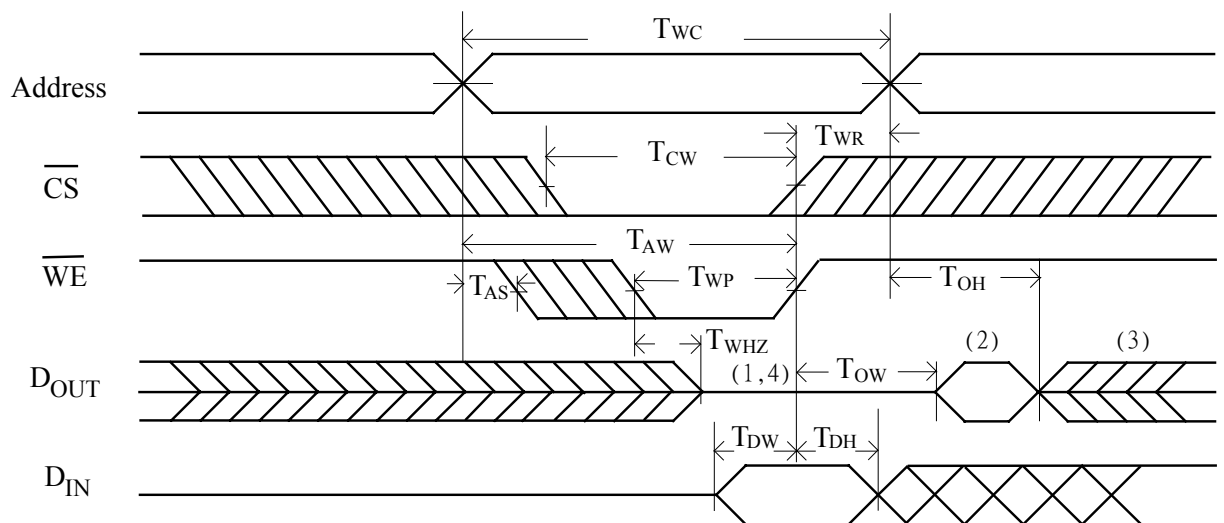
Write Cycle 1

(\overline{OE} Clock)



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)

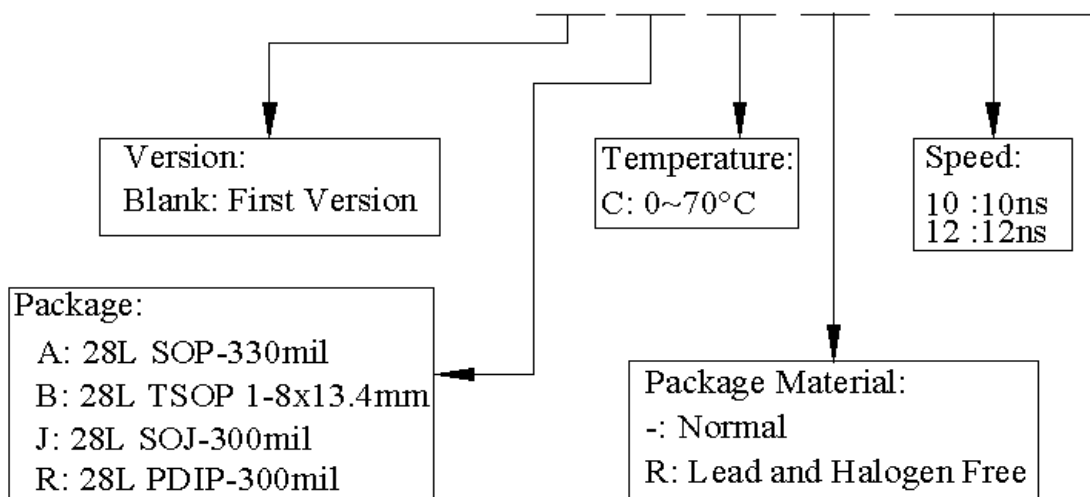


Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $\text{CL} = 5\text{pF}$. This parameter is guaranteed but not 100% tested.

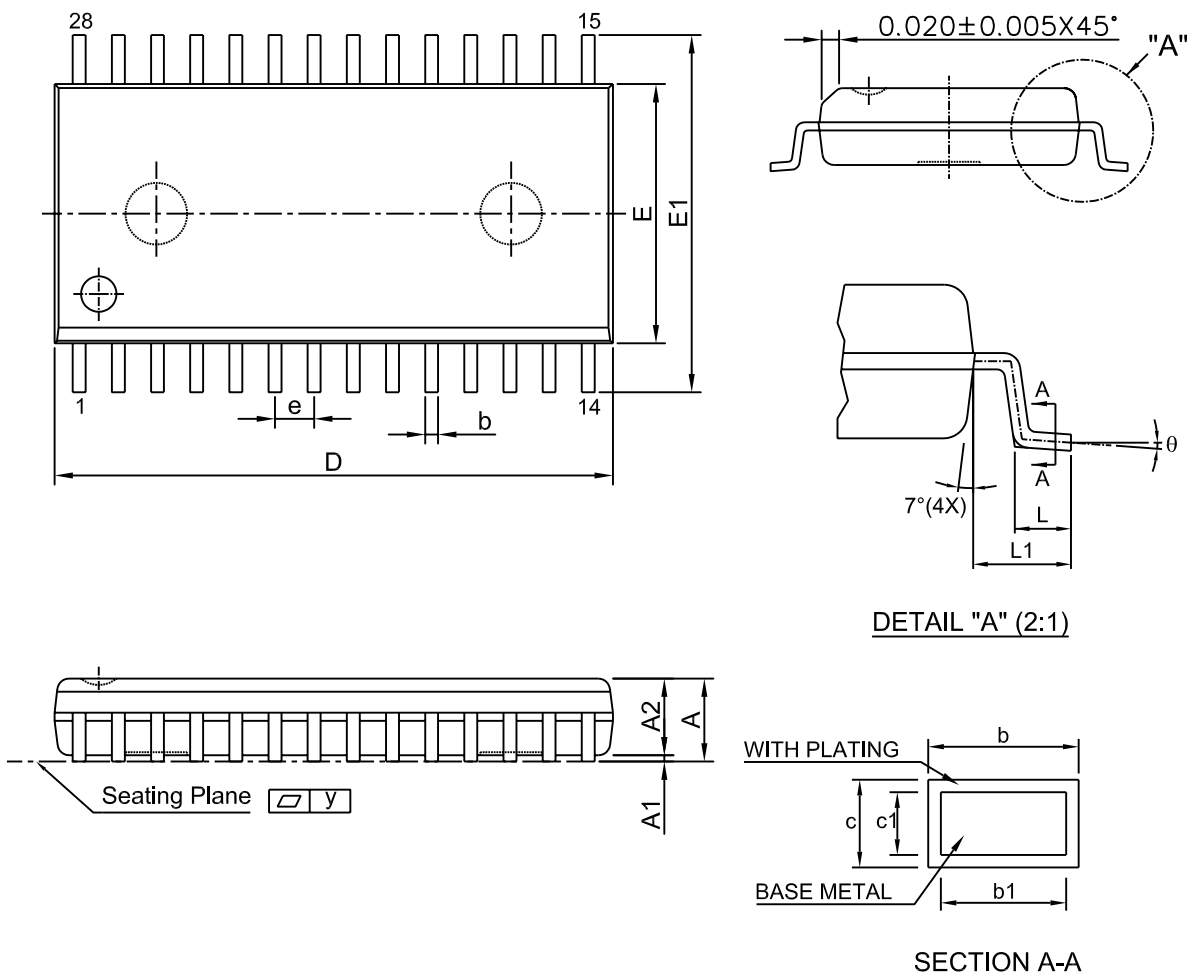
■ **ORDER INFORMATION**

CS18HS02563 X X X X XXX



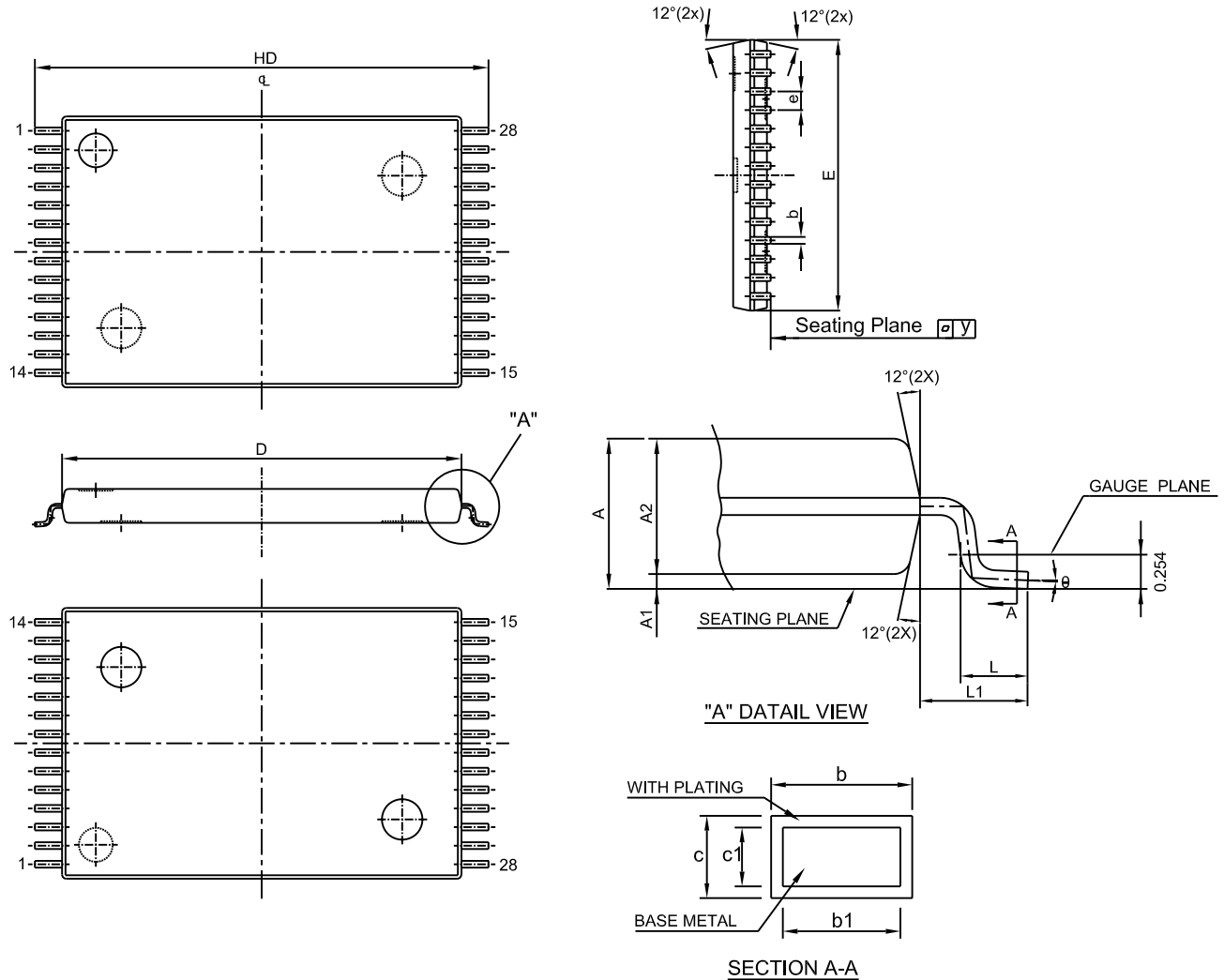
Note: Package material code "R" meets ROHS

■ PACKAGE DIMENSIONS - 28L SOP -330mil



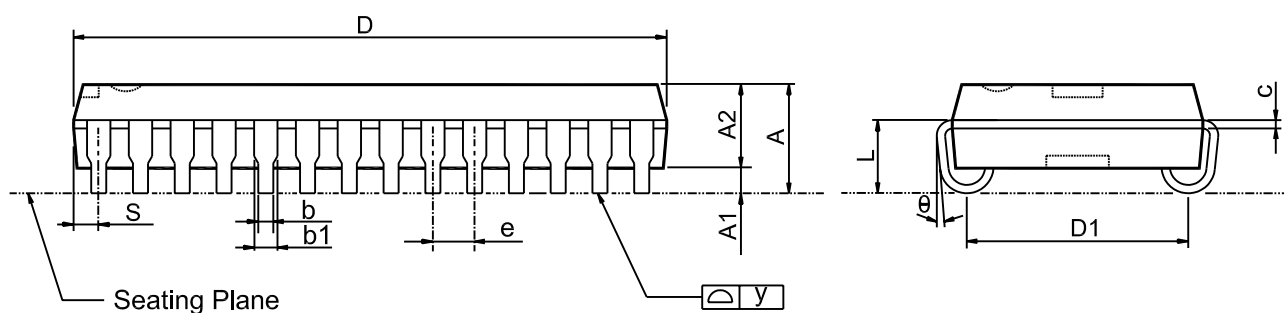
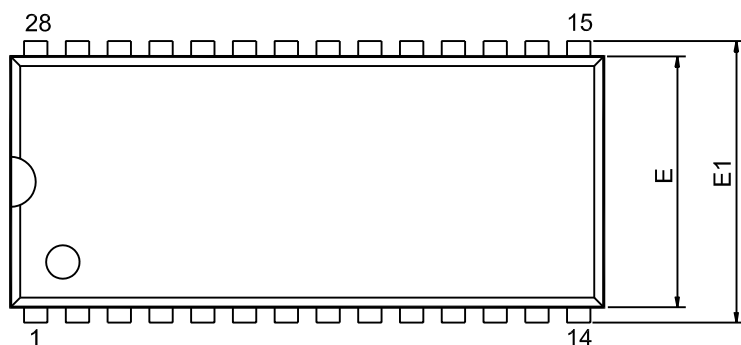
SYMBOL UNIT	A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ	
	mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	—
Nom.		2.692	0.226	2.489	—	—	—	—	18.110	8.407	11.811	1.270	0.964	1.720	—	—
Max.		2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	—	0°
	Nom.	0.106	0.009	0.098	—	—	—	—	0.713	0.331	0.465	0.050	0.0380	0.0677	—	—
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

■ PACKAGE DIMENSIONS - 28L TSOP 1- 8x13.4mm



UNIT	SYMBOL	A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
	mm	Min.	1.00	0.050	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.45	13.20	0.40	0.70	-
Nom.		1.10	0.115	1.00	0.22	0.20	-	-	11.80	8.00	0.55	13.40	0.50	0.80	-	-
Max.		1.20	0.180	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.65	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.0019	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.018	0.520	0.0157	0.0275	-	0°
	Nom.	0.0433	0.0045	0.039	0.009	0.008	-	-	0.465	0.315	0.022	0.528	0.0197	0.0315	-	-
	Max.	0.0473	0.0071	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.026	0.536	0.0277	0.0355	0.004	8°

■ PACKAGE DIMENSIONS - 28L SOJ -300mil



SYMBOL UNIT	A	A1	A2	b1	b	c	D	E	e	D1	E1	L	S	y	θ
	mm	Min. —	0.69	2.41	0.66	0.41	0.20	—	7.49	1.12	6.22	8.31	1.96	—	—
	Nom. —	—	2.54	0.71	0.46	0.25	18.03	7.62	1.27	6.73	8.56	2.21	—	—	—
	Max. 3.56	—	2.67	0.81	0.56	0.36	18.54	7.75	1.42	7.24	8.81	2.46	1.14	0.10	10°
inch	Min. —	0.027	0.095	0.026	0.016	0.008	—	0.295	0.044	0.245	0.327	0.077	—	—	0°
	Nom. —	—	0.100	0.028	0.018	0.010	0.710	0.300	0.050	0.265	0.337	0.087	—	—	—
	Max. 0.140	—	0.105	0.032	0.022	0.014	0.730	0.305	0.056	0.285	0.347	0.097	0.045	0.004	10°



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■ PACKAGE DIMENSIONS - 28L PDIP -300mil

